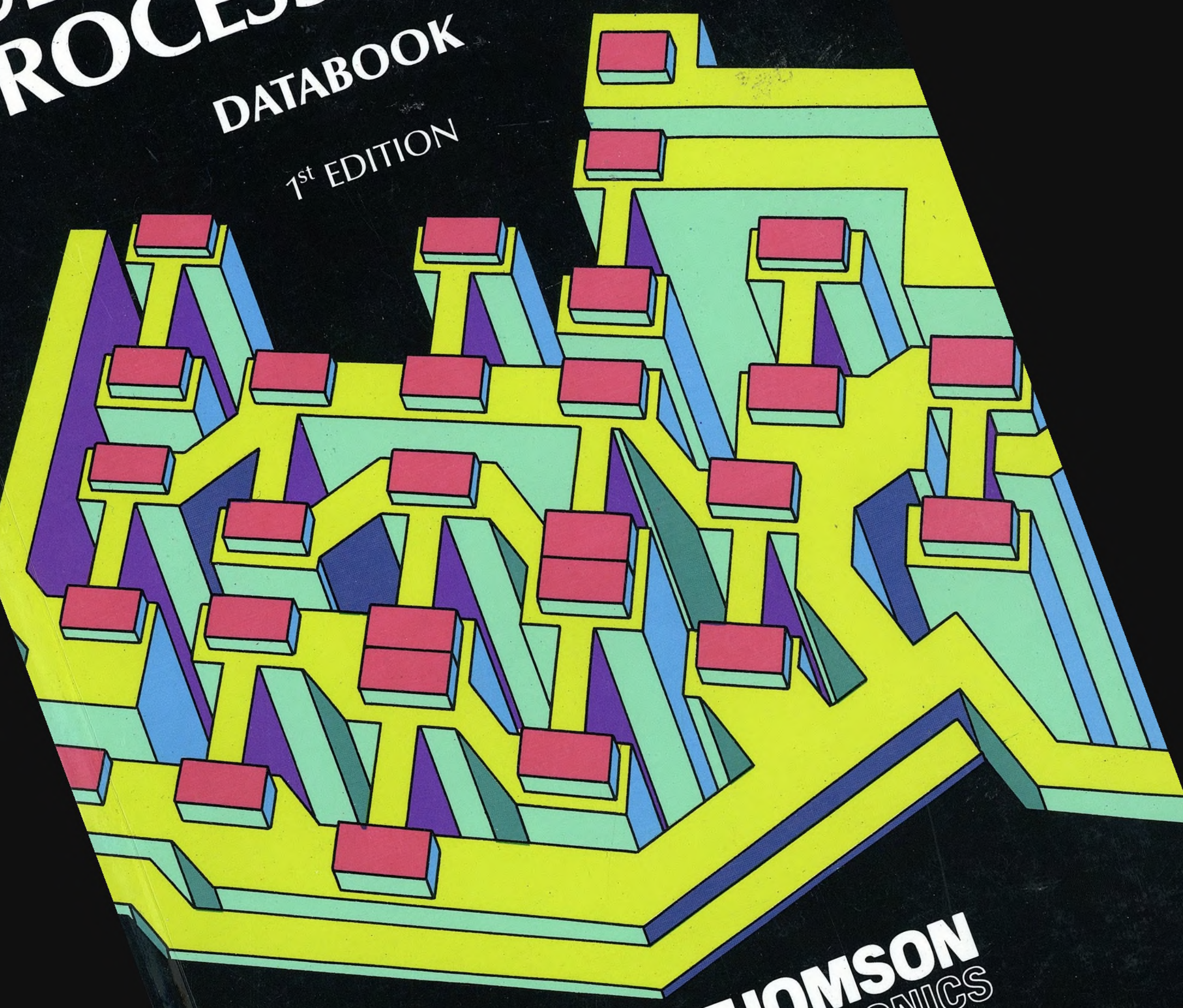
AUDIO POWER & PROCESSING ICs

DATABOOK

1st EDITION



SGS-THOMSON
MICROELECTRONICS

AUDIO POWER & PROCESSING ICs

DATABOOK

1st EDITION

JUNE 1991

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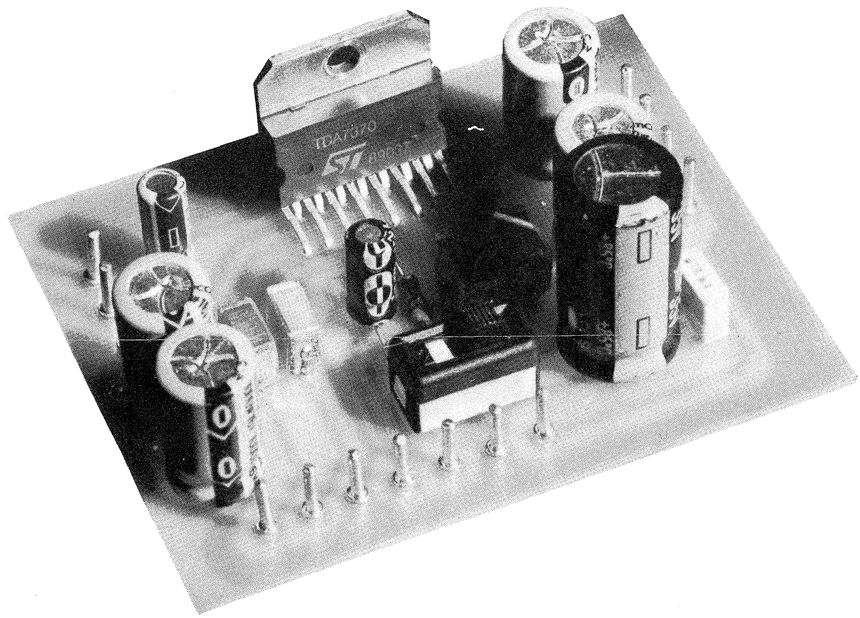
CONTINUOUS INNOVATION IN AUDIO ICs

In 1969 SGS-THOMSON Microelectronics developed the world's first monolithic audio power amplifier.Since then the company has always remained at the forefront in this field,designing many ICs that have become worldwide standards like the TDA2005 and TDA2030 and searching continually for innovative solution in technology,circuit design and packages.

These are just some of the SGS-THOMSON innovations:

* Fully complementary output stage thanks to new BTI technology; used in TDA7350 & TDA7360 (stereo) and TDA7370 (4 channel).
* Clipping detector circuit; used in TDA7360, TDA7362, TDA7363.
* High voltage bipolar technology used inTDA2050 & TDA2052.
* Mixed Bipolar technology to reach 100V.
* Pentawatt®, Heptawattt™, Multiwatt®, PowerDIP and Clipwatt™ power packages.

This technological leadership has brought with it an exceptional success in world markets: over the last 20 years SGS-THOMSON has sold almost 1.000.000.000 audio power amplifiers and production is still increasing yearly.



The TDA7370 a Unique Quad 6W Power Amplifier for Car-Radio.

INTRODUCTION

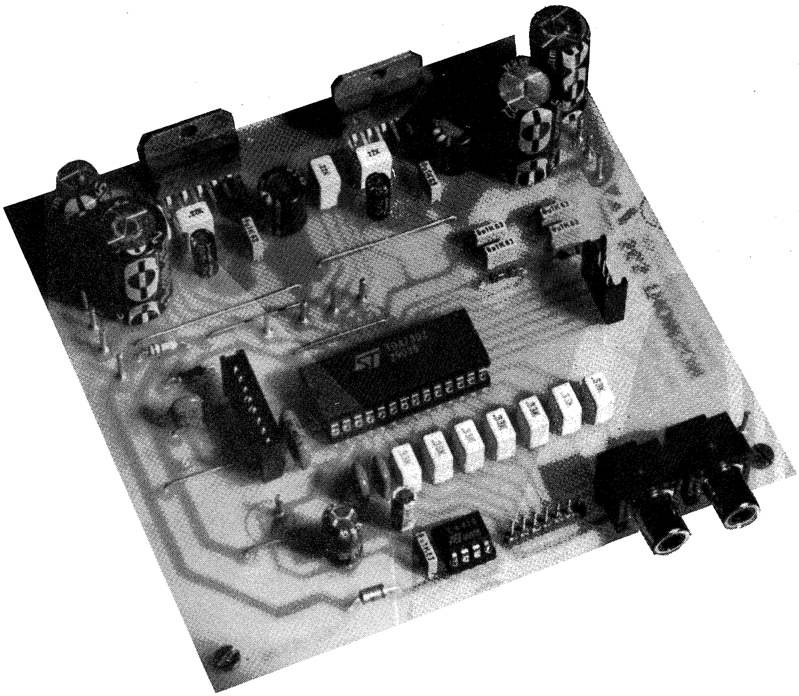
Audio amplifiers are just one part of the audio IC portfolio.SGS-THOMSON is also moving towards supplying global system solutions,developing a complete family of signal processing devices in CMOS and BiCMOS technologies.

Signal processing parts in this volume include:

* Digitally-controlled audio processors for car radio and TV applications (TDA73XX family).

* Dedicated filter & decoder for the Radio Data System (TDA7330 & TDA7332).

If you are designing an audio system,follow the example of some of the world's leading equipment houses and choose integrated circuits from SGS-THOMSON, the technology leader.Whatever your application you'll probably find the best solution right here in this book.



A Stereo 20+20 W System Completely Controlled By a Serial Bus Audio Processor.

ALPHANUMERICAL INDEX

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L272/M	Dual Power Operational Amplifiers	29
L272D	Dual Power Operational Amplifier	35
L2720/2/4	Low Drop Dual Power Operational Amplifiers	39
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L2750	Dual Low Drop High-Power Amplifier	51
L4901A	Dual 5V Regulator With Reset	59
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L4905	Dual 5V Regulator With Reset and Disable	95
L4915	Adjustable Voltage Regulator Plus Filter	103
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LS204	High Performance Dual Operational Amplifiers	121
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M3004AB1	Remote Control Transmitter	179
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M145026/7/8	Remote Control Encoder/Decoder Circuits	219
TBA810P	7W Audio Amplifier	231
TBA810S	7W Audio Amplifier	235
TBA820M	1.2W Audio Amplifier	239
TCA3189	FM IF High Quality Radio System	243
TDA1151	Motor Speed Regulator	247
TDA1154	Motor Speed Regulator	253
TDA1220B	AM-FM Quality Radio	257
TDA1904	4W Audio Amplifier	273
TDA1905	5W Audio Amplifier + Mute	281
TDA1908	8W Audio Amplifier	293
TDA1910	10W Audio Amplifier + Mute	303
TDA2003	10W Car-Radio Amplifier	315
TDA2004A	10+10W Stereo Amplifier for Car-Radio	325
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TDA2007A	6+6W Stereo Amplifier	367
TDA2008	12W Audio Amplifier	373
TDA2009	10+10W Quality Stereo Amplifier	381
TDA2009A	10+10W Quality Stereo Amplifier	391
TDA2030	14W Hi-Fi Audio Amplifier	401
TDA2030A	18W Hi-Fi Audio Amplifier	411
TDA2040	20W Hi-Fi Audio Amplifier	425
TDA2050	28W Hi-Fi Audio Amplifier	435
TDA2051	40W Hi-Fi Audio Amplifier	447
TDA2052	65W Hi-Fi Audio Amplifier With Mute/Stand-By	455
TDA2320A	Stereo Preamplifier	459
TDA2822	Dual 1.7 W Amplifier	469
TDA2822D	Dual 1W Amplifier	477
TDA2822M	Dual 1W Amplifier	481
TDA2824	Dual 1.7 W Amplifier	489
TDA2824S	Dual 1.7 W Amplifier	497
TDA3190	Complete TV Sound Channel	503
TDA3420/D	Dual Very Low-Noise Preamplifier	513
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TDA7211A	Low Voltage FM Front-End	531
TDA7220	Very Low Voltage AM/FM Radio	539
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TDA7231A	1.6W Audio Amplifier	561
TDA7233/D	1W Audio Amplifier + Mute	565
TDA7233S	1W Audio Amplifier + Mute	569
TDA7236/D	Very Low-Voltage Audio Bridge	573
TDA7240A	20W Amplifier for Car-Radio	577
TDA7241	20W Bridge Amplifier for Car-Radio	583
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TDA7245	5W Audio Amplifier	593
TDA7246	10W Audio Amplifer + Mute and Stand-By	603
TDA7250	Hi-Fi Dual Driver	609
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Type Number	Function	Page Number
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TDA7273/D	Stereo Cassette Playback System	647
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TDA7282/D	Stereo Low-Voltage Cassette Preamplifier	663
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TDA7285	Complete Stereo Cassette Player	681
TDA7300	Digital Control Stereo Audio Processor	689
TDA7302	Digital Control Stereo Audio Processor	703
TDA7306	Digital Control Stereo Audio Processor	715
TDA7318	Digital Control Stereo Audio Processor	727
TDA7326	AM/FM Radio Frequency Synthesizer	739
TDA7330	RDS Demodulator + Filter	751
TDA7332	RDS Filter	755
TDA7350	Bridge/Stereo Amplifier for Car-Radio	759
TDA7350A	Bridge/Stereo Amplifier for Car-Radio	779
TDA7353	24W Bridge/Stereo Amplifier for Car-Radio	799
TDA7360	Bridge/Stereo Amplifier + Clipping Detector	819
TDA7361	Low Voltage NBFM IF System	839
TDA7362	Stereo Amplifier + Clipping Detector	845
TDA7363	24W Bridge/Stereo + Clipping Detector	863
TDA7370	Quad Power Amplifier for Car-Radio	881
TDA7374	Dual Bridge Amplifier for Car-Radio	897
TDA8190	TV Sound Channel With DC Controls	909
TDA8191	TV Sound Channel	921
TDA8192	Multistandard AM/FM Sound IF for TV	927
TDA8196	Audio Switch & DC Volume Control	931
TDA8199	Stereo Amplifier & DC Volume Control for TV	937
TDB7910N	500mA Output Stage Power Operational Amplifier	939
TEA1330	Stereo Decoder	943
TEA2025B	2+2W Stereo Amplifier	949
TEA6420	Bus-Controlled Audio Matrix	953
TEB1033	High Performance Dual Operational Amplifier	957
TEB4033	High Performance Quad Operational Amplifier	965
TS271	Programmable Single CMOS Operational Amplifier	973
TS27L2	Very Low Power Dual CMOS Operational Amplifier	987
TS27M2	Low Power Dual CMOS Operational Amplifier	993

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Type Number	Function	Page Number
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TS27L4	Very Low Power Quad CMOS Operational Amplifier	1005
TS27M4	Low Power Quad CMOS Operational Amplifier	1011
TS274	High Speed Quad CMOS Operational Amplifier	1017
TS555	Low Power Single CMOS Timer	1023
TS556	Low Power Dual CMOS Timer	1031

SELECTION GUIDE

POWER AMPLIFIERS FOR CAR-RADIO

Type Number	Description	Packages	Page
TDA2003	10W Audio Amplifier	PENTAWATT	315
TDA2004A	10+10W Stereo Amplifier	MULTIWATT 11	325
TDA2005	20W Bridge Amplifier	MULTIWATT 11	333
TDA7240A	20W Bridge Amplifier	HEPTAWATT	577
TDA7241	20W Bridge Amplifier	HEPTAWATT	583
TDA7241B	20W Bridge Amplifier	HEPTAWATT	587
TDA7245	5W Audio Amplifier	POWERDIP (9+9)	593
TDA7246	10W Audio Amplifier + Mute and Stand-By	HEPTAWATT	603
TDA7256	22W Bridge Amplifier	MULTIWATT 11	617
TDA7350	22W Bridge/Stereo Amplifier	MULTIWATT 11	759
TDA7350A	22W Bridge/Stereo Amplifier	MULTIWATT 11	779
TDA7353	24W Bridge/Stereo Amplifier	MULTIWATT 11	799
TDA7360	2x12W Amplifier With Clipping Detector	MULTIWATT 11	819
TDA7362	Stereo Amplifier + Clipping Detector	MULTIWATT 11	845
TDA7363	24W Bridge/Stereo + Clipping Detector	MULTIWATT 11	863
TDA7370	Quad Power Amplifier for Car Radio	MULTIWATT 15	881
TDA7374	Dual Power Amplifier for Car-Radio	MULTIWATT 15	897

HI-FI AND HIGH QUALITY POWER AMPLIFIERS

Type Number	Description	Packages	Page
TDA1910	10W Audio Amplifier With Mute	MULTIWATT 11	303
TDA2006	12W Audio Amplifier	PENTAWATT	351
TDA2007	6+6W Stereo Amplifier	SIP9	361
TDA2007A	6+6W Stereo Amplifier	SIP9	367
TDA2009	10+10W Stereo Amplifier	MULTIWATT 11	381
TDA2009A	10+10W Short Circuit Protected Stereo	MULTIWATT 11	391
TDA2030	14W Audio Amplifier	PENTAWATT	401
TDA2030A	18W Amplifier and 35W Driver	PENTAWATT	411
TDA2040	20W Audio Power Amplifier	PENTAWATT	425
TDA2050	28W Hi-Fi Audio Amplifier	PENTAWATT	435
TDA2051	40W Hi-Fi Audio Amplifier	PENTAWATT	447
TDA2052	65W Hi-Fi Audio Amplifier With Mute-Stand-By	PENTAWATT	455
TDA7250	Hi-Fi Dual Driver	DIP20	609
TDA7262	20+20W High Quality TV Amplifier	MULTIWATT11	625

GENERAL PURPOSE POWER AMPLIFIERS

Type Number	Description	Packages	Page
TBA810P	7W Audio Amplifier	FINDIP	231
TBA810S	7W Audio Amplifier	FINDIP	235
TBA820M	1.2W Audio Amplifier	MINIDIP	239
TDA1904	4W Audio Amplifier	POWERDIP (8+8)	273
TDA1905	5W Audio Amplifier With Mute	POWERDIP (8+8)	281
TDA1908	8W Audio Amplifier	FINDIP	293
TDA1910	10W Audio Amplifier With Mute	MULTIWATT 11	303
TDA2007	6+6W Stereo Amplifier	SIP9	361
TDA2007A	6+6W Stereo Amplifier	SIP9	367
TDA2008	12W Audio Amplifier	PENTAWATT	373
TEA2025B	Stereo Amplifier	POWERDIP (12+2+2)	949
TDA2822	Dual 1.7 W Power Amplifier	POWERDIP (12+2+2)	469
TDA2822D	Dual 1W Power Amplifier	SO-16	477
TDA2822M	Dual Low-Voltage Power Amplifier	MINIDIP	481
TDA2824	Dual 1.7 W Power Amplifier	SIP9	489
TDA2824S	Dual Power Amplifier	SIP9	497
TDA7231A	1.6W Audio Amplifier	POWERDIP (4+4)	561
TDA7233/D	1W Audio Amplifier With Mute	MINIDIP, SO-8	565

LOW VOLTAGE POWER AMPLIFIERS and CASSETTE PLAYERS

Type Number	Description	Packages	Page
TDA2822M	1.2 W Audio Amplifier	MINIDIP	481
TDA7231A	1.6 W Audio Amplifier	MINIDIP, (4+4)	561
TDA7233/D	1W Audio Amplifier With Mute	MINIDIP, SO-8	565
TDA7233S	1W Audio Amplifier With Mute	SIP9	569
TDA7236/D	Very Low Voltage Audio Bridge	SO-8	573
TDA7273/D	Stereo Cassette Playback System	SO-16	647
TDA7284	Record/Playback Circuit With ALC	DIP14 - SO-14	669
TDA7285	Complete Stereo Cassette Player	DIP20, SO-20	681
TEA2025B	Stereo Amplifier	POWERDIP (12+2+2)	949

PREAMPLIFIERS AND AUDIO PROCESSORS

Type Number	Description	Packages	Page
TDA2320A	Stereo Preamplifier	MINIDIP	459
TDA3420/D	Dual Very Low Noise Preamplifier	DIP16, SO-16	513
TDA7282/D	Stereo Low Voltage Preamplifier	MINIDIP, SO-8	663
TDA7300	Digital Controlled Stereo Audio Processor	DIP28	689
TDA7302	Digital Controlled Stereo Audio Processor	DIP28	703
TDA7306	Digital Controlled Stereo Audio Processor	DIP28	715
TDA7318	Digital Controlled Stereo Audio Processor	DIP28 - SO-28	727
TEA6420	Audio Matrix	DIP24	953

RADIO CIRCUITS

Type Number	Description	Packages	Page
TCA3189	FM IF High Quality Radio System	DIP16	245
TDA1220B	AM/FM Quality Radio	DIP16	259
TDA7211A	Low Voltage FM Front-End	MINIDIP, SO-8	531
TDA7220	Very Low Voltage AM/FM Radio	DIP16, SO-16	539
TDA7222	3V AM/FM Single-Chip Radio	DIP24	551
TDA7227	Single-Chip AM/FM Radio With Front-End	DIP18	557
TDA7326	AM/FM Radio Frequency Synthesizer	DIP16, SO-16	739
TDA7330	RDS Demodulator + Filter	DIP20 - SO-20	751
TDA7332	RDS Filter	DIP14, SO-14	755
TDA7361	Low Voltage NBFM IF System	DIP16, SO-16	839
TEA1330	FM Stereo Decoder	DIP16	943

REMOTE CONTROL

Type Number	Description	Packages	Page
M3004AB1	Remote Control Transmitter	DIP20	179
M3004LAB1	Remote Control Transmitter	DIP20	187
M3005AB1	Remote Control Transmitter	DIP20	195
M3005LAB1	Remote Control Transmitter	DIP20	203
M3006LAB1	Remote Control Transmitter	DIP16	211
M145026/7/8	Remote Control Encoder/Decoder Circuits	DIP16, SO-16	219

TV SOUND CIRCUITS

Type Number	Description	Packages	Page
TDA3190	Complete TV Sound Channel	DIP16	503
TDA4190	TV Sound Channel With DC Controls	DIP20	519
TDA8190	TV Sound Channel With DC Controls	DIP20	909
TDA8191	TV Sound Channel	DIP20	921
TDA8192	Multistandard AM/FM Sound IF for TV	DIP20	927
TDA8196	Audio Switch & DC Volume Control	DIP8	931
TDA8199	Stereo Amplifier & DC Volume Control for TV	DIP20	937
TEA6420	Bus-Controlled Audio Matrix	DIP24	953

MOTOR CONTROLLERS

Type Number	Description	Packages	Page
L272/M	Dual Power Operational Amplifier	MINIDIP	29
L272D	Dual Power Operational Amplifier	SO-16	35
L2720/2/4	Low Drop Dual Power Operational Amplifier	8+8, MINIDIP, SIP9	39
L2726	Low Drop Dual Power Operational Amplifier	SO-20	47
L2750	Dual Low Drop High-Power Amplifier	MULTIWATT 11	51
TDA1151	Motor Speed Regulator	SOT-32	249
TDA1154	Speed Regulator for DC Motors	MINIDIP	255
TDA7271/2	High Performance Motor Speed Regulator	DIP20	631
TDA7274	Low Voltage DC Motor Speed Controller	MINIDIP	653
TDA7275A	Motor Speed Regulator	MINIDIP (4+4)	659

DEDICATED VOLTAGE REGULATORS

Type Number	Description	Packages	Page
L4901A	Dual 5V Regulator With Reset	HEPTAWATT	59
L4902A	Dual 5V Regulator With Reset and Disable	HEPTAWATT	69
L4903	Dual 5V Regulator With Reset and Disable	MINIDIP	79
L4904A	Dual 5V Regulator With Reset	MINIDIP	87
L4905	Dual 5V Regulator With Reset and Disable	HEPTAWATT	95
L4915	Adjustable Voltage Regulator Plus Filter	MINIDIP (4+4)	103
L4916	Voltage Regulator Plus Filter	MINIDIP (4+4)	109
L4918	Voltage Regulator Plus Filter	PENTAWATT, MINIDIP	115

CMOS OPERATIONAL AMPLIFIERS

Type Number	Description	Packages	Page
TS271	Programmable Single CMOS Operational Amplifier	DIP8, SO-8	973
TS27L2	Very Low Power Dual CMOS Operational Amplifier	DIP8, SO-8	987
TS27M2	Low Power Dual CMOS Operational Amplifier	DIP8, SO-8	993
TS272	High Speed Dual CMOS Operational Amplifier	DIP8, SO-8	999
TS27L4	Very Low Power Quad CMOS Operational Amplifier	DIP14, SO-14	1005
TS27M4	Low Power Quad CMOS Operational Amplifier	DIP14, SO-14	1011
TS274	High Speed Quad CMOS Operational Amplifier	DIP14, SO-14	1017

SPECIAL FUNCTIONS

Type Number	Description	Packages	Page
LS204	High Performance Dual Operational Amplifier	MINIDIP, SO-8	121
LS404	High Performance Quad Operational Amplifier	DIP14 - SO-14	131
M114A/AF	Digital Sound Generation	DIP40, DIP48	143
M114S/SF	Digital Sound Generation	DIP40, DIP48	161
TDB7910N	Power-500mA Output Stage	DIP16	939
TEB1033	High Performance Quad Operational Amplifier	DIP8 - SO-8	957
TEB4033	High Performance Dual Operational Amplifier	DIP14 - SO-14	965
TS555	Low Power Single CMOS Timers	DIP8 - SO-8	1023
TS556	Low Power Dual CMOS Timers	DIP14 - SO-14	1031

For detailed information on products referred to in the selection guide but not included as datasheet in this book, please refer to the databook indicated in column "DB"

SGS-THOMSON DATABOOKS

DB		ORDER CODE
a	4 BIT MCU FAMILY ET9400	DBET9400ST/1
b	8 BIT MCU FAMILIES EF6801/04/05	DB68XXST/1
c	16 BIT MPUs & ASSOCIATED PERIPHERALS	DB6800ST/1
d	AUTOMOTIVE PRODUCTS	DBAMOTIVEST/1
e	ANALOG CELLS AND ARRAYS	DBANACA/1090
f	CB12000 SERIES STANDARD CELLS	DBCB12ST/1
g	CMOS B SERIES	DBCMOSBST/1
h	CMOS LINEAR	BKCMOSLIN/0490
i	DATACOM PRODUCTS	DBDATACOMST/1
j	HIGH SPEED CMOS	DBHSCMOSST/1
k	IMAGE PROCESSING	DBIMAGEPROST/1
l	INDUSTRIAL and COMPUTER PERIPHERAL ICs	DBINDCOMPST/1
m	INDUSTY STANDARD ANALOG ICs	DBSTANDANAST/1
n	ISB12000 SERIES CONTINUOUS ARRAYS	DBISB12/1
o	ISB9000 SERIES CHANNELLESS LOGIC ARRAYS	DBISB9/2
p	LINE CARD ICs	DBLINCARDST/1
q	LOW POWER SCHOTTKY TTL ICs	DBLPSST/1
r	MODEM	DBMODEMST/1
s	NON - VOLATILE MEMORIES	DBNVMST/1
t	POWER BIPOLAR TRANSISTORS	DBBIPTRANST/1
u	POWER MODULES	DBPOMODULEST/1
v	POWER MOS DEVICES	DBPOWERMOSST/1
w	PROTECTION DEVICES	DBPROTECST/1
y	RF & MICROWAVE POWER TRANSISTORS	DBRFST/1
z	SMALL SIGNAL TRANSISTORS	DBSMSIGST/1
aa	STANDARD CELL LIBRARY	DASTACELL/2
ab	STATIC RAMs	DBSRAM/1
ac	ST8 MCU FAMILY	SGST8ST/1
ad	TELEPHONE SET ICs	DBTELSETST/1
ae	THE GRAPHICS DATABOOK	72TRN20400
af	THE L4970 SWITCHING REGULATOR IC FAMILY	BKL4970FA/0489
ag	THE TRANSPUTER DATABOOK	72TRN20300
ah	THE TRANSPUTER DEVELOPMENT AND iq SYSTEMS DATABOOK	72TRN21900
ai	THYRISTORS & TRIACS	DBTHYTRIACST/1
aj	VIDEO PRODUCTS SIGNAL PROCESSING	DBTVCRSPST/1
ak	VIDEO PRODUCTS POWER & GRAPHICS	DBPOMGRAST/1
al	Z8 MCU FAMILY	BKZ8SELEC/0289
am	Z80 MICROPROCESSOR FAMILY	DBZ80ST/1
an	ZENER, SCHOTTKY & RECTIFIER DIODES	DBDIODEST/1
* NOT INCLUDED IN CURRENT DATABOOKS. CONTACT YOUR NEAREST SGS-THOMSON SALES OFFICE		

VOLTAGE REGULATORS

STANDARD POSITIVE

I_o max (A)	Type Number	Regulated Output Voltage (V)												Precision %	Package	DB
		5	6	7.5	8	8.5	9	10	12	15	18	20	24			
2	L78S00CV	•		•			•	•	•	•	•		•	4	TO-220	m
	L78S00CT	•		•			•	•	•	•	•		•	4	TO-3	m
	L78S00T (**)	•		•			•	•	•	•	•		•	4	TO-3	m
1	L7800CV	•	•		•	•			•	•	•	•	•	4	TO-220	m
	L7800ABV (*)	•	•		•				•	•	•	•	•	2	TO-220	m
	L7800ACV	•	•		•				•	•	•	•	•	2	TO-220	m
	L7800CT	•	•		•	•			•	•	•	•	•	4	TO-3	m
	L7800T (**)	•	•		•	•			•	•	•	•	•	4	TO-3	m
0.5	L78M00ABV (*)	•	•		•				•	•	•	•	•	2	TO-220	m
	L78M00CV	•	•		•				•	•	•	•	•	4	TO-220	m
	L78M00CX	•	•		•				•	•	•	•	•	4	SOT-82	m
	L78M00CS	•	•		•				•	•	•	•	•	4	SOT-194	m
1	L7800CP	•	•		•	•			•	•	•	•	•	4	ISOWATT 220	m
0.5	L7800CP	•	•		•				•	•	•	•	•	4	ISOWATT 220	m

STANDARD NEGATIVE

I_o max (A)	Type Number	Regulated Output Voltage (V)										Precision %	Package	DB
		5	5.2	6	8	12	15	18	20	22	24			
1	L7900ACV	•	•	•	•	•	•	•	•	•	•	2	TO-220	m
	L7900CV	•	•	•	•	•	•	•	•	•	•	4	TO-220	m
	L7900CT	•	•	•	•	•	•	•	•	•	•	4	TO-3	m

(*) 40°C to 125°C

(**) –55°C to 150°C

PROPRIETARY

Type Number	Description	Package	DB
L4940 Series	1.5A Low-Drop Out Regulators	TO-220	m
L4941	1A Low-Drop Out Regulators	TO-220	m
TDA8134	600mA, 5V + 12V Dual Regulator With Disable	HEPTAWATT	ak, m
TDA8135	600mA, 5V + Adjustable Dual Regulator With Disable	HEPTAWATT	ak, m
TDA8136	600mA, 12V + 12V Dual Regulator With Disable	HEPTAWATT	ak, m
TDA8137	1A, 5,1V + 5,1V Dual Regulator With Disable + Reset	HEPTAWATT	ak, m
TDA8138	1A, 5,1V + 12V Dual Regulator With Disable + Reset	HEPTAWATT, SIP9	ak, m
TDA8139	1A, 5,1V + Adjustable Dual Regulator With Disable + Reset	SIP9	ak, m
TEA7605	500mA, 5V Very Low-Drop Out Regulator	TO-220	ak, m
TEA7610	500mA, 10V Very Low-Drop Out Regulator	TO-220	ak, m
TEA7685	500mA, 8,5V Very Low Drop Out Regulator	TO-220	ak, m

For detailed information on products referred to in the selection guide but not included as datasheet in this book, please refer to the databook indicated in column "DB"

HIGH CURRENT SWITCHING REGULATORS

Type Number	Description	Package	DB
L296/P	4 A Switching Regulator	MULTIWATT 15	l, m
L4960	2.5 A Power Switching Regulator	HEPTAWATT	l, m
L4962	1.5 A Power Switching Regulator	HEPTAWATT (12+2+2)	l, m
L4963	1.5 A Power Switching Regulator	POWERDIP (12+3+3)	l, m
L4964	4 A Switching Regulator	MULTIWATT 15	l, m
L4970A	10 A Switching Regulator	MULTIWATT 15	l, m
L4972A/AD	2A Switching Regulator	POWERDIP (16+2+2), SO-20	l, m
L4974A	3.5 A Switching Regulator	POWERDIP (16+2+2)	l, m
L4975A	5A Switching Regulator	MULTIWATT 15	l, m
L4977A	7A Switching Regulator	MULTIWATT 15	l, m

PWM CONTROLLERS

Type Number	Description	Package	DB
SG2524	Regulating Pulse Width Modulator (From –25° to + 85°C)	DIP16	l, m
SG2525A	Regulating Pulse Width Modulator (From –25° to + 85°C)	DIP16	l, m
SG2527A	Regulating Pulse Width Modulator (From –25° to + 85°C)	DIP16	l, m
SG3524	Regulating Pulse Width Modulator (From 0 to + 70°C)	DIP16	l, m
SG3525A	Regulating Pulse Width Modulator (From 0 to + 70°C)	DIP16	l, m
SG3527A	Regulating Pulse Width Modulator (From 0 to + 70°C)	DIP16	l, m
TDA4601	Free Frequency Running SMPS	SIP9	ak
TEA2018A	Fixed Frequency SMPS	DIP8	ak
TEA2019	Fixed Frequency SMPS With PLL	DIP14	ak
TEA2261	Fixed Frequency SMPS (Slave) + PLL + Stand-By	DIP16	ak
TEA5170	Fixed Frequency SMPS (Master)	DIP8	ak
UC2840	Regulating Pulse Width Modulator (From –25° to + 85°C)	DIP18	l, m
UC2842/3/4/5	Regulating Pulse Width Modulator (From –25° to + 85°C)	DIP14, MINIDIP	l, m
UC3840	Regulating Pulse Width Modulator (From 0 to + 70°C)	DIP18	l, m
UC3842/3/4/5	Regulating Pulse Width Modulator (From 0 to + 70°C)	DIP14, MINIDIP	l, m

POWER SWITCH

Type Number	Description	Package	DB
VN02	High Side Driver-$R_{DS(on)} \leq 0.5\ \Omega$	PENTAWATT	*
VN05	High Side Driver-$R_{DS(on)} \leq 0.2\ \Omega$	PENTAWATT	*
VN20	High Side Driver-$R_{DS(on)} \leq 0.05\ \Omega$	PENTAWATT	*

For detailed information on products referred to in the selection guide but not included as datasheet in this book, please refer to the databook indicated in column "DB"

EEPROMS

Capacity	Organization	Bus type	Part Number	Packages	Power Supply	Remark*	DB
256 Bits	16x16 SERIAL	MICROWIRE®	ST93C06B^x	PDIP8	5V		s
		MICROWIRE	ST93C06M^x	PSO8	5V		s
1K Bits	64x16 SERIAL or 128x8 SERIAL	MICROWIRE	ST93C46AB^x	PDIP8	5V		s
		MICROWIRE	ST93C46AM^x	PSO8	5V		s
1K Bits	64x16 SERIAL	MICROWIRE	ST93CS46B^x	PDIP8	5V	Write Protection Feature	s
		MICROWIRE	ST93CS46M^x	PSO8	5V	Write Protection Feature	s
		MICROWIRE	ST93CS47B^x	PDIP8	2.5V	Write Protection Feature	s
		MICROWIRE	ST93CS47M^x	PSO8	2.5V	Write Protection Feature	s
2K Bits	128x16 SERIAL	MICROWIRE	ST93CS56B^x	PDIP8	5V	Write Protection Feature	s
		MICROWIRE	ST93CS56M^x	PSO8	5V	Write Protection Feature	s
		MICROWIRE	ST93CS56ML^x	PSO14	5V	Write Protection Feature	s
		MICROWIRE	ST93CS57B^x	PDIP8	2.5V	Write Protection Feature	s
		MICROWIRE	ST93CS57M^x	PSO8	2.5V	Write Protection Feature	s
		MICROWIRE	ST93CS57ML^x	PSO14	2.5V	Write Protection Feature	s
2K Bits	256x8 SERIAL	I^2C	ST24C02AB^x	PDIP8	4.5 to 5.5V		s
		I^2C	ST24C02AM^x	PSO8	4.5 to 5.5V		s
		I^2C	ST25C02AB^x	PDIP8	2.5 to 5.5V		s
		I^2C	ST25C02AM^x	PSO8	2.5 to 5.5V		s
4K Bits	512x8 SERIAL	I^2C	ST24C04B^x	PDIP8	4.5 to 5.5V	Write Protection Feature	s
		I^2C	ST24C04ML^x	PSO14	4.5 to 5.5V	Write Protection Feature	s
		I^2C	ST25C04B^x	PDIP8	2.5 to 5.5V	Write Protection Feature	s
		I^2C	ST25C04ML^x	PSO14	2.5 to 5.5V	Write Protection Feature	s
8K Bits	1024x8 SERIAL	I^2C	ST24C08B^x	PDIP8	4.5 to 5.5V	Write Protection Feature	s

All products are available in 3 temperature ranges
Suffix x = 1 : 0°C to 70°C
Suffix x = 3 : -40°C to 125°C
Suffix x = 6 : -40°C to 85°C
• User defined size of memory section protected against write.

For detailed information on products referred to in the selection guide but not included as datasheet in this book, please refer to the databook indicated in column "DB"

DISCRETE AUDIO AMPLIFIERS
POWER BIPOLAR TRANSISTORS

Type Number	Complementary	V_{CEO}	V_{CBO}	I_C	h_{FE} @ I_C V_{CE}			$V_{CE(sat)}$ @ I_C I_B			R_{thj-c}	Packages	DB
		(V)	(V)	(A)		(A)	(V)	(V)	(A)	(mA)	(°C/W)		
2N3055	**MJ2955**	60	100	15	20	4.00	4.0	1.10	4.00	400	1.5	TO-3	t
2N4234		40	40	3	20	0.50	1.0	0.60	1.00	100	29	TO-39	t
2N4398	2N5301	40	40	30	15	15.00	2.0	1.00	15.00	1500	0.875	TO-3	t
2N4399	2N5302	60	60	30	15	15.00	2.0	1.00	15.00	1500	0.875	TO-3	t
2N4918	2N4921	40	40	1	30	0.50	1.0	0.60	1.00	100	4.16	SOT-32	t
2N4919	2N4922	60	60	1	30	0.50	1.0	0.60	1.00	100	4.16	SOT-32	t
2N4920	2N4923	80	80	1	30	0.50	1.0	0.60	1.00	100	4.16	SOT-32	t
2N4921	**2N4918**	40	40	1	30	0.50	1.0	0.60	1.00	100	4.16	SOT-32	t
2N4922	**2N4919**	60	60	1	30	0.50	1.0	0.60	1.00	100	4.16	SOT-32	t
2N4923	**2N4920**	80	80	1	30	0.50	1.0	0.60	1.00	100	4.16	SOT-32	t
2N5301	**2N4398**	40	40	30	15	15.00	2.0	1.00	15.00	1500	0.875	TO-3	t
2N5302	**2N4399**	60	60	30	15	15.00	2.0	1.00	15.00	1500	0.875	TO-3	t
2N5303	**2N5745**	80	80	20	15	10.00	2.0	1.50	15.00	1500	0.875	TO-3	t
2N5629	**2N6029**	100	100	16	25	8.00	2.0	1.00	10.00	1000	0.875	TO-3	t
2N5679	2N5681	100	100	1	40	0.25	2.0	1.00	0.50	50	17.5	TO-39	t
2N5680	2N5682	120	120	1	40	0.25	2.0	1.00	0.50	50	17.5	TO-39	t
2N5681	**2N5679**	100	100	1	40	0.25	2.0	1.00	0.50	50	17.5	TO-39	t
2N5682	**2N5680**	120	120	1	40	0.25	2.0	1.00	0.50	50	17.5	TO-39	t
2N5745	2N5303	80	80	20	15	10.00	2.0	1.50	15.00	1500	0.875	TO-3	t
2N6029	2N5629	100	100	16	25	8.00	2.0	1.00	10.00	1000	0.875	TO-3	t
2N6282	**2N6285**	60	60	20	750	10.00	3.0	3.00	20.00	200	1.09	TO-3	t
2N6283	**2N6286**	80	80	20	750	10.00	3.0	3.00	20.00	200	1.09	TO-3	t
2N6284	**2N6287**	100	100	20	750	10.00	3.0	3.00	20.00	200	1.09	TO-3	t
2N6285	2N6282	60	60	20	750	10.00	3.0	3.00	20.00	200	1.09	TO-3	t
2N6286	2N6283	80	80	20	750	10.00	3.0	3.00	20.00	200	1.09	TO-3	t
2N6287	2N6284	100	100	20	750	10.00	3.0	3.00	20.00	200	1.09	TO-3	t
BD135	**BD136**	45	45	1.5	25	0.50	2.0	0.50	0.50	50	10	SOT-32	t
BD136	BD135	45	45	1.5	25	0.50	2.0	0.50	0.50	50	10	SOT-32	t
BD137	**BD138**	60	60	1.5	25	0.50	2.0	0.50	0.50	50	10	SOT-32	t
BD138	BD137	60	60	1.5	25	0.50	2.0	0.50	0.50	50	10	SOT-32	t
BD139	**BD140**	80	80	1.5	25	0.50	2.0	0.50	0.50	50	10	SOT-32	t
BD140	BD139	80	80	1.5	25	0.50	2.0	0.50	0.50	50	10	SOT-32	t
BD331	**BD332**	60	60	6	750	3.00	3.0	2.00	3.00	12	2.08	SOT-82	t
BD332	BD331	60	60	6	750	3.00	3.0	2.00	3.00	12	2.08	SOT-82	t
BD333	**BD334**	80	80	6	750	3.00	3.0	2.00	3.00	12	2.08	SOT-82	t
BD334	BD333	80	80	6	750	3.00	3.0	2.00	3.00	12	2.08	SOT-82	t
BD335	**BD336**	100	100	6	750	3.00	3.0	2.00	3.00	12	2.08	SOT-82	t
BD336	BD335	100	100	6	750	3.00	3.0	2.00	3.00	12	2.08	SOT-82	t
BDX53	**BDX54**	45	45	8	750	3.00	3.0	2.00	3.00	12	2.08	TO-220	t
BDX53A	**BDX54A**	60	60	8	750	3.00	3.0	2.00	3.00	12	2.08	TO-220	t
BDX53B	**BDX54B**	80	80	8	750	3.00	3.0	2.00	3.00	12	2.08	TO-220	t
BDX53C	**BDX54C**	100	100	8	750	3.00	3.0	2.00	3.00	12	2.08	TO-220	t
BDX54	BDX53	45	45	8	750	3.00	3.0	2.00	3.00	12	2.08	TO-220	t
BDX54A	BDX53A	60	60	8	750	3.00	3.0	2.00	3.00	12	2.08	TO-220	t
BDX54B	BDX53B	80	80	8	750	3.00	3.0	2.00	3.00	12	2.08	TO-220	t
BDX54C	BDX53C	100	100	8	750	3.00	3.0	2.00	3.00	12	2.08	TO-220	t
BFX34		60	100	5	40	2.00	2.0	1.00	5.00	500	35	TO-39	t
BSS44		60	65	5	40	2.00	2.0	1.00	5.00	500	35	TO-39	t

PNP Type in bold

For detailed information on products referred to in the selection guide but not included as datasheet in this book, please refer to the databook indicated in column "DB"

DISCRETE AUDIO AMPLIFIERS (Cont'd)

POWER BIPOLAR TRANSISTORS (Cont'd)

Type Number	Complementary	V_{CEO} (V)	V_{CBO} (V)	I_C (A)	h_{FE} @ I_C V_{CE}	(A)	(V)	$V_{CE(sat)}$ @ I_C I_B (V)	(A)	(mA)	R_{thj-c} (°C/W)	Packages	DB
BUY68		60	100	7	40	1.00	1.0	1.00	5.00	500	17.5	TO-39	t
MJ2955	2N3055	60	100	15	20	4.00	4.0	1.10	4.00	400	1.5	TO-3	t
MJ4030	MJ4033	60	60	16	1000	10.00	3.0	4.00	16.00	80	1.17	TO-3	t
MJ4031	MJ4034	80	80	16	1000	10.00	3.0	4.00	16.00	80	1.17	TO-3	t
MJ4032	MJ4035	100	100	16	1000	10.00	3.0	4.00	16.00	80	1.17	TO-3	t
MJ4033	**MJ4030**	60	60	16	1000	10.00	3.0	4.00	16.00	80	1.17	TO-3	t
MJ4034	**MJ4031**	80	80	16	1000	10.00	3.0	4.00	16.00	80	1.17	TO-3	t
MJ4035	**MJ4032**	100	100	16	1000	10.00	3.0	4.00	16.00	80	1.17	TO-3	t
MJ4502	MJ802	90	100	30	25	7.50	2.0	0.80	7.50	750	0.875	TO-3	t
MJ11011	MJ11012	60	60	30	1000	20.00	5.0	4.00	30.00	300	0.875	TO-3	t
MJ11012	**MJ11011**	60	60	30	1000	20.00	5.0	4.00	30.00	300	0.875	TO-3	t
MJ11013	MJ11014	90	90	30	1000	20.00	5.0	4.00	30.00	300	0.875	TO-3	t
MJ11014	**MJ11013**	90	90	30	1000	20.00	5.0	4.00	30.00	300	0.875	TO-3	t
MJ11015	MJ11016	120	120	30	1000	20.00	5.0	4.00	30.00	300	0.875	TO-3	t
MJ11016	**MJ11015**	120	120	30	1000	20.00	5.0	4.00	30.00	300	0.875	TO-3	t
MJE170	MJE180	40	60	3	30	0.50	1.0	0.90	1.50	150	10	SOT-32	t
MJE171	MJE181	60	80	3	30	0.50	1.0	0.90	1.50	150	10	SOT-32	t
MJE172	MJE182	80	100	3	30	0.50	1.0	0.90	1.50	150	10	SOT-32	t
MJE180	**MJE170**	40	60	3	30	0.50	1.0	0.90	1.50	150	10	SOT-32	t
MJE181	**MJE171**	60	80	3	30	0.50	1.0	0.90	1.50	150	10	SOT-32	t
MJE182	**MJE172**	80	100	3	30	0.50	1.0	0.90	1.50	150	10	SOT-32	t
MJE200	**MJE210**	25	40	5	70	0.50	1.0	0.30	0.50	50	8.34	SOT-32	t
MJE210	MJE200	25	40	5	70	0.50	1.0	0.30	0.50	50	8.34	SOT-32	t
MJE370	MJE520	30	30	3	25	1.00	1.0				5	SOT-32	t
MJE371	MJE521	40	40	4	40	1.00	1.0				3.12	SOT-32	t
MJE520	**MJE370**	30	30	3	25	1.00	1.0				5	SOT-32	t
MJE521	**MJE371**	40	40	4	40	1.00	1.0				3.12	SOT-32	t
MJE2955T	MJE3055T	60	70	10	20	4.00	4.0	1.10	4.00	400	1.66	TO-220	t
MJE3055T	**MJE2955T**	60	70	10	20	4.00	4.0	1.10	4.00	400	1.66	TO-220	t
SGSD100	**SGSD200**	80	80	25	300	20.00	3.0	1.75	10.00	40	0.96	TO-218	t
SGSD200	SGSD100	80	80	25	300	20.00	3.0	1.75	10.00	40	0.96	TO-218	t
TIP35A	**TIP36A**	60	100	25	10	15.00	4.0	1.80	15.00	1500	1	TO-218	t
TIP35B	**TIP36B**	80	120	25	10	15.00	4.0	1.80	15.00	1500	1	TO-218	t
TIP35C	**TIP36C**	100	140	25	10	15.00	4.0	1.80	15.00	1500	1	TO-218	t
TIP36A	TIP35A	60	100	25	10	15.00	4.0	1.80	15.00	1500	1	TO-218	t
TIP36B	TIP35B	80	120	25	10	15.00	4.0	1.80	15.00	1500	1	TO-218	t
TIP36C	TIP35C	100	140	25	10	15.00	4.0	1.80	15.00	1500	1	TO-218	t
TIP140	**TIP145**	60	60	10	1000	5.00	4.0	3.00	10.00	40	1	TO-218	t
TIP140T	**TIP145T**	60	60	15	1000	5.00	4.0	3.00	10.00	40	1.25	TO-220	t
TIP141	**TIP146**	80	80	10	1000	5.00	4.0	3.00	10.00	40	1	TO-218	t
TIP141T	**TIP146T**	80	80	15	1000	5.00	4.0	3.00	10.00	40	1.25	TO-220	t
TIP142	**TIP147**	100	100	10	1000	5.00	4.0	3.00	10.00	40	1	TO-218	t
TIP142T	**TIP147T**	100	100	15	1000	5.00	4.0	3.00	10.00	40	1.25	TO-220	t
TIP145	TIP140	60	60	10	1000	5.00	4.0	3.00	10.00	40	1	TO-218	t
TIP145T	TIP140T	60	60	15	1000	5.00	4.0	3.00	10.00	40	1.25	TO-220	t
TIP146	TIP141	80	80	10	1000	5.00	4.0	3.00	10.00	40	1	TO-218	t
TIP146T	TIP141T	80	80	15	1000	5.00	4.0	3.00	10.00	40	1.25	TO-220	t
TIP147	TIP142	100	100	10	1000	5.00	4.0	3.00	10.00	40	1	TO-218	t

PNP Type in bold

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DISCRETE AUDIO AMPLIFIERS (Cont'd)

POWER BIPOLAR TRANSISTORS (Cont'd)

Type Number	Complementary	V_{CEO} (V)	V_{CBO} (V)	I_C (A)	h_{FE} @ I_C V_{CE}	(A)	(V)	$V_{CE(sat)}$ @ I_C I_B (V)	(A)	(mA)	R_{thj-c} (°C/W)	Packages	DB
TIP147T	TIP142T	100	100	15	1000	5.00	4.0	3.00	10.00	40	1.25	TO-220	t
TIP2955	TIP3055	60	100	15	20	4.00	4.0	1.10	4.00	400	1.39	TO-218	t
TIP3055	**TIP2955**	60	100	15	20	4.00	4.0	1.10	4.00	400	1.39	TO-218	t

PNP Type in bold.

POWER MOS TRANSISTORS

V_{DSS} (V)	$R_{DS(on)}$ max (Ω)	I_D max (A)	P_{tot} (W)	Type Number	Packages	DB
50	0.040	30.0	75	BUZ11	TO-220	v
50	0.060	25.0	75	BUZ11A	TO-220	v
50	0.040	20.0	35	BUZ11FI	ISOWATT 220	v
50	0.100	14.0	40	BUZ71	TO-220	v
50	0.120	13.0	40	BUZ71A	TO-220	v
50	0.120	11.0	30	BUZ71AFI	ISOWATT 220	v
50	0.100	12.0	30	BUZ71FI	ISOWATT 220	v
50	0.028	35.0	125	IRFZ40	TO-220	v
50	0.028	26.0	40	IRFZ40FI	ISOWATT 220	v
50	0.035	35.0	125	IRFZ42	TO-220	v
50	0.035	23.0	40	IRFZ42FI	ISOWATT 220	v
50	0.016	70.0	180	STH70N05	TO-218	*
50	0.016	52.0	70	STH70N05FI	ISOWATT 218	*
50	0.023	52.0	125	STVHD90	TO-220	v
50	0.023	0.0	0	STVHD90FI	ISOWATT 220	*
50	0.023	60.0	150	STH60N05	TO-218	*
50	0.023	40.0	65	STH60N05FI	ISOWATT 218	*
60	0.150	12.0	40	MTP3055F	TO-220	*
60	0.150	12.0	40	MTP3055EFI	TO-220	*
60	0.080	25.0	100	STP25N06	TO-220	*
60	0.014	75.0	180	STH75N06	TO-218	*
60	0.014	55.0	70	STH75N06FI	ISOWATT 218	*
60	0.028	50.0	125	STP50N06	TO-220	*
60	0.028	–	40	STP50N06FI	ISOWATT 220	*
60	0.023	55.0	125	STP55N06	TO-220	*
60	0.023	–	40	STP55N06FI	ISOWATT 220	v
80	0.077	28.0	125	IRF141	TO-3	v
80	0.055	33.0	150	IRF151	TO-3	*
80	0.540	5.6	43	IRF511	TO-220	*
80	0.270	9.2	60	IRF521	TO-220	v
80	0.270	7.0	30	IRF521FI	ISOWATT 220	v
80	0.160	14.0	79	IRF531	TO-220	v
80	0.160	9.0	35	IRF531FI	ISOWATT 220	v
80	0.077	28.0	125	IRF541	TO-220	v
80	0.077	15.0	40	IRF541FI	ISOWATT 220	v
80	0.077	31.0	150	IRFP141	TO-218	*

For detailed information on products referred to in the selection Guide but not included as datasheet in this book please refer to the databook indicated in column "DB"

DISCRETE AUDIO AMPLIFIERS (Cont'd)

POWER MOS TRANSISTORS (Cont'd)

V_{DSS} (V)	$R_{DS(on)}$ max (Ω)	I_D max (A)	P_{tot} (W)	Type Number	Packages	DB
80	0.077	20.0	60	IRFP141FI	ISOWATT 218	*
80	0.055	40.0	150	IRFP151	TO-218	v
80	0.055	26.0	65	IRFP151FI	ISOWATT 218	v
100	0.100	19.0	75	BUZ21	TO-220	v
100	0.250	9.0	40	BUZ72A	TO-220	v
100	0.077	28.0	125	IRF140	TO-3	v
100	0.055	40.0	150	IRF150	TO-3	v
100	0.540	5.6	43	IRF510	TO-220	*
100	0.270	9.2	60	IRF520	TO-220	v
100	0.270	7.0	30	IRF520FI	ISOWATT 220	v
100	0.160	14.0	79	IRF530	TO-220	v
100	0.160	9.0	35	IRF530FI	ISOWATT 220	v
100	0.077	28.0	125	IRF540	TO-220	v
100	0.077	15.0	40	IRF540FI	ISOWATT 220	v
100	0.077	31	150	IRFP140	TO-218	*
100	0.077	20.0	60	IRFP140FI	ISOWATT 218	*
100	0.055	40.0	150	IRFP150	TO-218	v
100	0.055	26.0	65	IRFP150FI	ISOWATT 218	v
150	0.800	5.0	40	IRF621	TO-220	v
150	0.800	4.0	30	IRF621FI	ISOWATT 220	v
200	0.400	9.5	75	BUZ32	TO-220	v
200	0.180	18.0	125	IRF240	TO-3	*
200	0.085	–	–	IRF250	TO-3	*
200	0.800	5.0	40	IRF620	TO-220	v
200	0.800	4.0	30	IRF620FI	ISOWATT 220	v
200	0.180	18.0	125	IRF640	TO-220	*
200	0.085	33.0	180	STH33N20	TO-218	*
200	0.085	20.0	70	STH33N20FI	ISOWATT 218	*
250	0.750	–	–	STP6N25FI	ISOWATT 220	*
350	1.800	3.3	50	IRF721	TO-220	v
350	1.800	2.5	30	IRF721FI	ISOWATT 220	v
350	1.000	5.5	75	IRF731	TO-220	v
350	1.000	3.5	35	IRF731FI	ISOWATT 220	v
350	0.550	10.0	125	IRF741	TO-220	v
350	0.550	5.5	40	IRF741FI	ISOWATT 220	v
400	0.300	15.0	150	IRF350	TO-3	v
400	1.800	3.3	50	IRF720	TO-220	v
400	1.800	2.5	30	IRF720FI	ISOWATT 220	v
400	1.000	5.5	75	IRF730	TO-220	v
400	1.000	3.5	35	IRF730FI	ISOWATT 220	v
400	0.550	10.0	125	IRF740	TO-220	v
400	0.550	5.5	40	IRF740FI	ISOWATT 220	v
400	0.300	16.0	180	IRFP350	TO-218	*
400	0.300	10.0	70	IRFP350FI	ISOWATT 218	*
450	0.400	13.0	150	IRF451	TO-3	v
450	3.000	2.5	50	IRF821	TO-220	v

For detailed information on products referred to in the selection Guide but not included as datasheet in this book please refer to the databook indicated in column "DB"

DISCRETE AUDIO AMPLIFIERS (Cont'd)

POWER MOS TRANSISTORS (Cont'd)

V_{DSS} (V)	$R_{DS(on)}$ max (Ω)	I_D max (A)	P_{tot} (W)	Type Number	Packages	DB
450	3.000	2.0	30	IRF821FI	ISOWATT 220	v
450	1.500	4.5	75	IRF831	TO-220	v
450	1.500	3.0	35	IRF831FI	ISOWATT 220	v
450	0.850	8.0	125	IRF841	TO-220	v
450	0.850	4.5	40	IRF841FI	ISOWATT 220	v
450	0.850	5.5	60	IRFP441FI	ISOWATT 218	*
450	0.400	14.0	180	IRFP451	TO-218	v
450	0.400	9.0	70	IRFP451FI	ISOWATT 218	v
500	0.600	9.5	125	BUZ353	TO-218	v
500	0.400	13.0	150	IRF450	TO-3	v
500	3.000	2.5	50	IRF820	TO-220	v
500	3.000	2.0	30	IRF820FI	ISOWATT 220	v
500	1.500	4.5	75	IRF830	TO-220	v
500	1.500	3.0	35	IRF830FI	ISOWATT 220	v
500	0.850	8.0	125	IRF840	TO-220	v
500	0.850	4.5	40	IRF840FI	ISOWATT 220	v
500	0.850	5.5	60	IRFP440FI	ISOWATT 218	*
500	0.400	14.0	180	IRFP450	TO-218	v
500	0.400	9.0	70	IRFP450FI	ISOWATT 218	v

For detailed information on products referred to in the selection Guide but not included as datasheet in this book please refer to the databook indicated in column "DB"

DISCRETE AUDIO AMPLIFIERS (Cont'd)
SMALL SIGNAL TRANSISTORS IN TO-39

V_{CEO} V_{CER}*	h_{FE} @ I_C		Type		$V_{CE(sat)}$ @ I_C / I_B		f_T	t_s t_{off}*	P_{tot}	DB
			NPN	PNP	max		min			
(V)	min/max	(mA)			(V)	(mA)	(MHz)	(ns)	(mW)	
30	40/120	150	BSY53		1.2	500/50	100 typ	–	800	z
30	100/300	150	BSY54		1.2	500/50	100 typ	–	800	z
40	40/120	150		2N2904	0.4	150/15	200	80	600	z
40	40/120	150	2N3110		0.25	150/15	60	1000*	800	z
40	40/240	500	BC440		1	1000/100	50	–	1000	z
40	40/250	100	BC140		0.35 typ	500/50	50	850*	800	z
40	40/250	500		BC460	1	1000/100	50	–	1000	z
40	50/250	150	2N3053		1.4	150/15	100 typ	–	800	z
40	100/230	150		2N2905	0.4	150/15	200	80	600	z
40	100/300	150	2N3109		0.25	150/15	70	1000*	800	z
45	40/240	150		BC304	0.65	150/15	100 typ	–	850	z
45	120/240	150	BC302		0.5	150/15	100 typ	–	850	z
50	40/250	500		2N5323	1.2	500/50	50	–	1000	z
50	40/250	500	2N5321		0.8	500/50	50	800*	1000	z
50*	40/120	150	2N1613		1.5	150/15	60	–	800	z
50*	100/300	150	2N1711		1.5	150/15	70	–	800	z
60	40/120	150		2N2904A	0.4	150/15	200	80	600	z
60	40/120	150	2N3108		1.4	150/15	100 typ	–	800	z
60	40/240	150		BC303	0.65	150/15	75	–	850	z
60	40/240	150	BC301		0.5	150/15	120 typ	–	800	z
60	40/240	500	BC441		1	1000/100	50	–	1000	z
60	40/250	100	BC141		0.35 typ	500/50	50	850*	800	z
60	40/250	500		BC461	1	1000/100	50	–	1000	z
60	100/300	150		2N2905A	0.4	150/15	200	80	600	z
60	100/300	150	2N3107		1.4	150/15	100 typ	–	800	z
75	30/130	500		2N5322	0.7	500/50	50	1000*	1000	z
75	30/130	500	2N5320		0.5	500/50	50	800*	1000	z
80	40/120	150	2N1893		5	150/15	50	–	800	z
80	40/120	150	BSY55		0.6	150/15	100 typ	–	800	z
80	40/240	150	BC300		0.5	150/15	120 typ	–	800	z
80	100/300	150	BSY56		0.6	150/15	100 typ	–	800	z

For detailed information on products referred to in the selection guide but not included as datasheet in this book, please refer to the databook indicated in column "DB"

DISCRETE AUDIO AMPLIFIERS (Cont'd)

SMALL SIGNAL TRANSISTORS IN TO-18

V_{CEO} V_{CER}* (V)	h_{FE} @ I_C min/max	h_{FE} @ I_C (mA)	Type NPN	Type PNP	$V_{CE(sat)}$ @ I_C / I_B max (V)	$V_{CE(sat)}$ @ I_C / I_B (mA)	f_T min (MHz)	t_s t_{off}* (ns)	P_{tot} (mW)	DB
25	50/–	10		BCY72	0.5	50/5	200	350	350	z
25	75/260	100	BC377		0.7	500/50	300 typ	–	375	z
30	100/300	150	2N3302		0.6	500/50	–	150*	360	z
40	40/120	150		2N2906	1.6	500/50	200	80	400	z
40	50/–	10		BCY70	0.5	50/5	250	350	350	z
40	75/260	100	BC378		0.7	500/50	300 typ	–	375	z
40	100/300	150		2N2907	1.6	500/50	200	80	400	z
45	100/300	150		2N3504	1.6	500/50	200	100*	400	z
45	100/600	10		BCY71	0.5	50/5	200	–	350	z
50*	40/120	150	2N718A		1.5	150/15	60	–	500	z
50*	100/300	150	2N956		1.5	150/15	70	–	500	z
60	40/120	150		2N2906A	1.6	500/50	200	80	400	z
60	100/300	150		2N2907A	1.6	500/50	200	80	400	z
60	100/300	150		2N3505	1.6	500/50	200	100*	400	z
80	40/–	150	2N720A		1.2	50/5	–	–	500	z

LOW LEVEL, LOW NOISE TRANSISTORS IN TO-18

V_{CEO} V_{CER}* (V)	h_{FE} @ I_C min/max	h_{FE} @ I_C (mA)	Type NPN	Type PNP	$V_{CE(sat)}$ @ I_C / I_B max (V)	$V_{CE(sat)}$ @ I_C / I_B (mA)	f_T min (MHz)	NF (dB)	P_{tot} (mW)	DB
20	110/800■	2	BC108		0.6	100/5	100	10	300	z
20	200/800■	2	BC109		0.6	100/5	100	4	300	z
20	240/500■	2		BC179	0.25	10/0.5	200 typ	4	300	z
25	125/500■	2		BC178	0.25	10/0.5	200 typ	10	300	z
32	120/630	2	BCY58		0.35	10/0.25	200 typ	6	360	z
32	120/460	2		BCY78	0.8	100/2.5	180 typ	6	360	z
40	110/450	2		BC478	0.25	10/0.5	150 typ	6	360	z
40	200/–	2		BC479	0.25	10/0.5	–	4	360	z
45	100/500	0.01	2N930		1	10/0.5	30	3	300	z
45	110/450■	2	BC107		0.6	100/5	100	10	300	z
45	120/460	2		BCY79	0.8	100/2.5	180 typ	6	360	z
45	120/630	2	BCY59		0.7	100/2.5	200 typ	6	360	z
45	125/500■	2		BC177	0.25	10/0.5	200 typ	10	300	z
45	250/500	0.01		2N3964	0.25	10/0.5	50	2	360	z
60	130/–	0.01	BFR17		1	1/0.1	70	3	360	z
60	100/300	0.01		2N3962	0.25	10/0.5	40	3	360	z
60	100/500	0.01	2N2484		0.35	1/0.1	60	2	360	z
60	150/300	1	BFY76		0.35	1/0.1	100	4	360	z
60	250/500	0.01		2N3965	0.25	10/0.5	50	4	360	z
80	70/230	0.01		BFX37	0.4	50/5	40	3.5	360	z
80	100/300	0.01		2N3963	0.25	10/0.5	40	3	360	z
80	110/250	2		BC477	0.25	10/0.5	150 typ	10	360	z

■ h_{fe} @ 1 KHz

For detailed information on products referred to in the selection guide but not included as datasheet in this book, please refer to the databook indicated in column "DB"

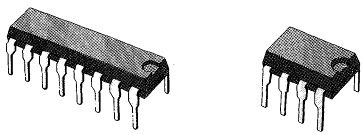
DATASHEETS

DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272 and L272M are monolithic integrated circuits in powerdip and minidip packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8) **Minidip Plastic**

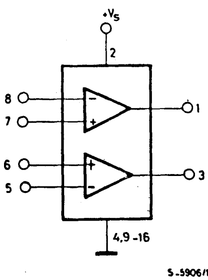
ORDERING NUMBERS:

L272 L272M

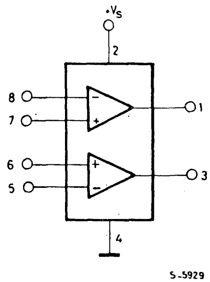
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C **(L272)**, T_{amb} = 50°C **(L272M)** T_{case} = 75°C **(L272)**	1.2 5	W W
T_{op}	Operating Temperature	−40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	−40 to 150	°C

BLOCK DIAGRAM

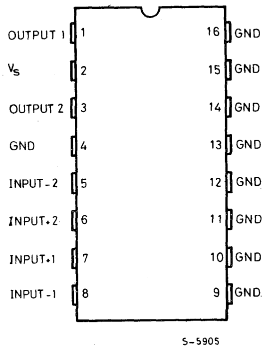


L272

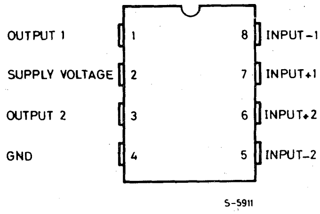


L272M

CONNECTION DIAGRAM
(Top view)

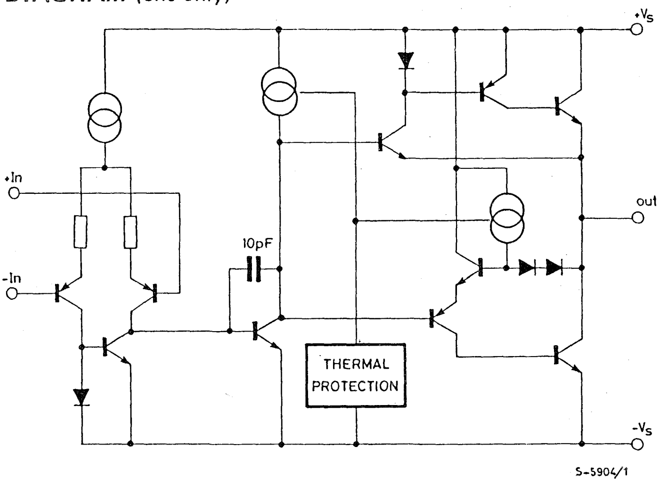


L272



L272M

SCHEMATIC DIAGRAM (one only)



THERMAL DATA			Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70°C/W	100°C/W

* Thermal resistance junction-pin 4

ELECTRICAL CHARACTERISTICS ($V_s = 24V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$; $V_s = 24V$		8	12	mA
		$V_o = \frac{V_s}{2}$; $V_s = 12V$		7.5	11	mA
I_b	Input bias current			0.3	2.5	μA
V_{os}	Input offset voltage			15	60	mV
I_{os}	Input offset current			50	250	nA
SR	Slew rate			1		V/μs
B	Gain-bandwidth product			350		KHz
R_i	Input resistance		500			KΩ
G_v	O.L. voltage gain	f = 100Hz	60	70		dB
		f = 1KHz		50		dB
e_N	Input noise voltage	B = 20KHz		10		μV
I_N	Input noise current	B = 20KHz		200		pA
CRR	Common Mode rejection	f = 1KHz	60	75		dB
SVR	Supply voltage rejection	f = 100Hz; R_G = 10KΩ; V_R = 0.5V; V_s = 24V		70		dB
		V_s = ±12V	54	62		dB
		V_s = ± 6V		56		dB
V_o	Output voltage swing	I_p = 0.1A		23		V
		I_p = 0.5A	21	22.5		V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB; V_s = 24V		60		dB
		V_s = ± 6V		60		dB
d	Distortion	f = 1KHz; V_s = 24V; G_v = 30dB; R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature			145		°C

Fig. 1 - Quiescent current vs. supply voltage

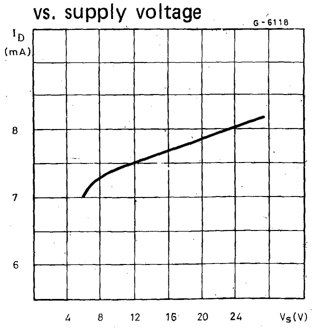


Fig. 2 -- Quiescent drain current vs. temperature

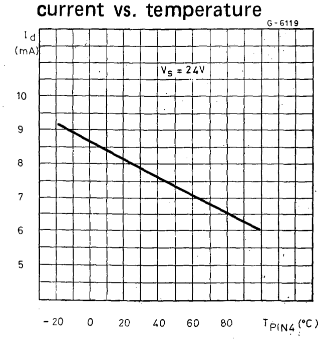


Fig. 3 - Open loop voltage gain

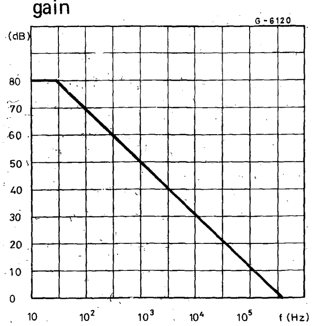


Fig. 4 -- Output voltage swing vs. load current

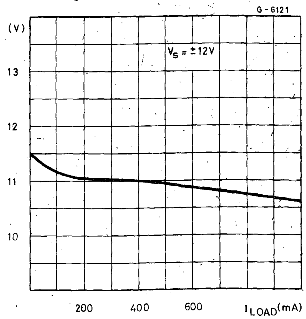


Fig. 5 -- Output voltage swing vs. load current

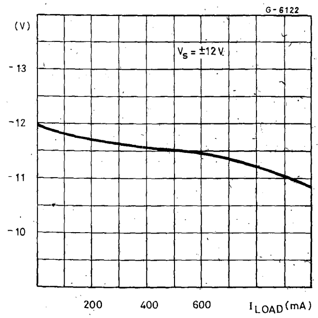


Fig. 6 - Supply voltage rejection vs. frequency

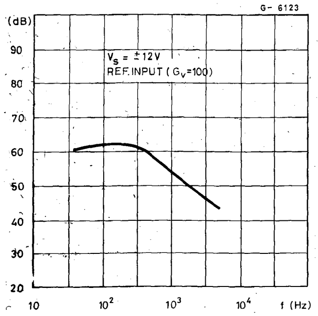


Fig. 7 - Channel separation vs. frequency

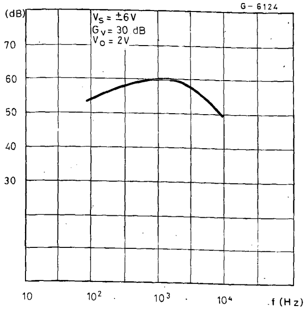
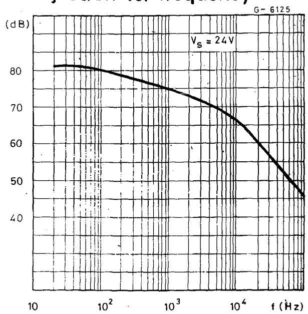


Fig. 8 -- Common mode rejection vs. frequency



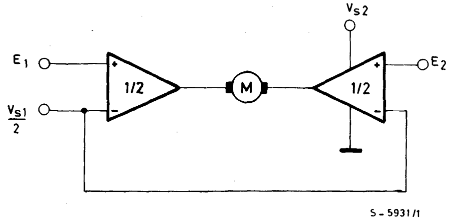
APPLICATION SUGGESTION

NOTE

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2μF + 1Ω series) between outputs and ground or across the load.

Fig. 9 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 10 - Servocontrol for compact-disc

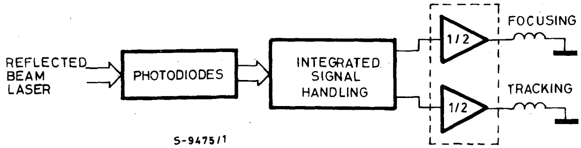


Fig. 11 - Capstan motor control in video recorders

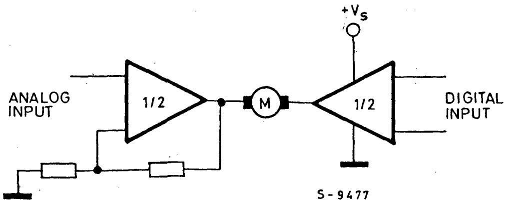
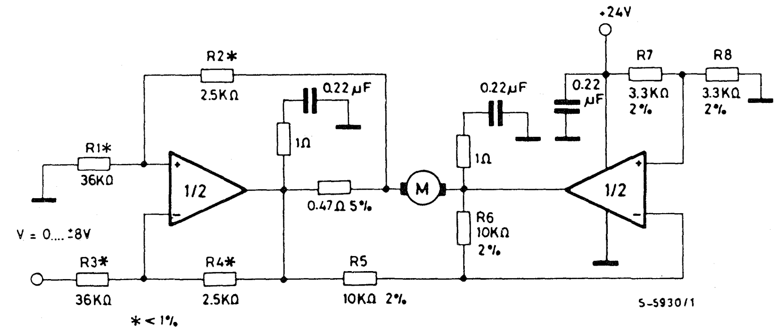


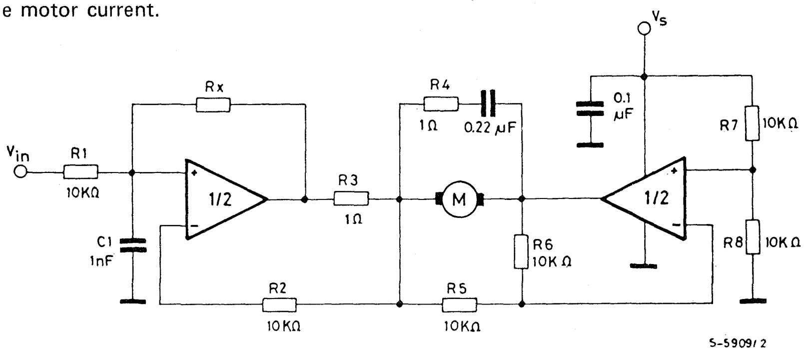
Fig. 12 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 13 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2 \left(V_i - \frac{V_s}{2} \right) + |R_o| . I_M$ where $|R_o| = \frac{2R3 \circ R1}{R_X}$ and I_M is the motor current.



SGS-THOMSON MICROELECTRONICS

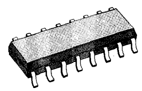
L272D

DUAL POWER OPERATIONAL AMPLIFIER

PRELIMINARY DATA

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272D is a monolithic integrated circuit in SO-16 packages intended for use as power operational amplifier in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc. The high gain and high output power capability provide superior performance wheatever an operational amplifier/power booster combination is required.



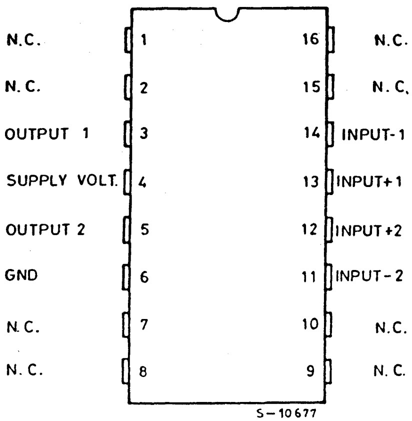
SO-16J

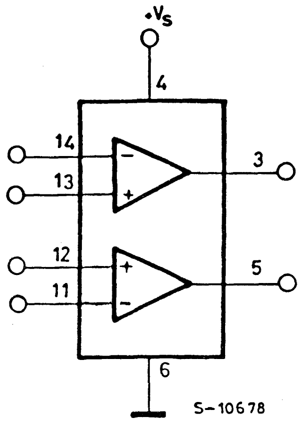
ORDERING NUMBER: L272D

ABSOLUTE MAXIMUM RATINGS

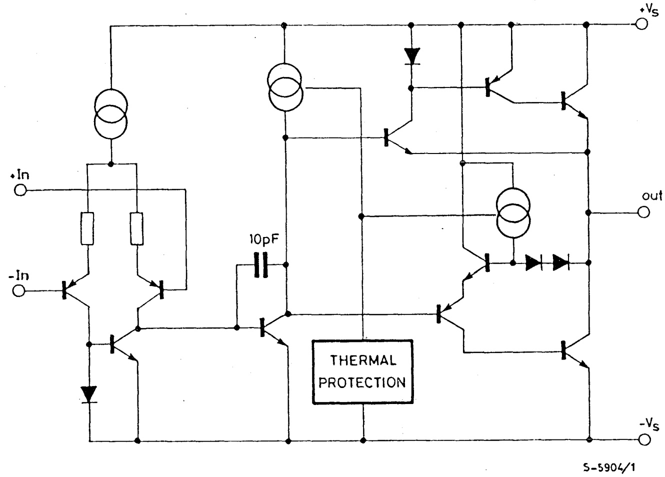
Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at $T_{case} = 90°C$	1.2	W
T_{op}	Operating Temperature Range	-40 to $+85$	°C
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAMS





SCHEMATIC DIAGRAM (one only)



THERMAL DATA

$R_{thj-alumina(*)}$	Thermal resistance junction-alumina	max 50	°C/W

(*) Thermal resistance junctions-pins with the chip soldered on the middle of an alumina supporting substrate measuring 15 x 20 mm; 0.65 mm thickness and infinite heathsink.

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	nA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

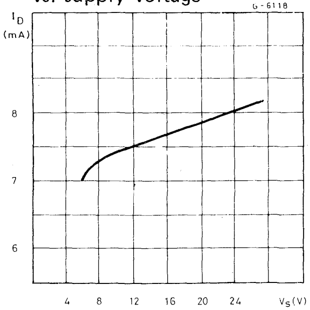


Fig. 2 -- Quiescent drain current vs. temperature

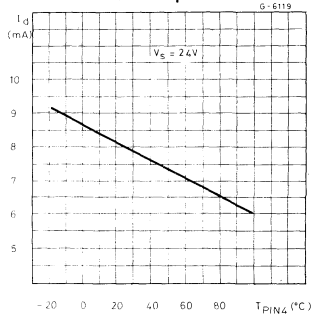


Fig. 3 - Open loop voltage gain

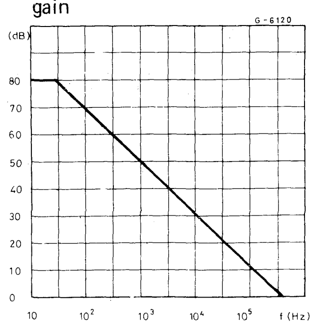


Fig. 4 - Output voltage swing vs. load current

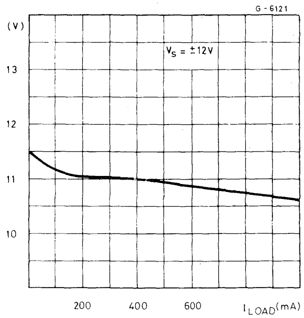


Fig. 5 -- Output voltage swing vs. load current

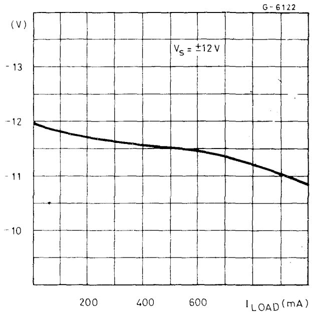


Fig. 6 - Supply voltage rejection vs. frequency

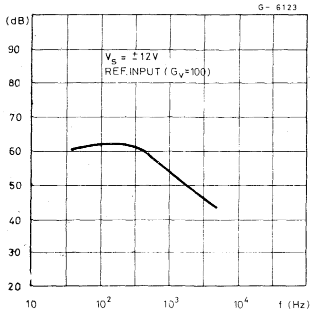


Fig. 7 - Channel separation vs. frequency

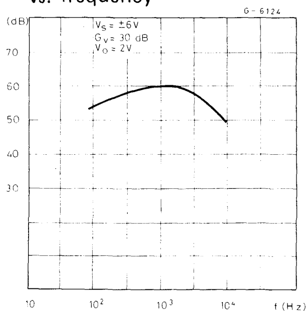
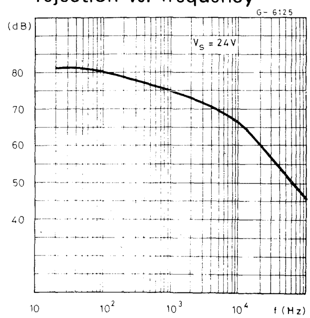


Fig. 8 -- Common mode rejection vs. frequency



LOW DROP DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE
- ESD PROTECTION
- DUMP PROTECTION

The L2720, L2722 and L2724 are monolithic integrated circuits in powerdip, minidip and SIP-9 packages, intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

They are particularly indicated for driving, inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.

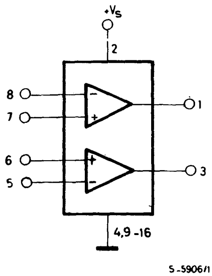
Powerdip (8 + 8) **Minidip Plastic** **SIP-9**

ORDERING NUMBERS:
L2720 L2722 L2724

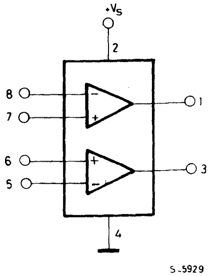
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C **(L2720)**, T_{amb} = 50°C **(L2722)** T_{case} = 75°C **(L2720)** T_{case} = 50°C **(L2724)**	1 5 10	W W W
T_{op}	Operating Temperature	–40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	–40 to 150	°C

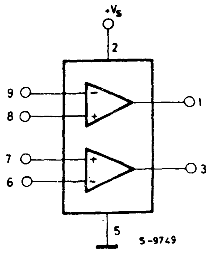
BLOCK DIAGRAMS



L2720

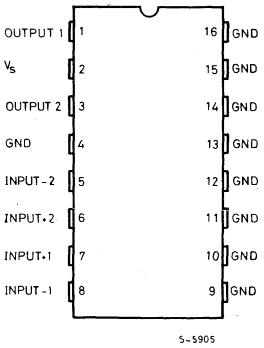


L2722

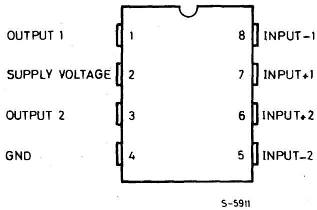


L2724

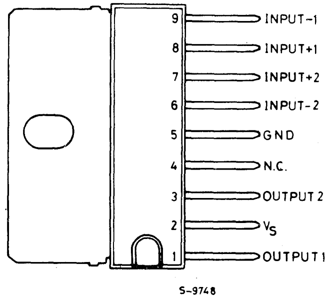
CONNECTION DIAGRAMS
(Top view)



L2720

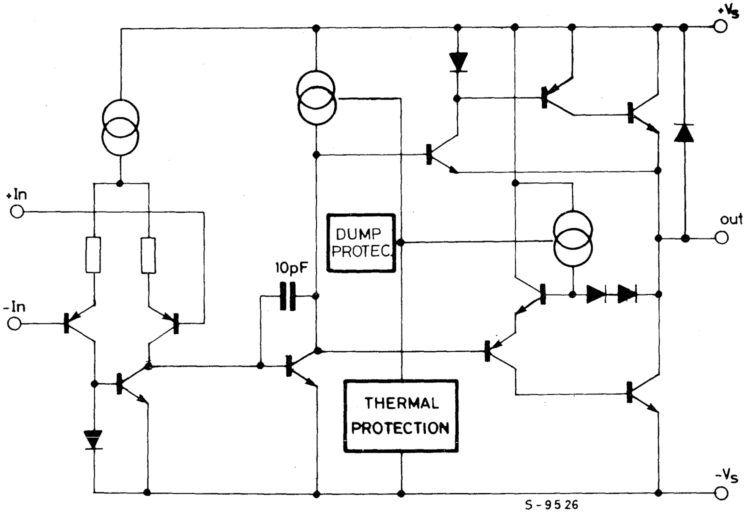


L2722



L2724

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			SIP-9	Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	10°C/W	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-albient	max	70°C/W	70°C/W	100°C/W

* Thermal resistance junction-pin 4.

ELECTRICAL CHARACTERISTICS ($V_s = 24V$, $T_{amb} = 25°C$ unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_O = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input bias current				0.2	1	μA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/μs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_V	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		μV
I_N	Input noise current	B = 22Hz to 22KHz			200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		dB
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

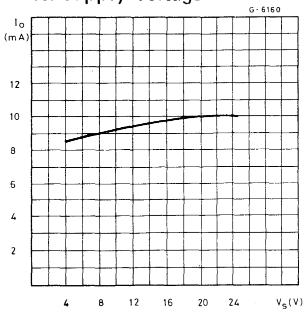


Fig. 2 - Open loop gain vs. frequency

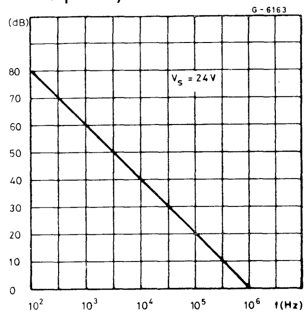


Fig. 3 - Common mode rejection vs. frequency

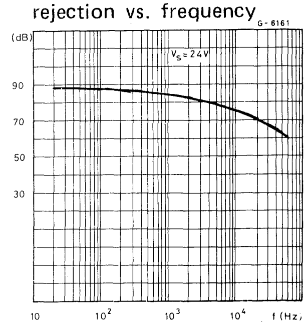


Fig. 4 - Output swing vs. load current ($V_s = \pm$ 5V)

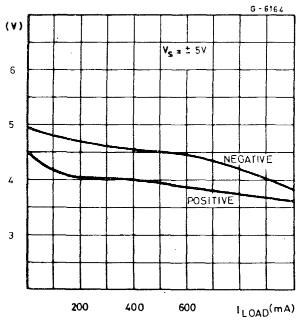


Fig. 5 - Output swing vs. load current ($V_s = \pm$ 12V)

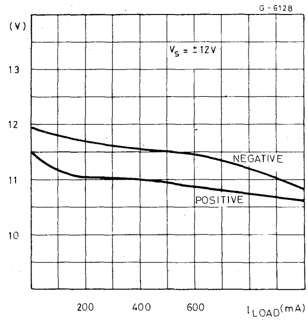


Fig. 6 - Supply voltage rejection vs. frequency

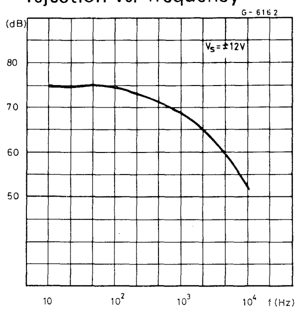
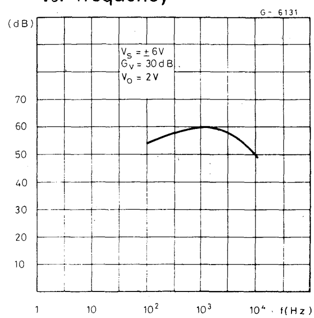


Fig. 7 - Channel separation vs. frequency

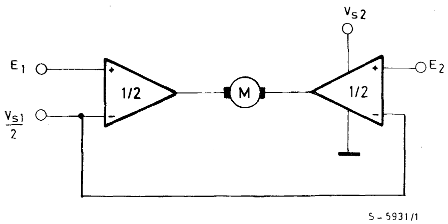


APPLICATION SUGGESTION

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor connected between supply pins and ground;
- boucherot cell (0.1 to 0.2 μF + 1Ω series) between outputs and ground or across the load. With single supply operation, a resistor (1KΩ) between the output and supply pin can be necessary for stability.

Fig. 8 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 9 - Servocontrol for compact-disc

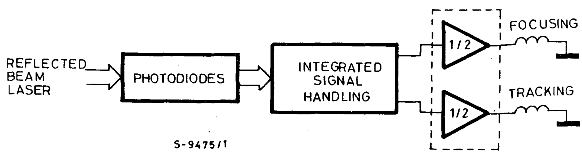


Fig. 10 - Capstan motor control in video recorders

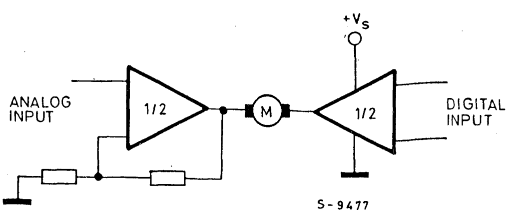
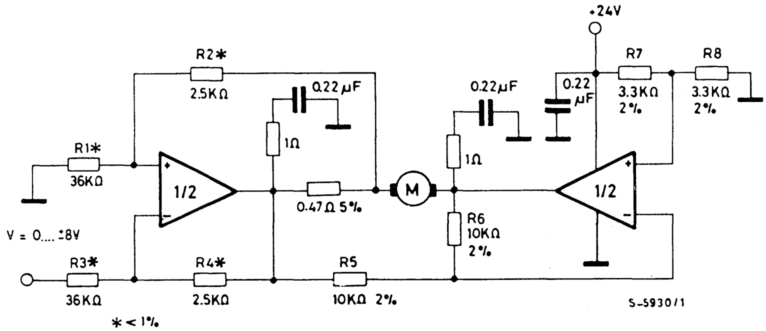


Fig. 11 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 12 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2 (V_i - \frac{V_s}{2}) + |R_o| . I_M$ where $|R_o| = \frac{2R3 \circ R1}{R_X}$ and I_M is the motor current.

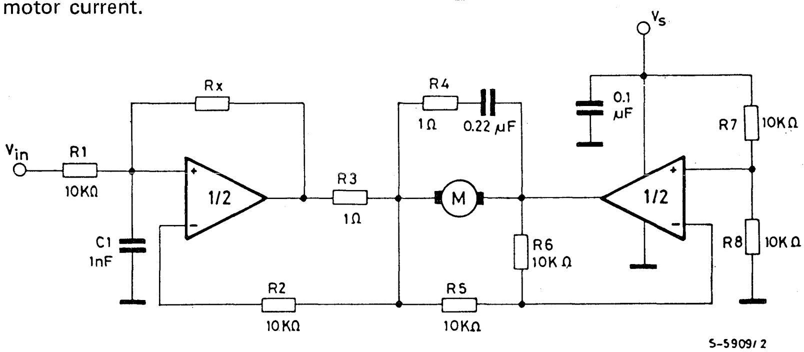
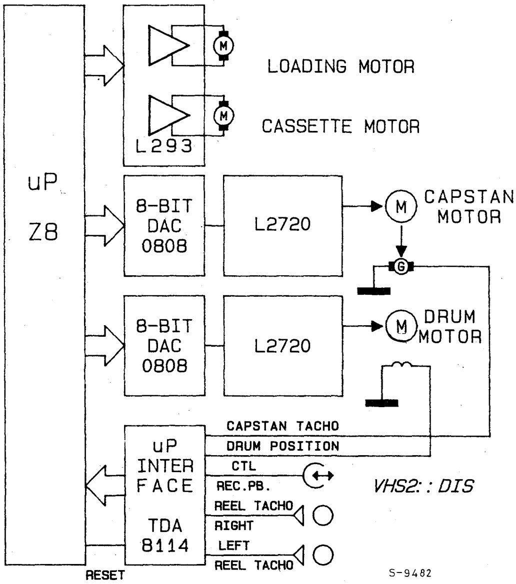


Fig. 13 - VHS-VCR Motor control circuit



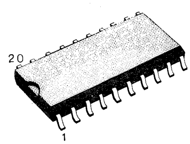
LOW DROP DUAL POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE
- ESD PROTECTION
- DUMP PROTECTION

The L2726 is a monolithic integrated circuit in SO-20 package intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

It is particularly indicated for driving inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



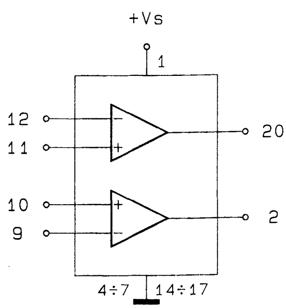
SO-20
(12 + 4 + 4)

ORDER NUMBER: L2726

ABSOLUTE MAXIMUM RATINGS

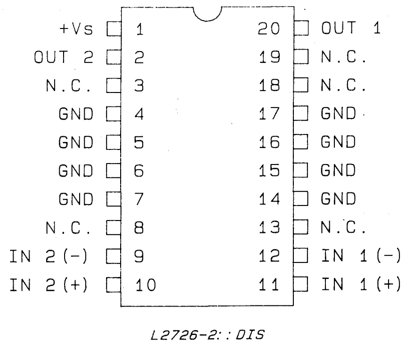
Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at $T_{amb} = 85°C$ $T_{case} = 75°C$	1 5	W W
T_{op}	Operating Temperature	– 40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	– 40 to 150	°C

BLOCK DIAGRAM

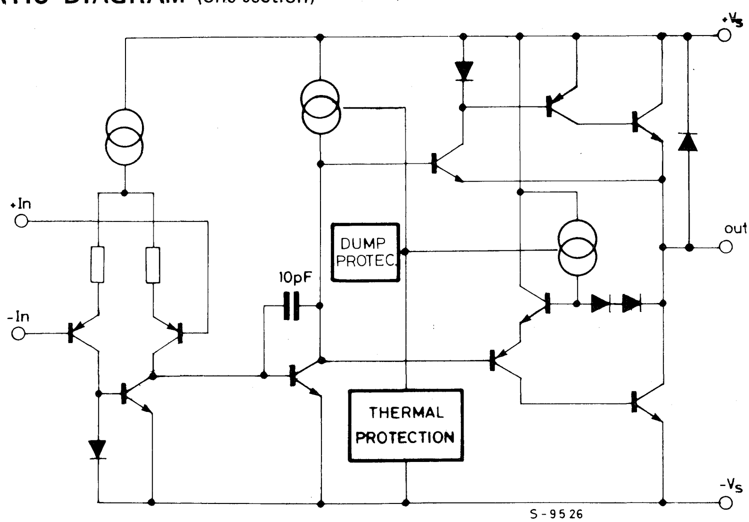


L2726-1::DIS

CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM (one section)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	15.0	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient (*)	max	65	°C/W

(*) With 4 sq. cm copper area heatsink

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_O = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input bias current				0.2	1	μA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/μs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		μV
I_N	Input noise current	B = 22Hz to 22KHz			200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		dB
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

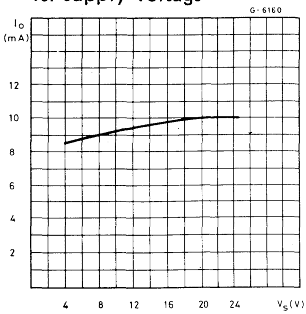


Fig. 2 - Open loop gain vs. frequency

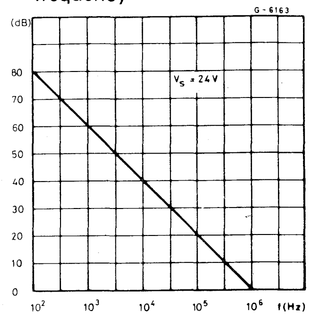


Fig. 3 - Common mode rejection vs. frequency

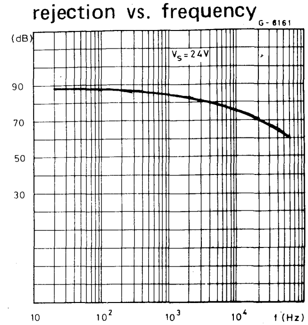


Fig. 4 - Output swing vs. load current (V_s = ± 5V)

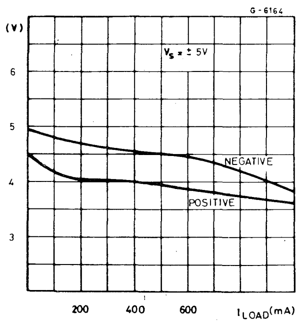


Fig. 5 - Output swing vs. load current (V_s = ± 12V)

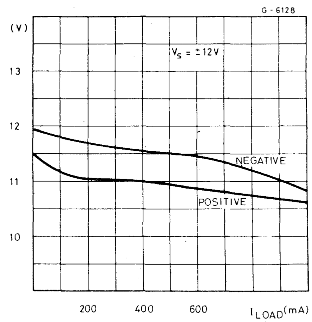


Fig. 6 - Supply voltage rejection vs. frequency

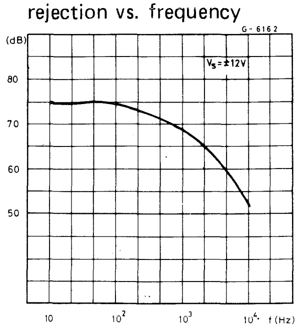
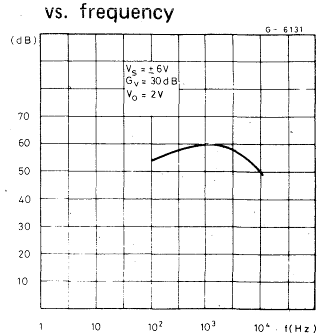


Fig. 7 - Channel separation vs. frequency

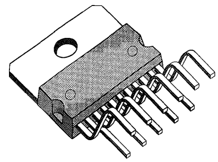


DUAL LOW DROP HIGH POWER OPERATIONAL AMPLIFIER

ADVANCE DATA

- HIGH OUTPUT CURRENT
- VERY LOW SATURATION VOLTAGE
- LOW VOLTAGE OPERATION
- LOW INPUT OFFSET VOLTAGE
- GND COMPATIBLE INPUTS
- ST-BY FUNCTION (LOW CONSUMPTION)
- HIGH APPLICATION FLEXIBILITY

PROTECTIONS:
- VERY INDUCTIVE LOADS
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GROUND
- ESD



Multiwatt-11

ORDERING NUMBER: L2750

DESCRIPTION

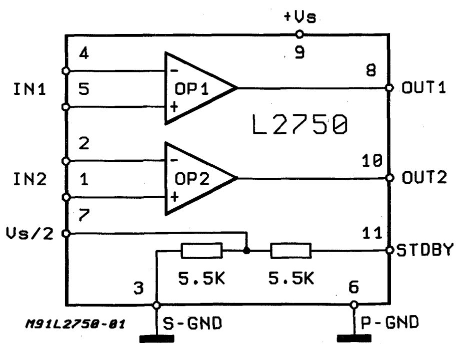
The L2750 is a new technology class AB dual power operational amplifier assembled in Multiwatt 11 package.

Thanks to the fully complementary PNP/NPN output configuration the L2750 can deliver a rail-to-rail output voltage swing even at the highest current.

Additional feature is the very low current Stand-By function.

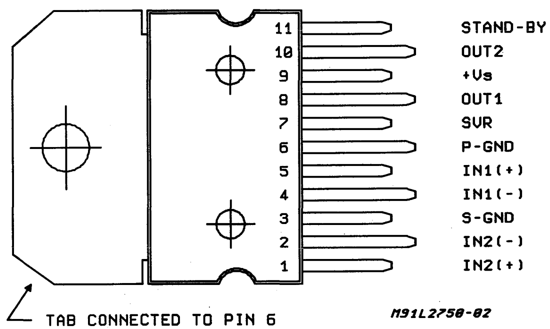
The high application flexibility of the L2750 makes the device suitable for either motor driving/control and audio applications purposes.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{S\ op}$	Operating Supply Voltage	18	V
$V_{S\ max}$	Supply Voltage	28	V
V_{PEAK}	Peak Supply Voltage (t = 50ms)	40	V
V_i	Input Voltage	$V_{S\ op}$	V
V_i	Differential Input Voltage	$V_{S\ op}$	V
I_O	Output Peak Current (non rep. t = 100μs)	5	A
I_O	Output Peak Current (rep. f > 10Hz)	4	A
P_{tot}	Power Dissipation T_{CASE} = 85°C	36	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the operational amplifier with G_V = 24dB; V_S = 14.4V; T_{amb} = 25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		4		18	V
I_d	Total Quiescent Drain Current			30	50	mA
V_{OS}	Input Offset Voltage				5	mV
I_{SB}	ST-BY Current Consumption				50	μA
I_S	Input Bias Current				0.5	μA
I_{OS}	Input Offset Current				50	nA
V_{DROP}	Output Voltage Drop (High)	I_O = 0.5A I_O = 3A		0.25 1.1	0.5 2.5	V V
	Output Voltage Drop (Low)	I_O = 0.5A I_O = 3A		0.25 1	0.5 2	V V
SR	Slew Rate			4		V/μs
B	Gain Bandwidth Prod			10		MHz
G_V	Open Loop Voltage Gain	f = 1KHz		85		dB
R_{IN}	Input Resistance			150		MΩ
E_{IN}	Input Noise Voltage	R_s = 0 to 10KΩ f = 22Hz to 22KHz		3		μV
CMRR	Common Mode Rejection Ratio		75	90		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SVR	Supply Voltage Rejection	$R_s = 0$ f = 100Hz	75	90		dB
C_T	Crosstalk	f = 1KHz to 10KHz		80		dB

APPLICATION SUGGESTION

The high flexibility makes the L2750 suitable for a wide range of applications.

Motor Controller

The device can be utilized as a motor controller. Fig.1 represents a bidirectional DC motor control suitable for logic driving. In these kinds of application it is possible to take advantage of the high current capability of the L2750 for driving several types of low impedance motors in a broad range of applications. Moreover the low drop allows high start up currents even at lowest supply voltage.

Audio Applications

Another typical utilization of the L2750 concerns the audio field, as follows:

1) DRIVER FOR BOOSTER : The remarkably low distortion and noise makes the device proper to be used as high quality driver for main amplifiers (i.e. car radio boosters). An example is shown by Fig. 5, where the gain is set to 24 dB (see also the relevant characteristics).

2) CAR RADIO BOOSTER WITH DIFFERENTIAL INPUT : Fig. 10 shows an example of car radio booster, with a gain of 30 dB, that is specially recommended for active loudspeakers. Among its main feature is the differential input and subsequent high noise suppression. The typical output power delivered into a 4Ω load is 24W (V_S = 14.4V; d =10%), as shown by the characteristics enclosed.

Figure 1

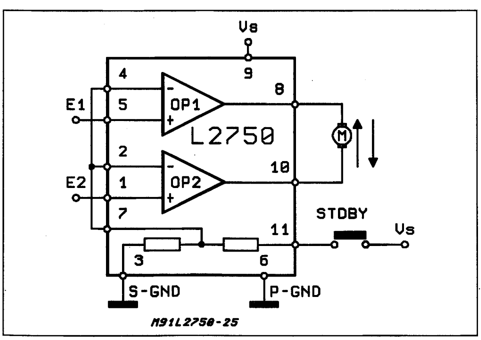


Figure 2: Low Drop Voltage vs. Output Current

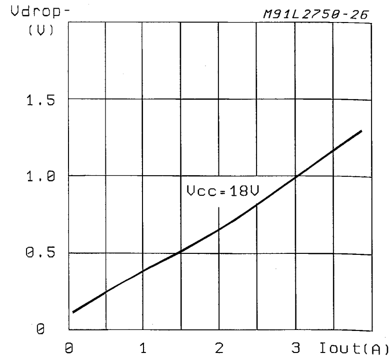


Figure 3: High Drop Voltage vs. Output Current

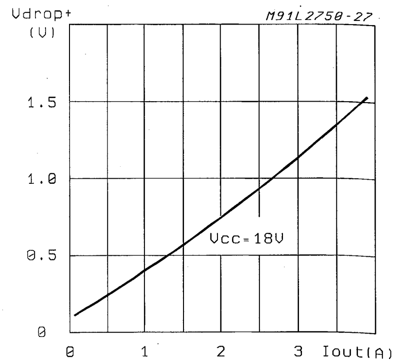


Figure 4: Open Loop Gain vs. Phase Response

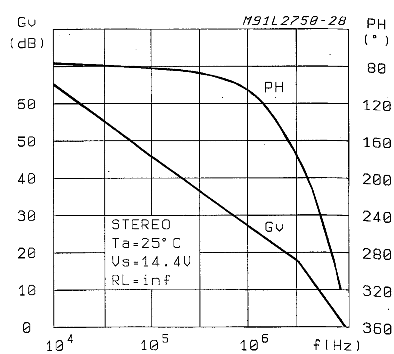


Figure 5: Stereo Audio Amplifier Application Circuit

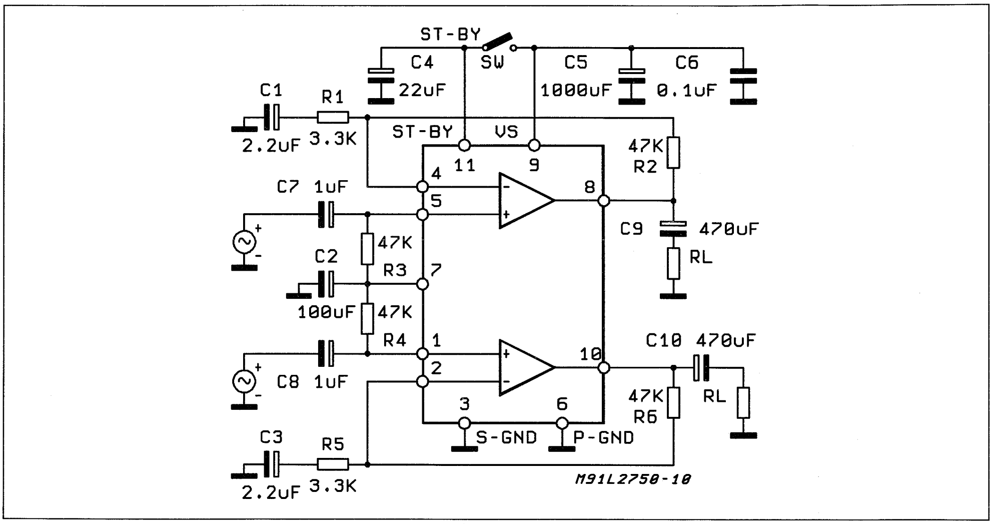
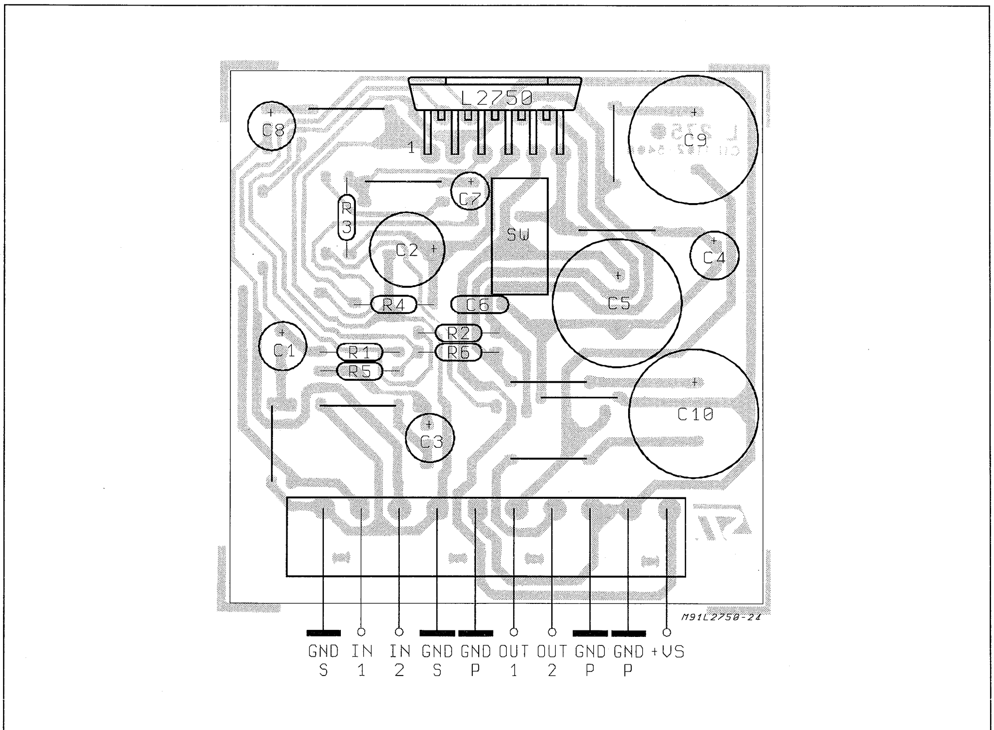


Figure 6: P.C. Board and Components Layout of the Circuit of Figure 5 (1:1 scale)



AUDIO STEREO APPLICATION CIRCUIT OF FIGURE 5

Figure 7: Quiescent Drain Current vs. Supply Voltage

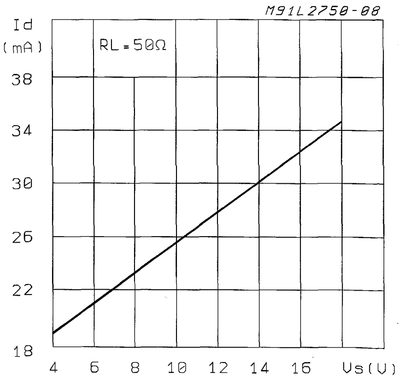


Figure 8: Distortion vs. Output Voltage

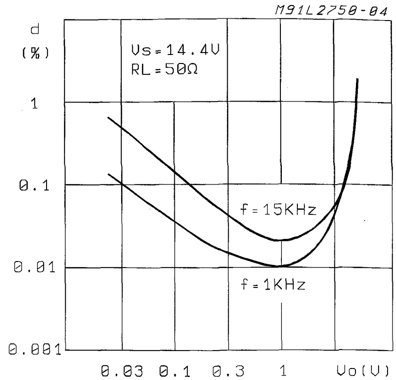


Figure 9: Distortion vs. Frequency

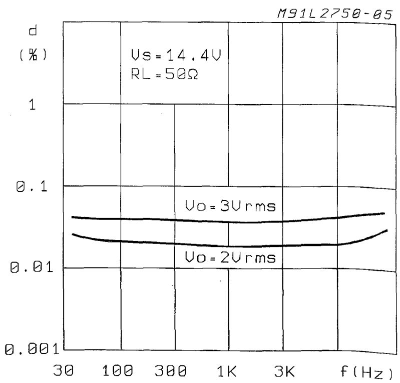


Figure 10: Cross-Talk vs Frequency

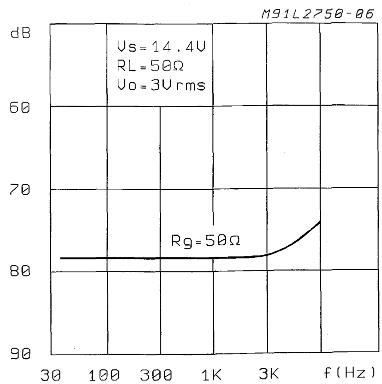


Figure 11: Supply Voltage Rejection vs. Frequency

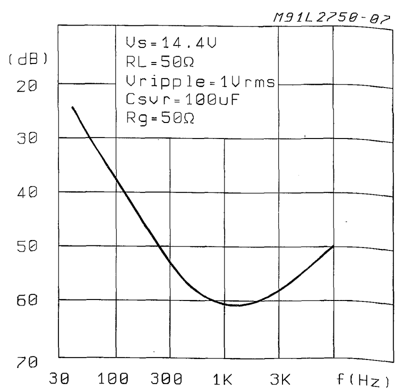


Figure 12: E_N Input vs. R_g

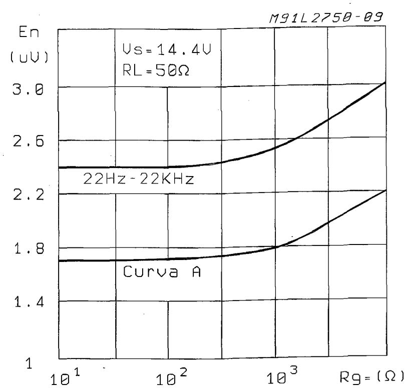


Figure 13: Bridge Power Amplifier with Balanced Input Application Circuit

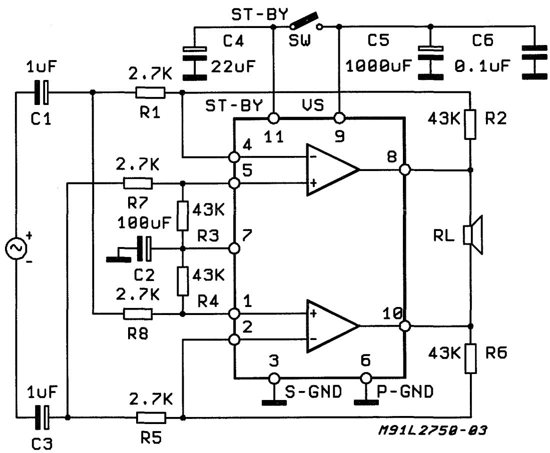
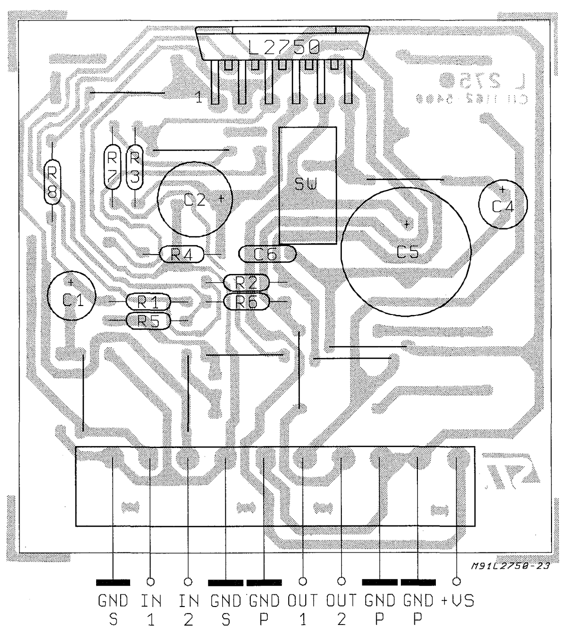


Figure 14: P.C. Board and Component Layout of the Circuit of Figure 13 (1:1 scale)



BRIDGE AUDIO APPLICATION CIRCUIT OF FIGURE 13

Figure 15: Quiescent Drain Current vs. Supply Voltage

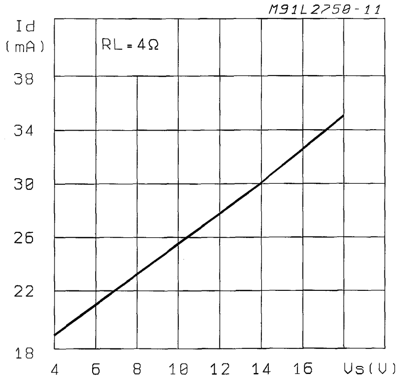


Figure 16: Noise vs. Rs

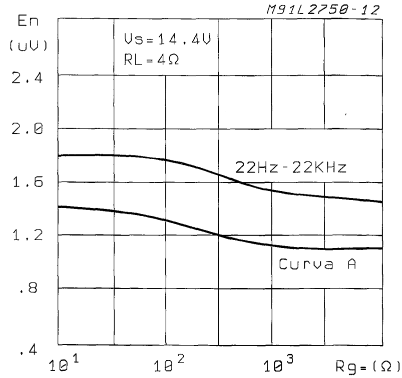


Figure 17: Output Power vs. Supply Voltage

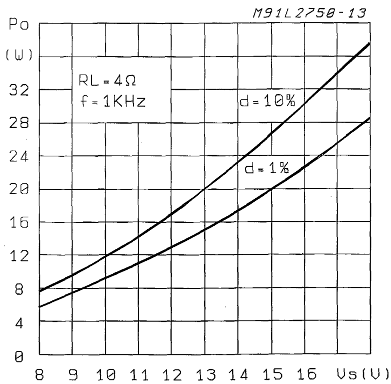


Figure 18: Output Power vs Supply Voltage

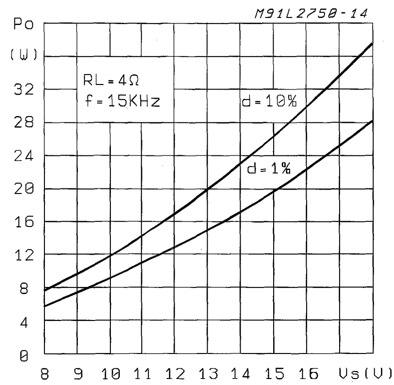


Figure 19: Distortion vs. Output Power

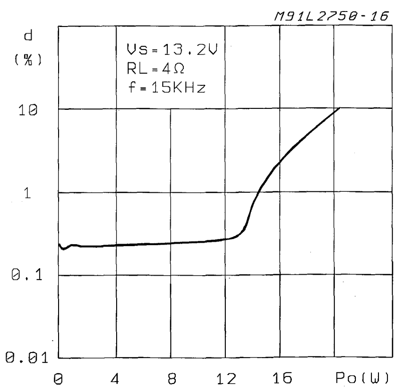


Figure 20: Distortion vs. Output Power

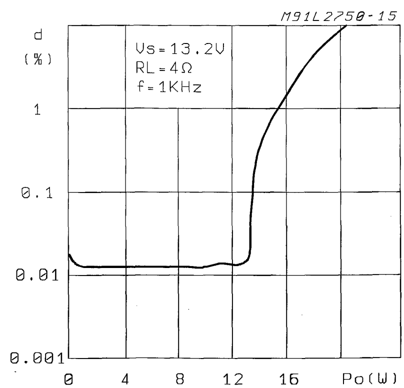


Figure 21: Distortion vs. Output Power

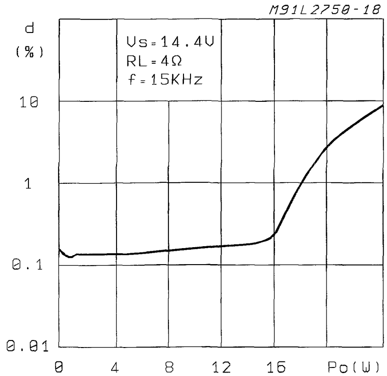


Figure 22: Distortion vs. Output Power

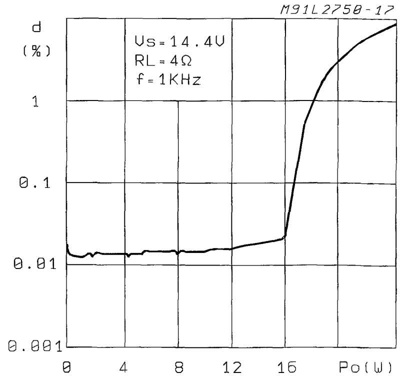


Figure 23: Distortion vs. Frequency

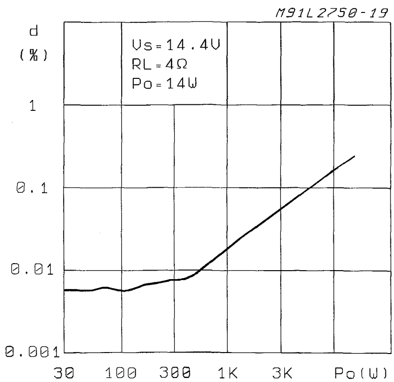


Figure 24: Supply Voltage Rejection vs. Frequency

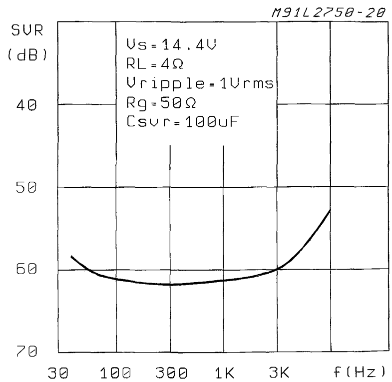


Figure 25: Total Power Dissipation and Efficiency vs. Output Power

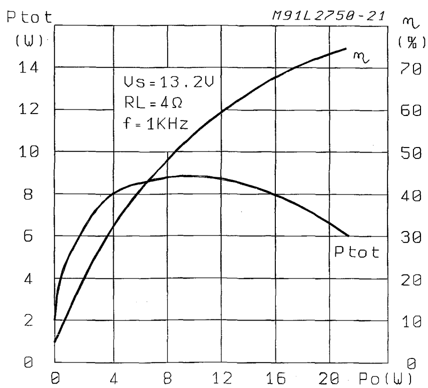
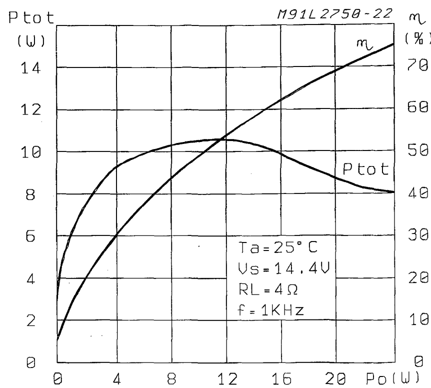


Figure 26: Total Power Dissipation and Efficiency vs. Output Power



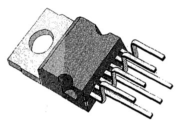
DUAL 5V REGULATOR WITH RESET

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 400mA
  I_{02} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4901A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



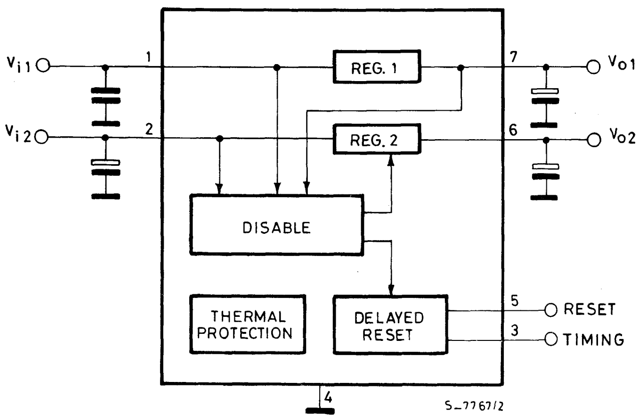
Heptawatt

ORDERING NUMBER: L4901A

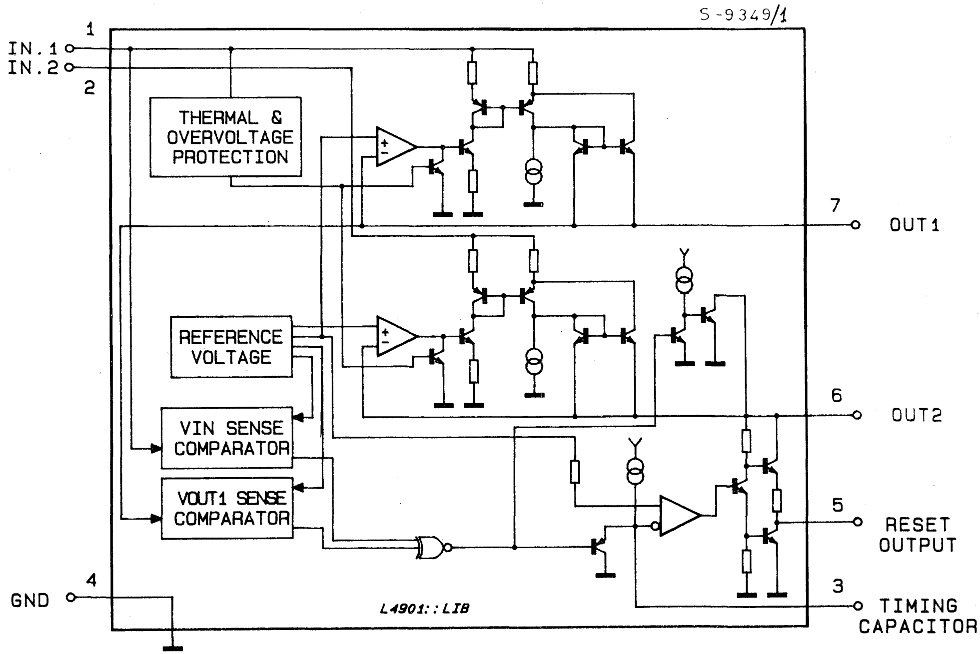
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

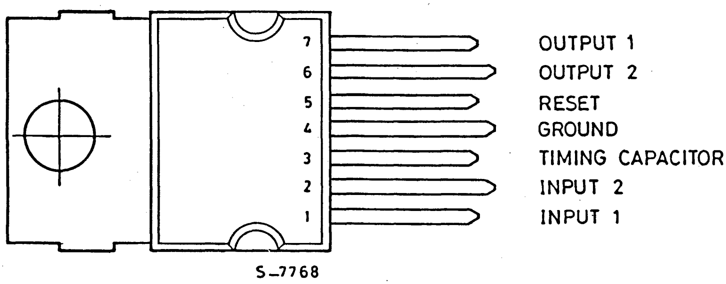
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



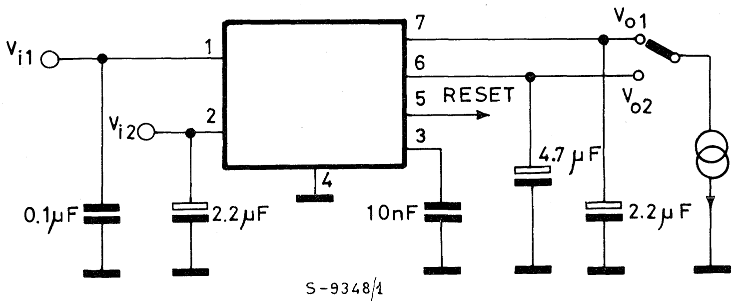
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 400mA regulator input.
2	INPUT 2	400mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10µA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A} \right)$; t_{RD} (ms) $= C_t$ (nF)
6	OUTPUT 2	5V - 400mA regulator output. Enabled if V_O $1 > V_{RT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 400mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_{IN1} = V_{IN2} = 14,4V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	$I_{02} = -5mA$		0.1		V
I_{01}	Output current 1	$\Delta V_{01} = -100mV$	400			mA
I_{L01}	Leakage output 1 current	$V_{IN} = 0$ $V_{01} \leqslant 3V$			1	μA
I_{02}	Output current 2	$\Delta V_{02} = -100mV$	400			mA
V_{i01}	Output 1 dropout voltage (*)	$I_{01} = 10mA$ $I_{01} = 100mA$ $I_{01} = 300mA$		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	$7V < V_{IN} < 18V$ $I_{01} = 5mA$		5	50	mV
ΔV_{02}	Line regulation 2	$I_{02} = 5mA$		5	50	mV
ΔV_{01}	Load regulation 1	$5mA < I_{01} < 400mA$		50	100	mV
ΔV_{02}	Load regulation 2	$5mA < I_{02} < 400mA$		50	100	mV
I_Q	Quiescent current	$0 < V_{IN} < 13V$ $7V < V_{IN} < 13V$ $I_{02} = I_{01} \leqslant 5mA$		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	$6.3V < V_{IN1} < 13V$ $V_{IN2} = 0$ $I_{01} \leqslant 5mA$ $I_{02} = 0$		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500µA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	µs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for µP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4901A makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

– an input overvoltage
– an overload on the output 1 ($V_{01} < V_{RT}$);
– a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

– 5V internal reference without voltage divider between the output and the error comparator;
– very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

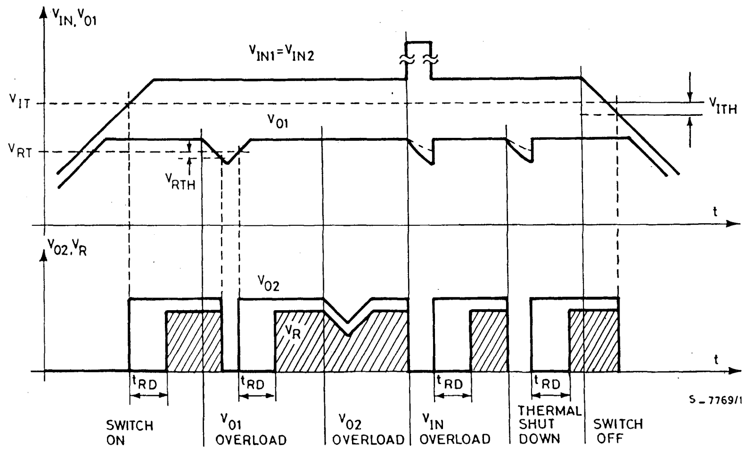
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a µP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4901A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS µP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

The L4901A is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shown in fig. 5 the reset output is used both to disable the µP and, through the address decoder M74HC138, to ensure that the RAMS are disabled as soon as the main supply starts to fall.

Another interesting application of the L4901A is in µP system with shadow memories. (see fig. 6)

When the input voltage goes below V_{IT}, the reset output enables the execution of a routine that saves the machine's state in the shadow RAM (xicor x 2201 for example).

Thanks to the low consumption of the Reg. 1 a 680µF capacitor on its input is sufficient to provide enough energy to complete the operation. The diode on the input guarantees the supply of the equipment even if a short circuit on V_i occurs.

APPLICATION SUGGESTION (continued)

Fig. 2

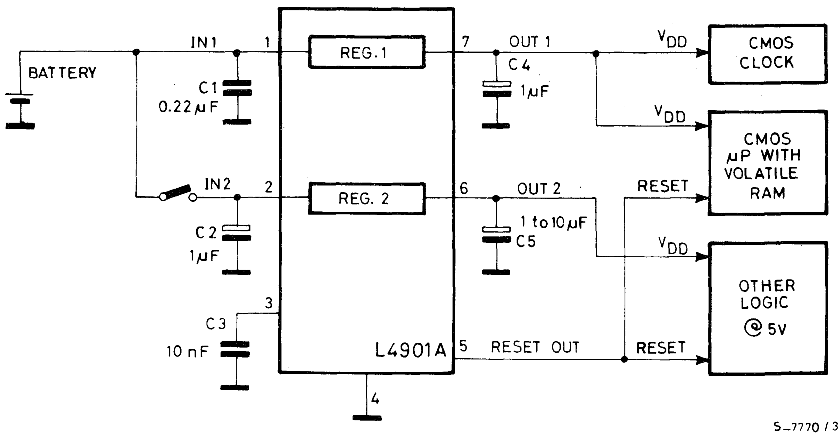
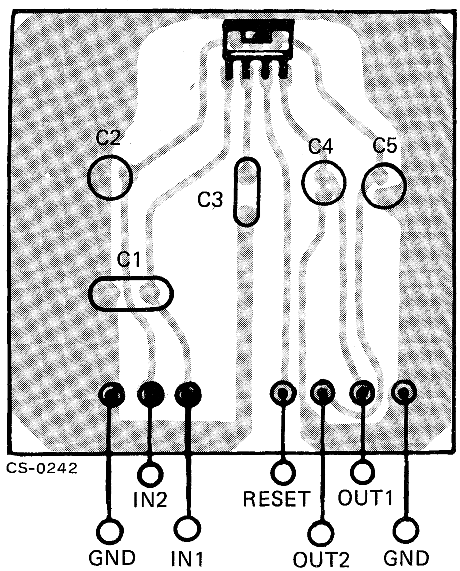


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

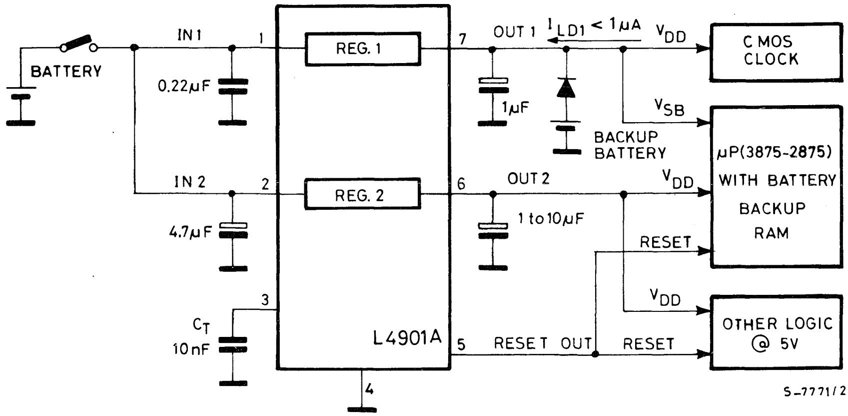
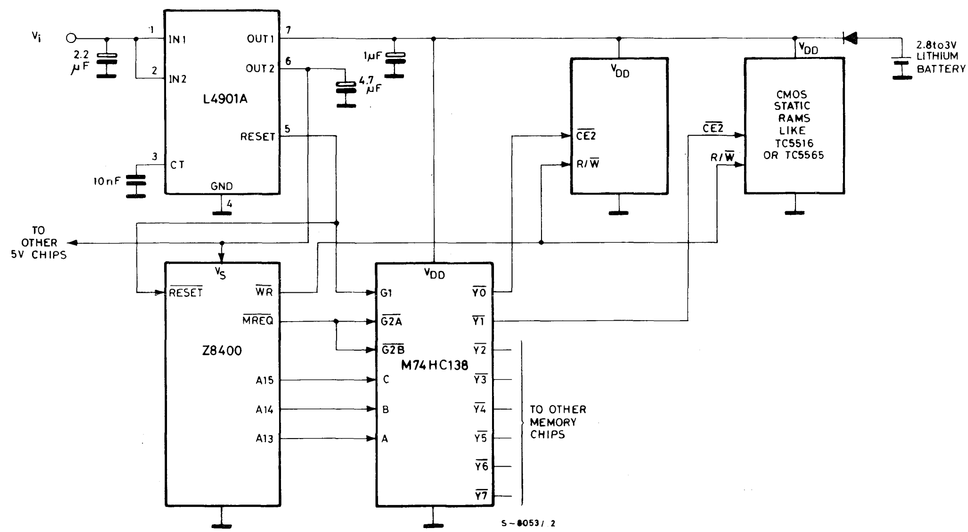


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6

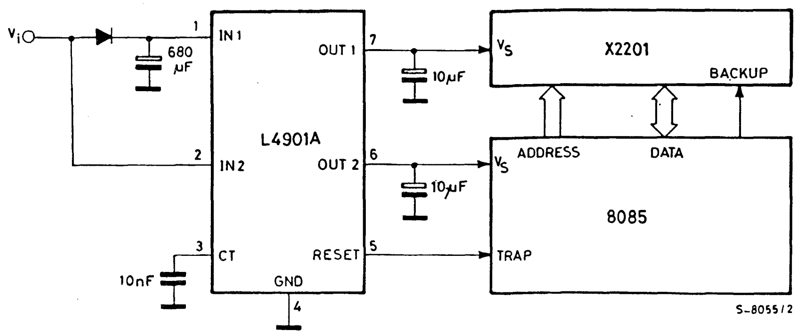


Fig. 7 - Quiescent current (Reg. 1) vs. output current

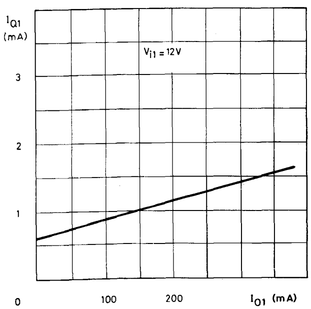


Fig. 8 - Quiescent current (Reg. 1) vs. input voltage

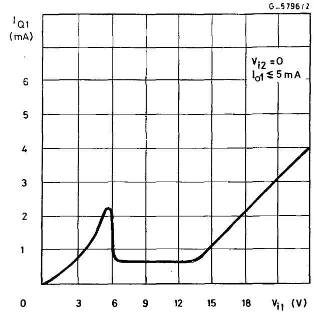


Fig. 9 - Total quiescent current vs. input voltage

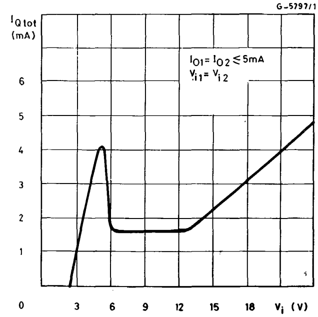


Fig. 10 - Regulator 1 output current and short circuit current vs. input voltage

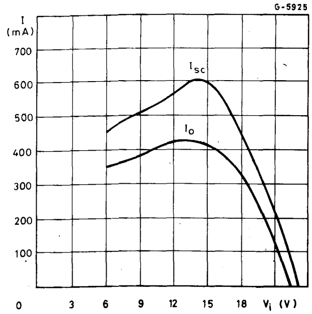


Fig. 11 - Regulator 2 output current and short circuit current vs. input voltage

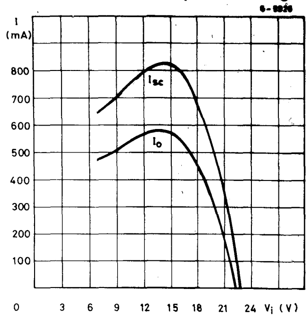
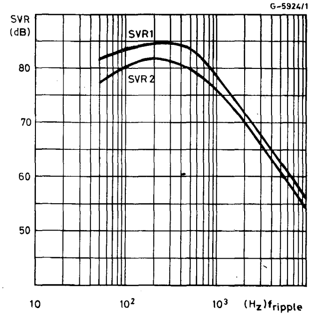


Fig. 12 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



SGS-THOMSON MICROELECTRONICS

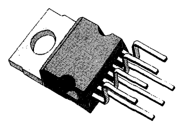
L4902A

DUAL 5V REGULATOR WITH RESET AND DISABLE

PRELIMINARY DATA

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: I_{01} = 300mA
  I_{02} = 300mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- RESET OUTPUT NORMALLY HIGH
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4902A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.
Reset and data save functions and remote switch on/off control can be realized.



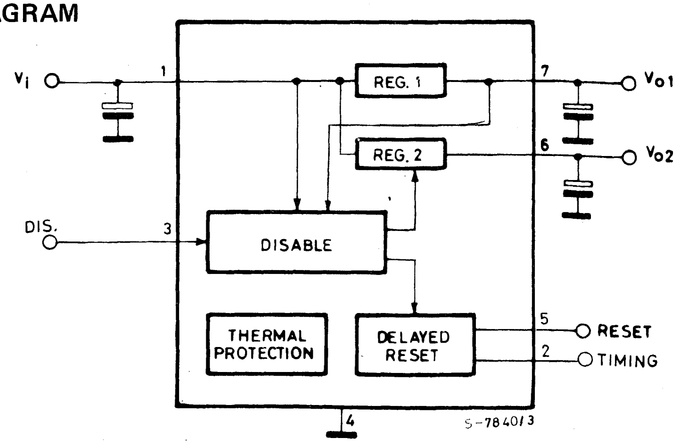
Heptawatt

ORDERING NUMBER: L4902A

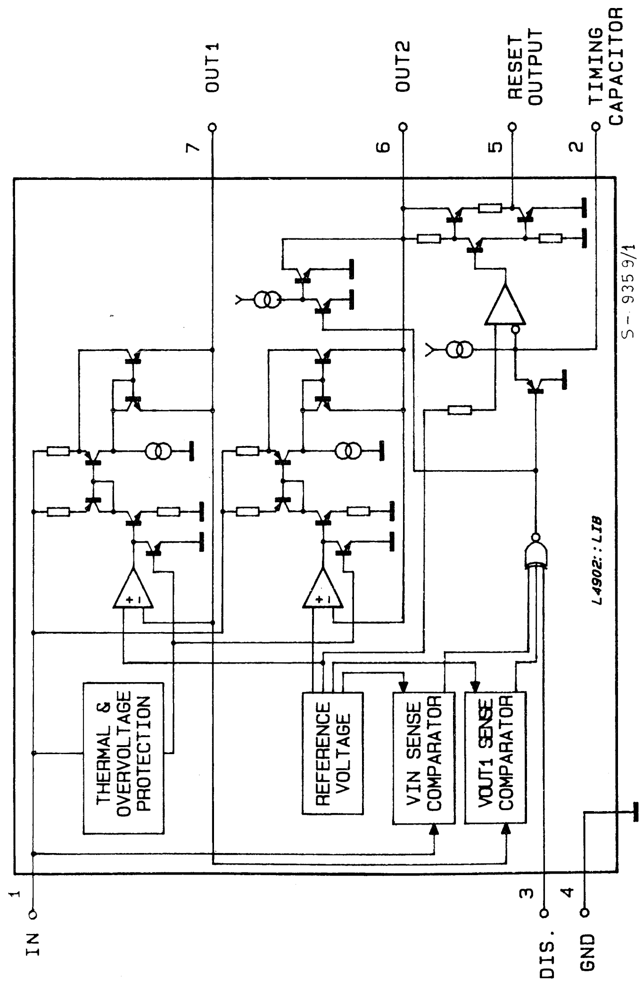
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

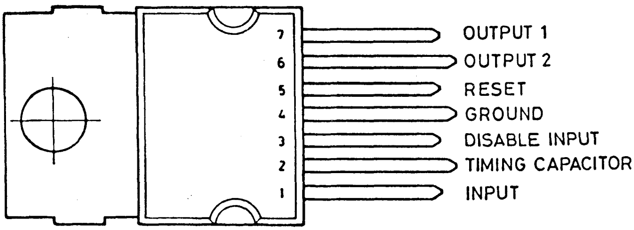
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



S-7841

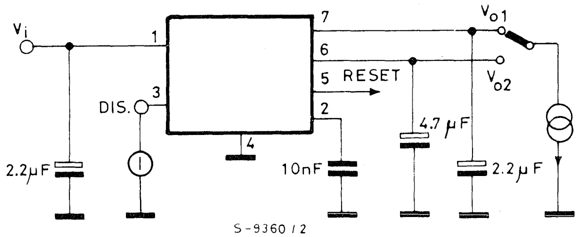
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Regulators common input.
2	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
3	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
4	GND	Common ground.
5	RESET OUTPUT	When pin 2 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \; (\frac{5V}{10\mu A})$; t_{RD} (ms) $= C_t$ (nF).
6	OUTPUT 2	5V - 300mA regulator output. Enabled if $V_O 1 > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 300mA. Low leakage (in switch-OFF condition) output.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				24	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max.	ΔV_{01} = -100mV	300			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq 3V$			1	μA
I_{02}	Output current 2 max.	ΔV_{02} = -100mV	300			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{iTH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 24V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 300mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 300mA		50	80	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -1mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-150 -30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R=0.5V I_o = 100mA	50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4902A makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with common inputs plus a reset output for the data save function and a Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:
- a high level ($> V_{DT}$) is applied on pin 3;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:
- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

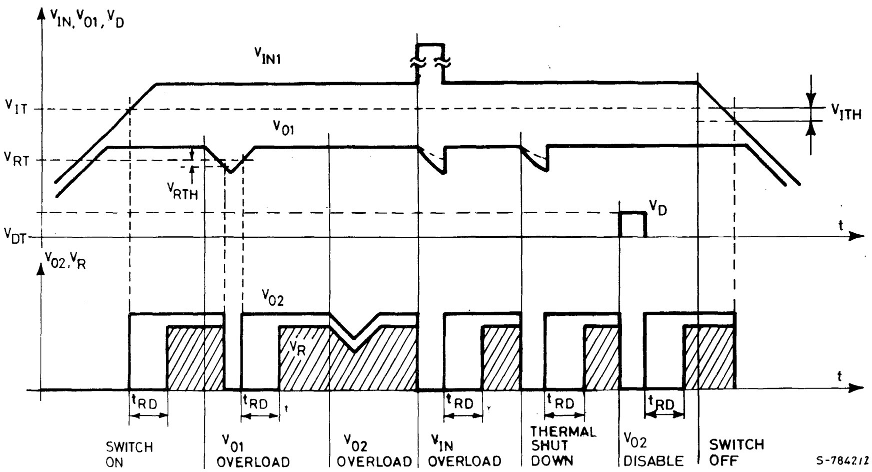
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



APPLICATION SUGGESTION

Fig. 2 illustrate how the L4902A's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Another application for the L4902A is supplying a shadow-ram microcomputer chip (SGS M38SH72 for exemple) where a fast NV memory is backed up on chip by a EEPROM when a low level on the reset output occurs.

By adding two CMOS-SCHMIDT-TRIGGER and few external components, also a watch dog function may be realized (see fig. 5). During normal operation the microsystem supplies a periodical pulse waveform; if an anomalous condition occours (in the program or in the system), the pulses will be absent and the disable input will be activated after a settling time determined by R1 C1. In this condition all the circuitry connected to V_{02} will be disabled, the system will be restarted with a new reset front.

The disable of V_{02} prevent spurious operation during microprocessor malfunctioning.

APPLICATION SUGGESTION (continued)

Fig. 2

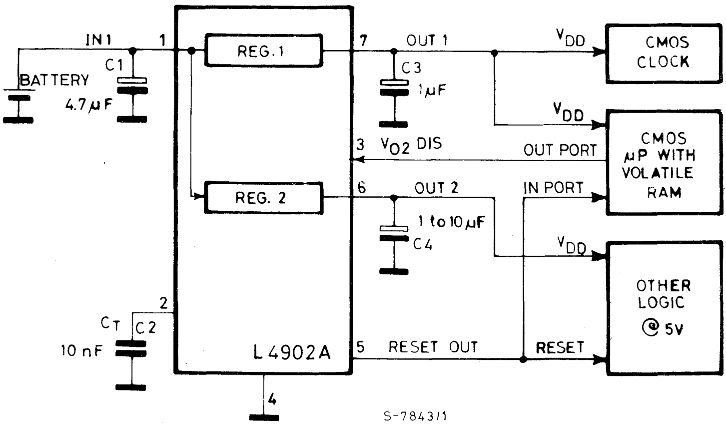
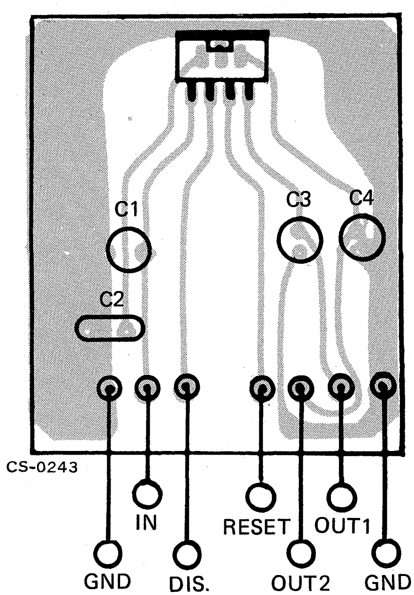


Fig. 3 - P.C. board and component layout of the circuit of Fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

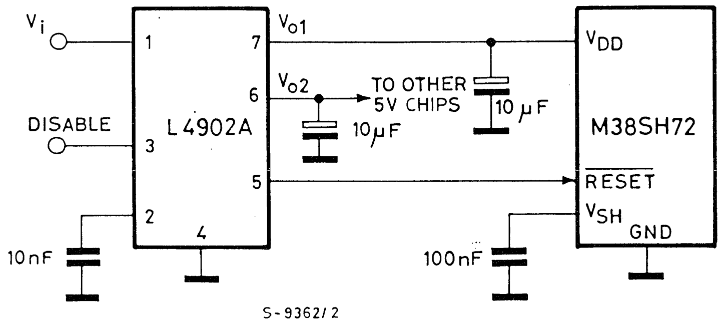
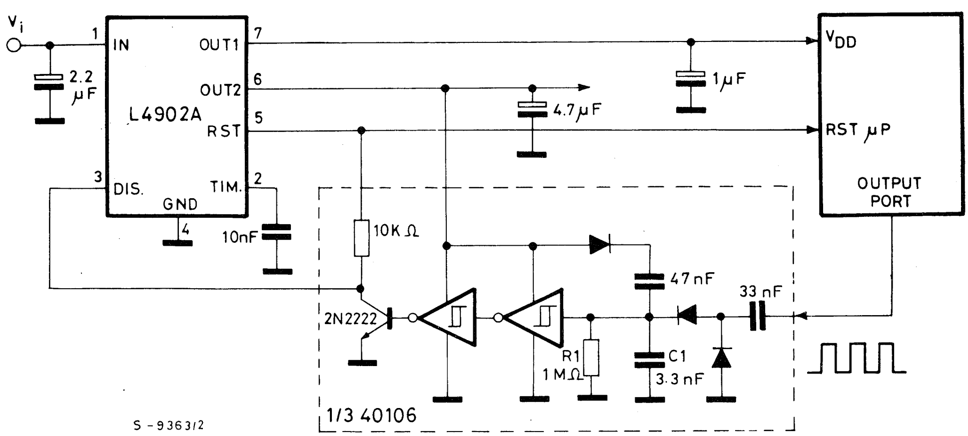


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6 - Quiescent current vs. output current

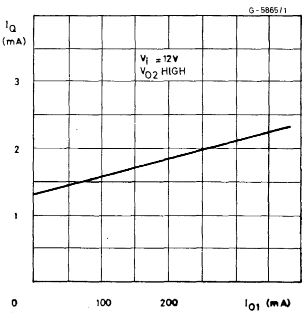


Fig. 7 - Quiescent current vs. input voltage

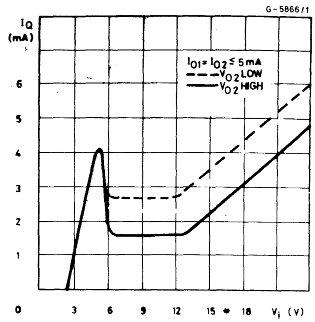
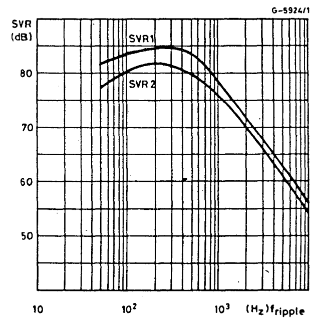


Fig. 8 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



SGS-THOMSON MICROELECTRONICS

L4903

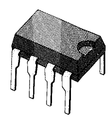
DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 50mA
  I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4903 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset, data save functions and remote switch on/off control can be realized.



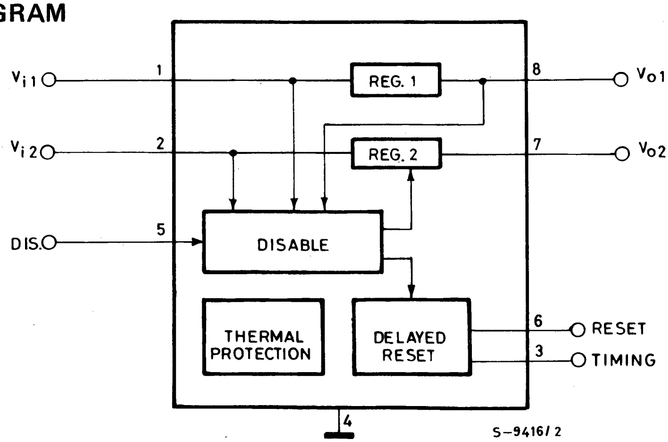
Minidip Plastic

ORDERING NUMBER: L4903

ABSOLUTE MAXIMUM RATINGS

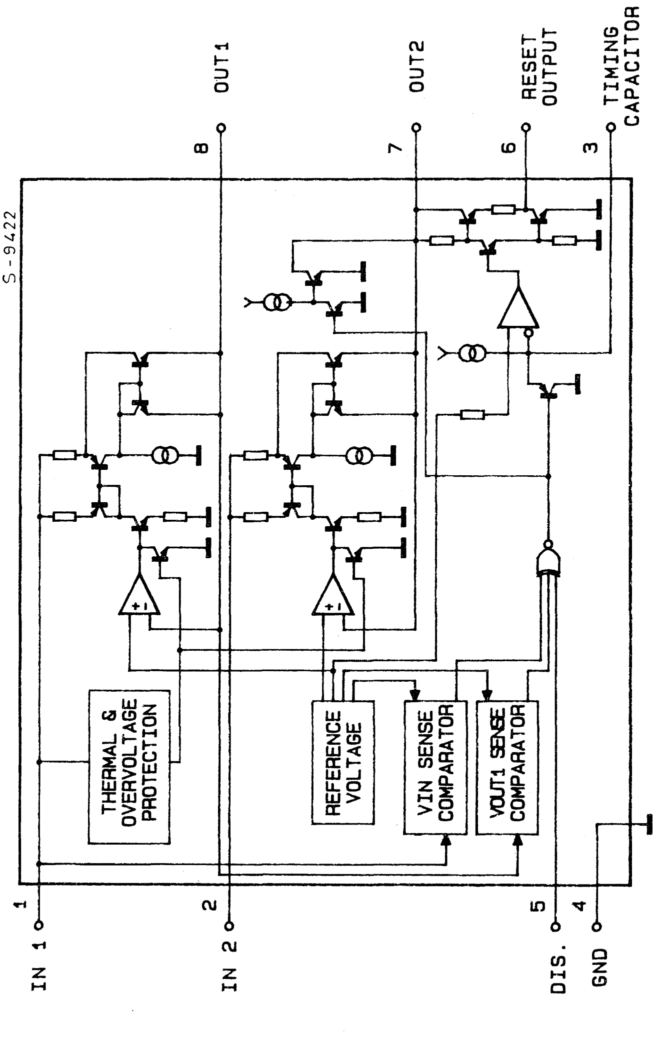
V_{IN}	DC input voltage	24	V
V_t	Transient input overvoltage (t = 40 ms)	60	V
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM

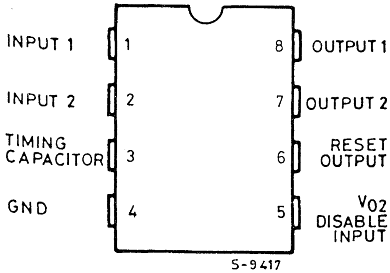


June 1988

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



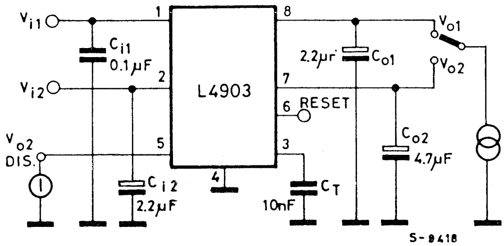
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disables output Reg. 2.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) $= C_t$ (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if V_O 1 $> V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

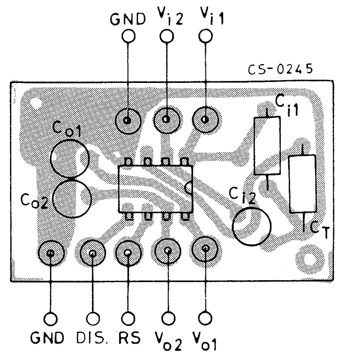
THERMAL DATA

$R_{th\ j\text{-}pin}$	Thermal resistance junction-pin 4	max	70	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb}= 25°C unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max. (*)	ΔV_{01} = -100mV	50			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	μA
I_{02}	Output current 2 max. (*)	ΔV_{02} = -100mV	100			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	V_{IN1} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 I_{01} < 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.4	4.7	V_{02}-0.2	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-150 30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	50	84		dB
SVR2	Supply voltage rejection	I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current conditions.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4903 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function and Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02} and V_R) switches on and the reset output (V_R) goes low after a programmable time T_{RD} (timing capacitor).

V_{02} is switched at low level and V_R at high level when one of the following conditions occurs:

- a high level (> V_{DT}) is applied on pin 5;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

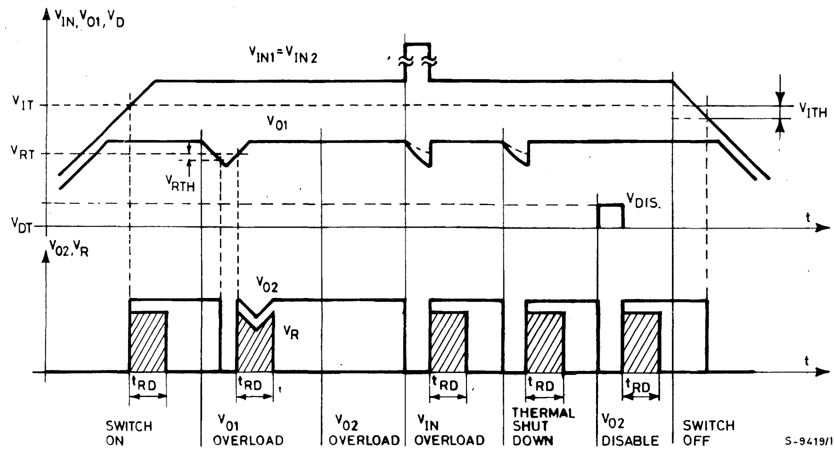
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



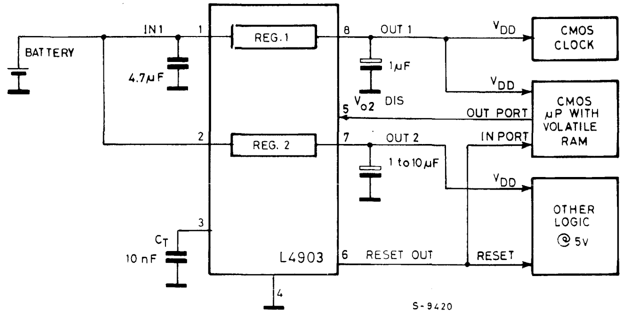
APPLICATION SUGGESTION

Fig. 2 illustrates how the L4903's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Fig. 2



APPLICATION SUGGESTIONS (continued)

Fig. 3 - Quiescent current (Reg. 1) vs. output current

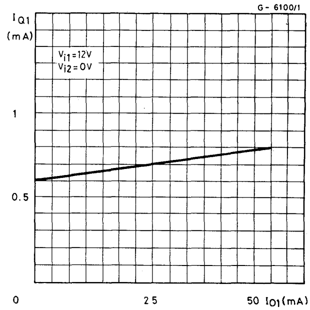


Fig. 4 - Quiescent current (Reg. 1) vs. input voltage

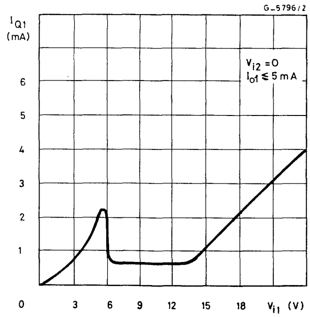


Fig. 5 -- Total quiescent current vs. input voltage

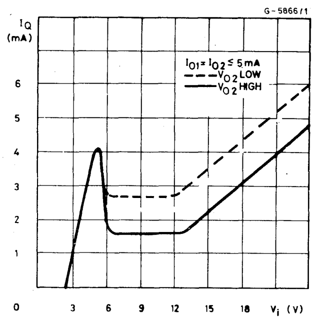
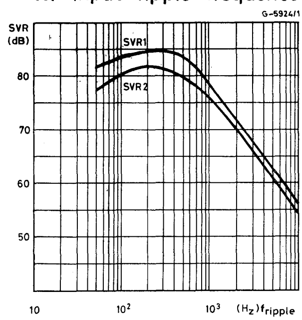


Fig. 6 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



SGS-THOMSON MICROELECTRONICS

L4904A

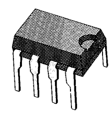
DUAL 5V REGULATOR WITH RESET

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 50mA, I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4904A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



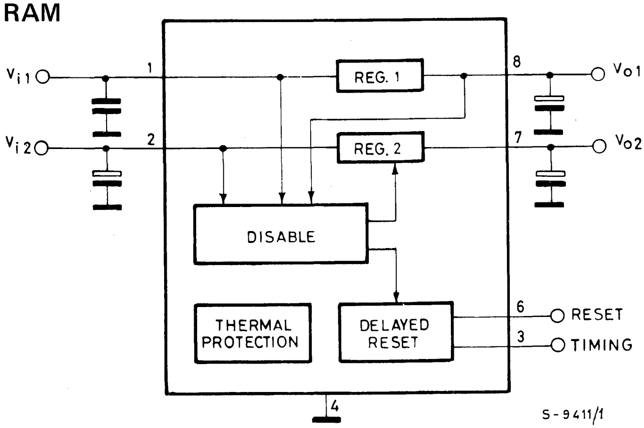
Minidip Plastic

ORDERING NUMBER: L4904A

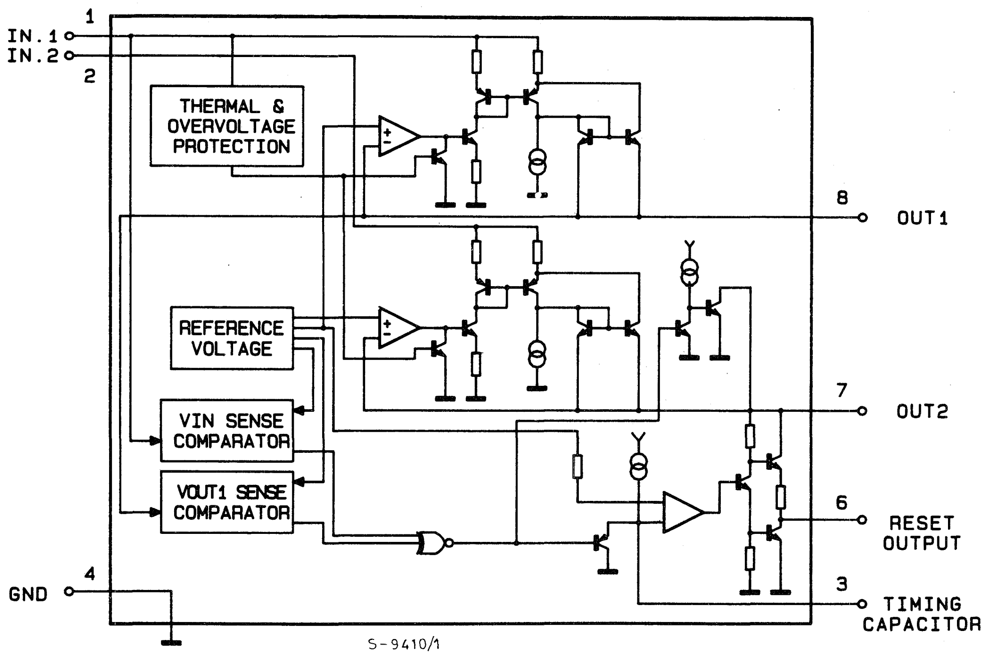
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_j	Storage and junction temperature	-40 to 150	°C

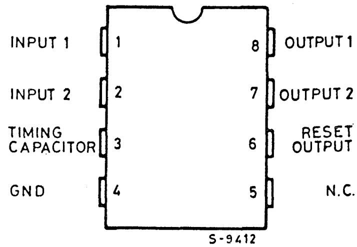
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



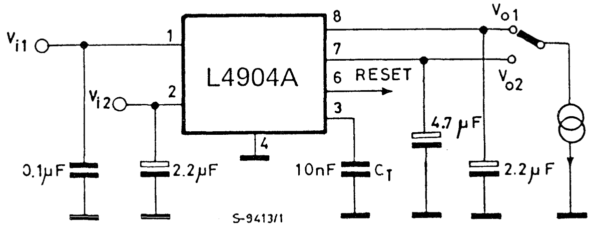
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) $= C_t$ (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

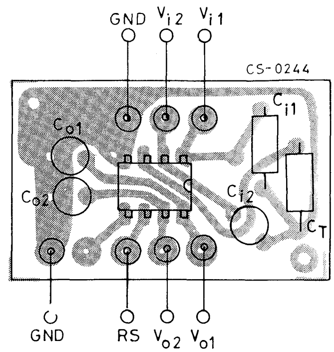
THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01} -0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	50			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	μA
I_{02}	Output current 2	ΔV_{02} = -100mV	100			mA
V_{I01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01} +1.2	6.4	V_{01} +1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation	7V < V_{IN} < 18V, I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	7V < V_{IN} < 18V, I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	V_{IN} = 8V, 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	V_{IN} = 8V, 5mA < I_{02} < 100mA		10	50	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA, I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3		11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz, V_R = 0.5V, I_o = 50mA	50	84		dB
SVR2	Supply voltage rejection	f = 100Hz, V_R = 0.5V, I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4904A makes it very easy to supply such equipments; it provides two voltage regulators (booth 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:
- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:
- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01} regulator also features low consumption (0.6mA

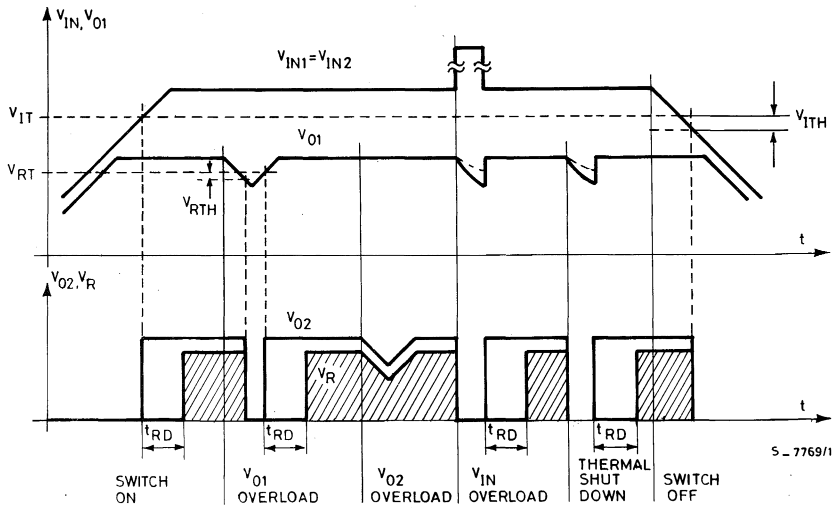
CIRCUIT OPERATION (continued)

typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 3 shows the L4904A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type C-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTIONS (continued)

Application Circuits of a Microprocessor system (Fig. 2) or with data save battery (Fig. 3). The reset output provide delayed rising front at the turn-off of the regulator 2.

Fig. 2

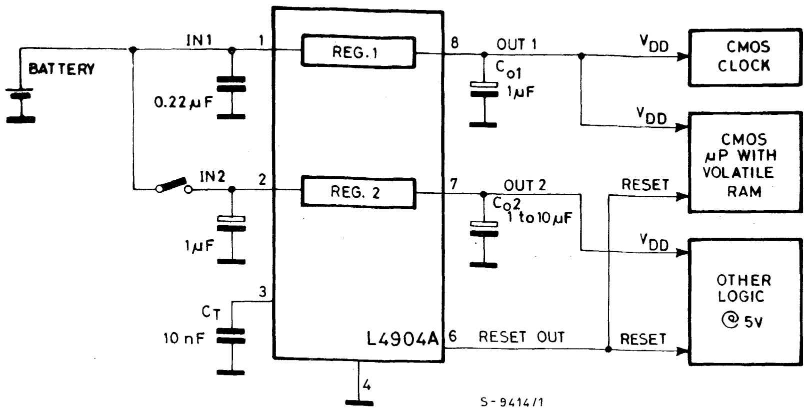
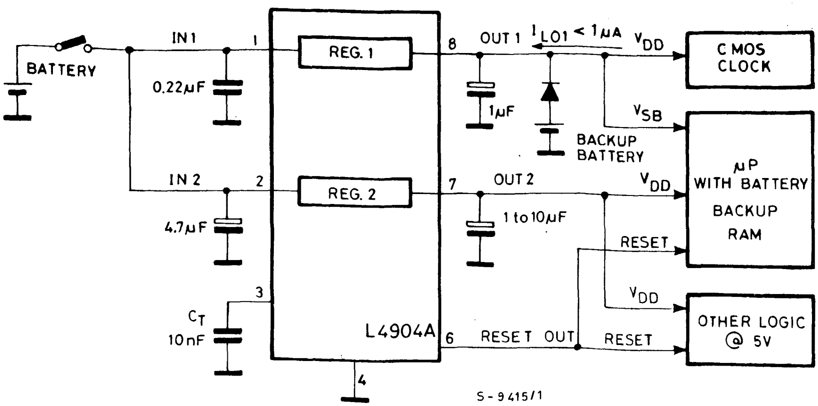


Fig. 3



APPLICATION SUGGESTIONS (continued)

Fig. 4 - Quiescent current (Reg. 1) vs. output current

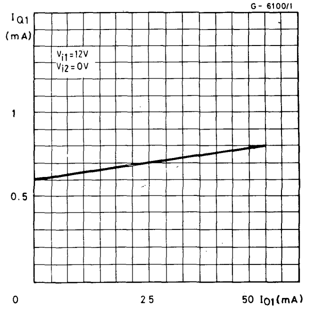


Fig. 5 - Quiescent current (Reg. 1) vs. input voltage

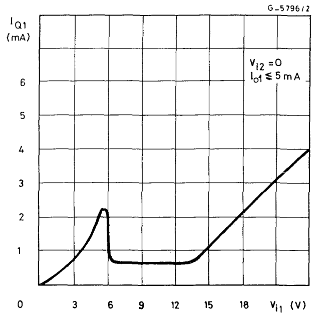


Fig. 6 - Total quiescent current vs. input voltage

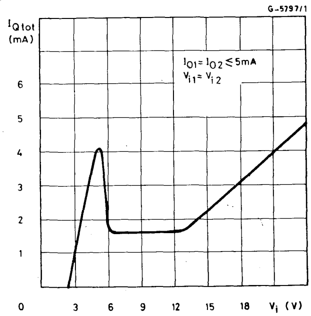
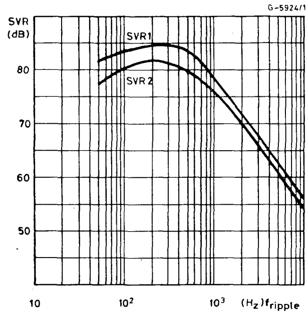


Fig. 7 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



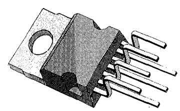
DUAL 5V REGULATOR WITH RESET

ADVANCE DATA

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: I_{01} = 200mA
  I_{02} = 300mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 1%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCIENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4905 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



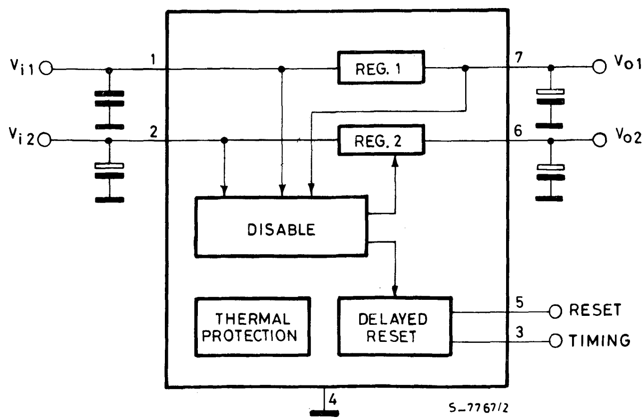
Heptawatt

ORDERING NUMBER: L4905

ABSOLUTE MAXIMUM RATINGS

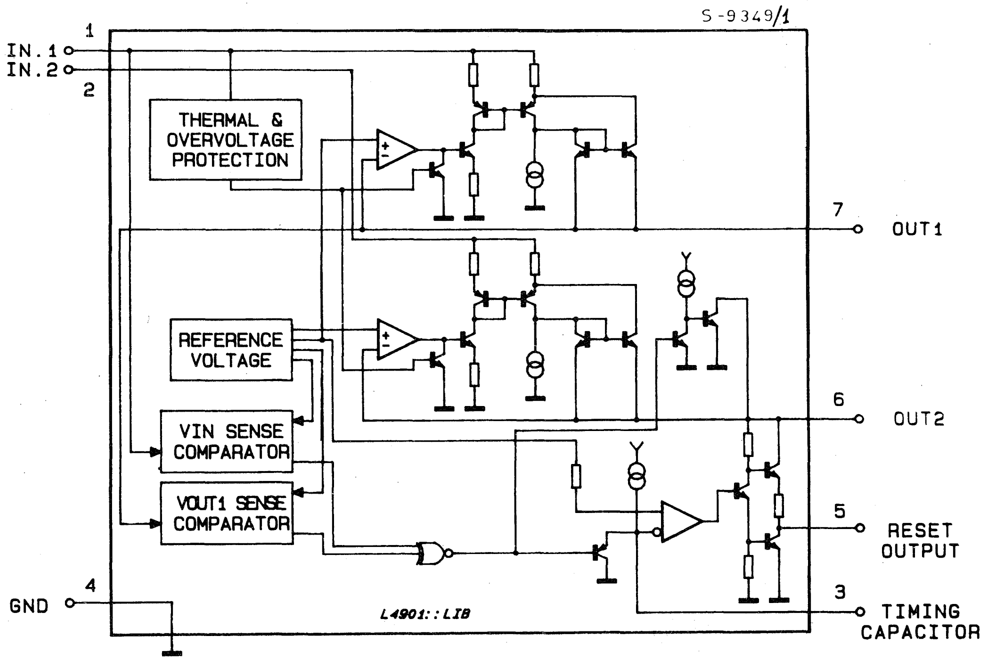
V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM

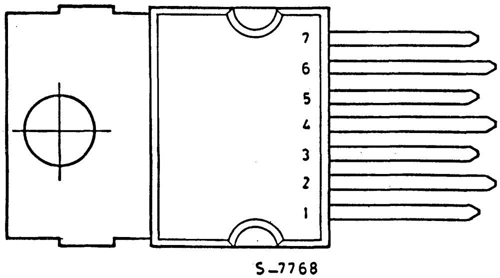


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



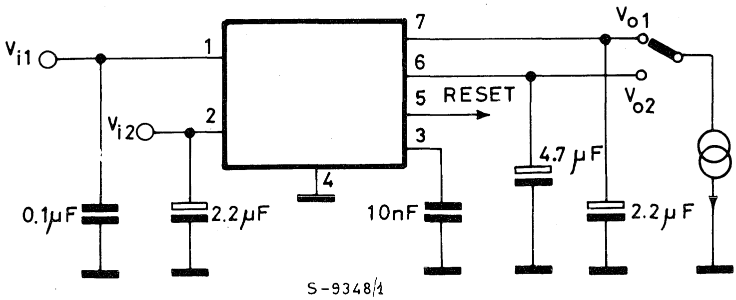
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 200mA regulator input.
2	INPUT 2	300mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A} \right)$; t_{RD} (ms) $= C_t$ (nF)
6	OUTPUT 2	5V - 300mA regulator output. Enabled if $V_O\ 1 > V_{RT}$ and $V_{IN\ 2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 200mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS
(V_{IN1} = V_{IN2} = 14,4V, T_{amb} = 25° unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				24	V
V_{01}	Output voltage 1	R load 1KΩ	5.0	5.05	5.1	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	200			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leqslant$ 3V			1	μA
I_{02}	Output current 2	ΔV_{02} = -100mV	300			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 200mA		0.7 0.8 1.05	0.8 1 1.3	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 24V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 200mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 300mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leqslant$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leqslant$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	54 50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4905 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

– an input overvoltage

– an overload on the output 1 ($V_{01} < V_{RT}$);

– a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

– 5V internal reference without voltage divider between the output and the error comparator;

– very low drop series regulator element utilizing current mirrors;

– permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

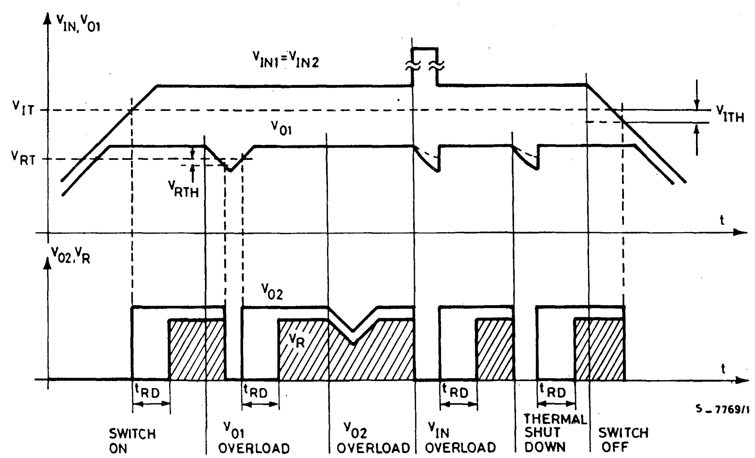
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{O2} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4905 with a back up battery on the V_{O1} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTION (continued)

Fig. 2

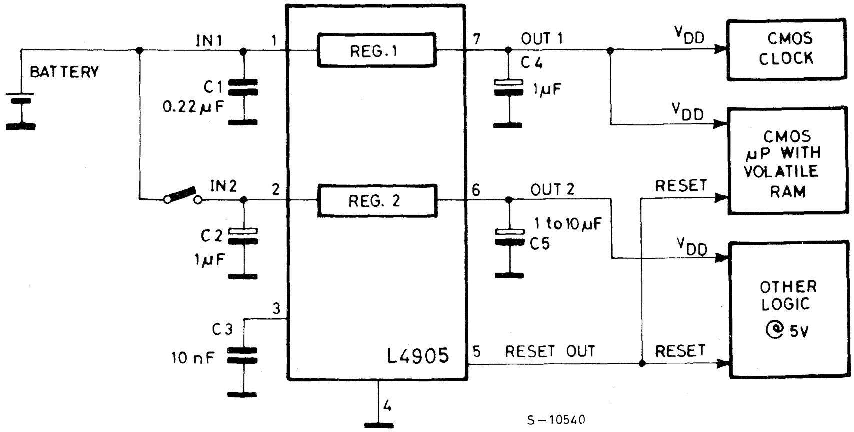
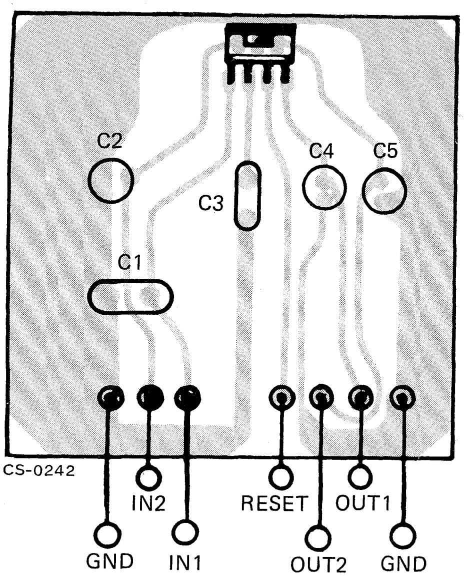


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

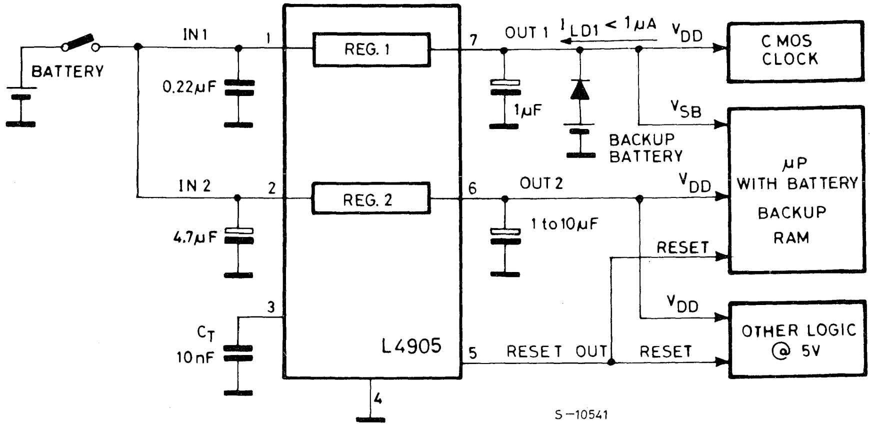


Fig. 5 - Quiescent current (Reg. 1) vs. output current

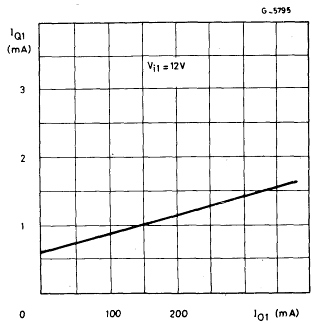


Fig. 6 - Quiescent current (Reg. 1) vs. input voltage

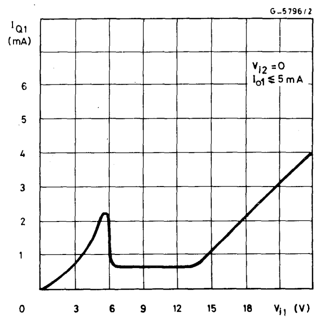
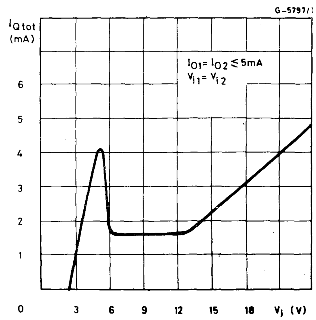


Fig. 7 - Total quiescent current vs. input voltage



ADJUSTABLE VOLTAGE REGULATOR PLUS FILTER

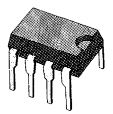
PRELIMINARY DATA

- OUTPUT VOLTAGE ADJUSTABLE FROM 4 TO 11V
- HIGH OUTPUT CURRENT (UP TO 250mA)
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION

This circuit combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wide input voltage range.

A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltage.

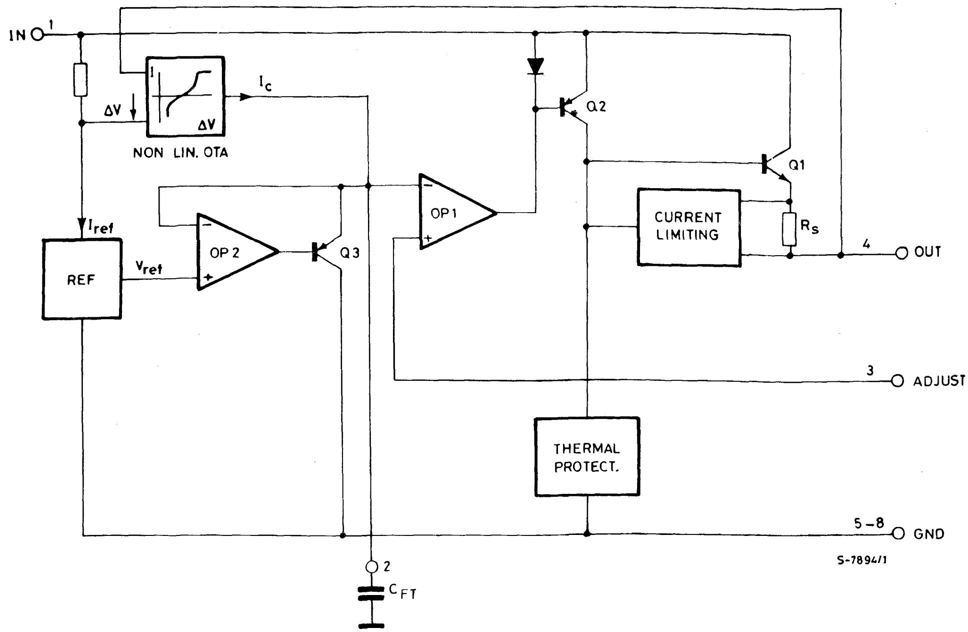
The non linear behaviour of this control circuitry allows a fast settling of the filter.



Power Minidip
(4 + 4)

ORDERING NUMBER: L4915

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_i	Peak input voltage (300ms)	40	V
V_i	DC input voltage	28	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM

(Top view)

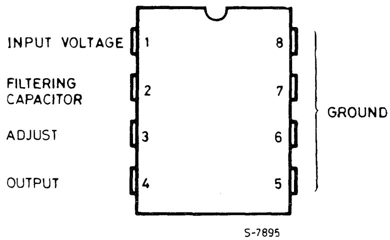
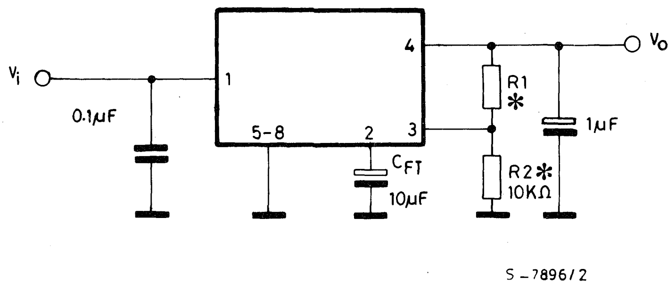


Fig. 1 - Application circuit



$$✱\text{OUTPUT VOLTAGE } V_O = \frac{2.5(R1+R2)}{R2}$$

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	20	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_i = 13.5V, V_o = 8.5V, circuit of Fig. 1, unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Input voltage				20	V
V_o	Output voltage	V_i = 6 to 18V I_o = 5 to 150mA	4		11	V
$\Delta V_{I/O}$	Controlled input-output dropout voltage	I_o = 5 to 150mA V_i = 6 to 10V		1.6	2.1	V
ΔV_o	Line regulation	V_i = 12 to 18V I_o = 10mA		1	20	mV
ΔV_o	Load regulation	I_o = 5 to 250mA t_{on} = 30μs t_{off} = ≥ 1ms		50	100	mV
ΔV_o	Load regulation (filter mode)	V_i = 8.5V I_o = 5 to 150mA t_{on} = 30μs t_{off} = ≥ 1ms		150	250	mV
V_{ref}	Internal voltage reference			2.5		V
I_q	Quiescent current	I_o = 5mA		1	2	mA
ΔI_q	Quiescent current change	V_i = 6 to 18V I_o = 5 to 150mA		0.05		mA
I_{AD}	Adjust input current			40		nA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 10mA		1.2		mV/°C
SVR	Supply voltage rejection	V_{iac} = 1V_{rms} f = 100Hz I_o = 150mA Regulator		71		dB
		Filter mode		35 (*)		dB
I_{SC}	Short circuit current		250	300		mA
T_{on}	Switch on time	I_o = 150mA Filter mode		500 (*)		ms
		Regulator		300		ms
T_j	Thermal shutdown junction temperature			145		°C

(*) Depending of the C_{FT} capacitor.

PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{I\,MIN} = V_{OUT\,NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.
The series pass element uses a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from a REF through the OP2 and Q3, acting as an active zener diode of value V_{REF}.
In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig. 2).
The output voltage is fixed to its nominal value:

$$V_{OUT\,NOM} = V_{REF}\ (1 + \frac{R1}{R2}) =$$

$$V_{CFT}\ (1 + \frac{R1}{R2})$$

The ripple rejection is quite high (70dB) and independent to C_{FT} value.
On the usual voltage regulators, when the input voltage goes below the nominal value, the regulation transistors (series element) saturate bringing the system out of regulation and making it very sensible to every variation of the input voltage. On the contrary, a control loop on the L4915 consents to avoid the saturation of the series element by regulating the value of the reference voltage (pin 2). In fact, whenever the input voltage decreases below ($V_{I\,MIN}$ the supervisor loop, utilizing a non linear OTA, forces the reference voltage at pin 2 to decrease by discharging C_{FT}. So, during the static mode, when the input voltage goes below V_{MIN} the drop out is kept fixed to about 1.6V. In this condition the device works as a low pass filter in the range (2) of the OTA characteristic. The ripple rejection is externally adjustable acting on C_{FT} as follows:

$$SVR\ (j\Omega) = \left| \frac{V_i\ (j\Omega)}{V_{out}\ (j\Omega)} \right| = \left| 1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}}\ (1 + \frac{R1}{R2})} \right|$$

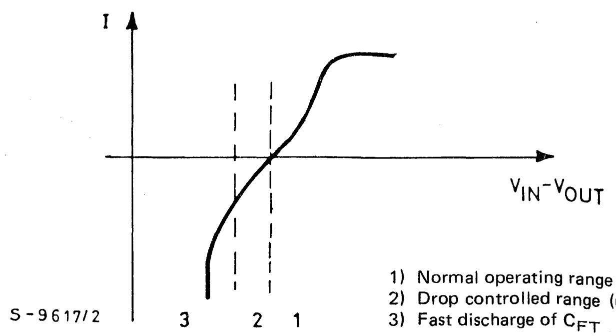
Where:
$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the transconductance of the OTA and by C_{FT}. When the value of the ripple voltage is so high and its negative peak is fast enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharges the capacitor rapidously.
If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection; the device's again working as a filter (fast transient range).
With C_{FT} = 10μF; f = 100Hz; V_o = 8.5V a SVR of 35 is obtained.

Fig. 2 – Nonliner transfer characteristic of the drop control unit



1) Normal operating range (high ripple rejection)
2) Drop controlled range (medium ripple rejection)
3) Fast discharge of C_{FT}

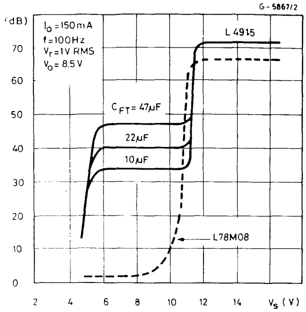


Fig. 3 - Supply voltage rejection vs. input voltage

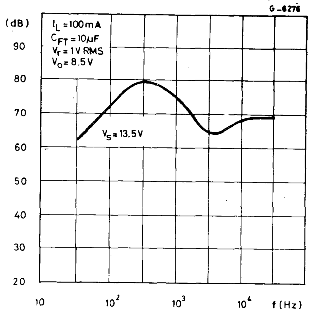


Fig. 4 - Supply voltage rejection vs. frequency

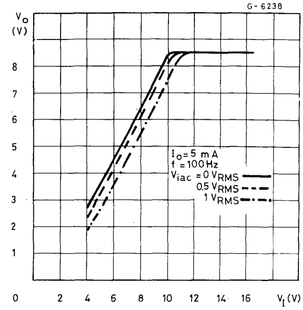


Fig. 5 - V_o vs. supply voltage (V_o = 8.5V)

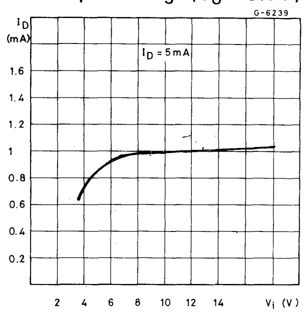


Fig. 6 - Quiescent current vs. input voltage (V_o = 8.5V)

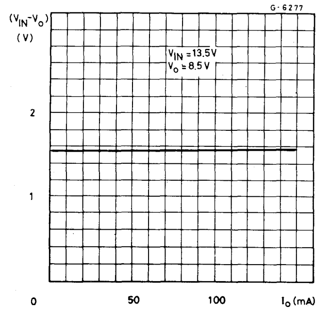


Fig. 7 - Dropout vs. load current

VOLTAGE REGULATOR PLUS FILTER

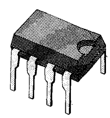
PRELIMINARY DATA

- FIXED OUTPUT VOLTAGE 8.5V
- 250mA OUTPUT CURRENT
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION

This circuit combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wider input voltage range.

A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltages.

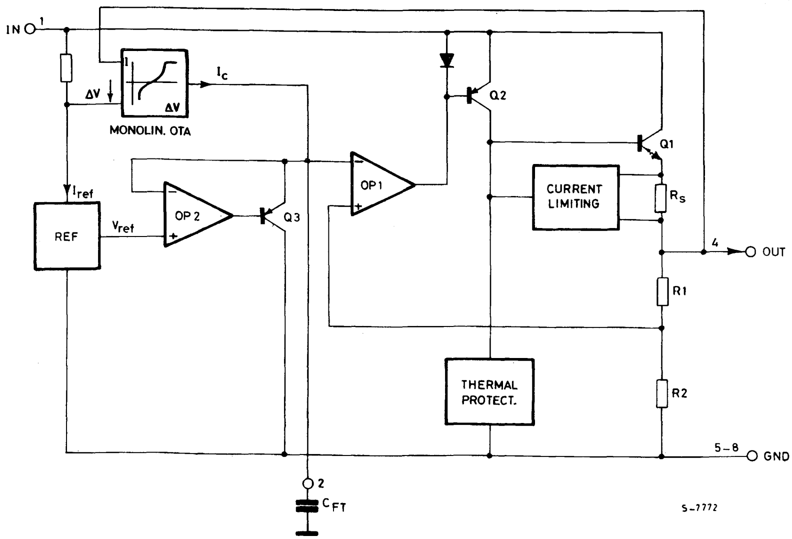
The non linear behaviour of this control circuitry allows a fast settling of the filter.



Power Minidip
(4 + 4)

ORDER CODE: L4916

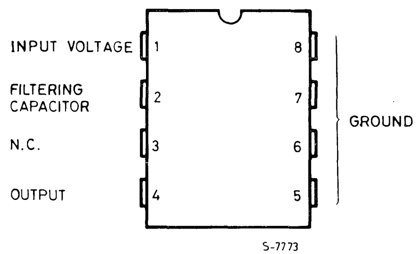
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_i	Peak input voltage (300 ms)	40	V
V_i	DC input voltage	28	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction pins	max	20	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_i = 13.5V, Test circuit of fig. 1, unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Input voltage				20	V
V_o	Output voltage	V_i = 12 to 18V I_o = 5 to 150mA	8.1	8.5	8.9	V
$\Delta V_{I/O}$	Controlled input-output dropout voltage	V_i = 5 to 10V I_o = 5 to 150mA		1.6	2.1	V
ΔV_o	Line regulation	V_i = 12 to 18V I_o = 10mA		1	20	mV
ΔV_o	Load regulation	I_o = 5 to 250mA t_{on} = 30µs t_{off} = ≥ 1ms		50	100	mV
ΔV_o	Load regulation (filter mode)	V_i = 8.5V I_o = 5 to 150mA t_{on} = 30µs,. t_{off} = ≥ 1ms		150	250	mV
I_q	Quiescent current	I_o = 5mA		1	2	mA
ΔI_q	Quiescent current change	V_i = 6 to 18V I_o = 5 to 150mA		0.05		mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 10mA		1.2		mV/°C
SVR	Supply voltage rejection	V_{iac} = 1V_{rms} f = 100Hz I_o = 150mA V_{IDC} = 12 to 18V V_{IDC} = 6 to 11V		 70 35 (*)		 dB dB
I_{SC}	Short circuit current		250	300		mA
T_{on}	Switch on time	I_o = 150mA V_i = 5 to 11V V_i = 11 to 18V		 500 (*) 300		 ms ms
T_j	Thermal shutdown junction temperature			145		°C

(*) Depending of the C_{FT} capacitor.

Fig. 1 - Test and Application Circuit

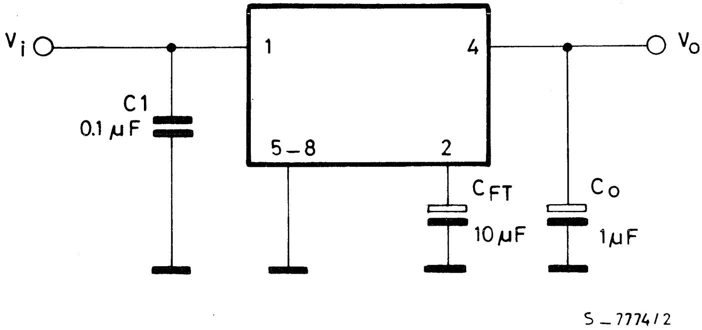
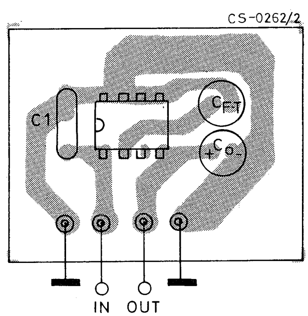


Fig. 2 - P.C. board and component layout of fig. 1 (1 : 1 scale)



PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{I\,MIN} = V_{OUT\,NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.
The series pass element use a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from a REF through the OP2 and Q3, acting as an active zener diode of value V_{REF}.
In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig. 3).
The output voltage is fixed to its nominal value:

$$V_{OUT\,NOM} = V_{REF}\left(1 + \frac{R1}{R2}\right) =$$

$$V_{CFT}\left(1 + \frac{R1}{R2}\right)$$

$$\frac{R1}{R2} = \text{INTERNALLY FIXED RATIO} = 2.4$$

The ripple rejection is quite high (70 dB) and independent from C_{FT} value.
On the usual voltage regulators, when the input voltage goes below the nominal value, the regulation transistors (series element) saturate bringing the system out of regulation making it very sensible to every variation of the input voltage.
On the contrary, a control loop on the L4916 consents to avoid the saturation of the series element by regulating the value of the reference voltage (pin 2). In fact, whenever the input voltage decreases below $V_{I\,MIN}$ the supervisor loop, utilizing a non linear OTA, forces the reference voltage at pin 2 to decrease by discharging C_{FT}.

So, during the static mode, when the input voltage goes below V_{MIN} the drop out is kept fixed to about 1.6V. In this condition the device works as a low pass filter in the range (2) of the OTA characteristic. The fipple rejection is externally adjustable acting on C_{FT} as follows:

$$SVR\,(jw) = \left|\frac{V_I\,(jw)}{V_{out}\,(jw)}\right| = \left|1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}}\left(1 + \frac{R1}{R2}\right)}\right|$$

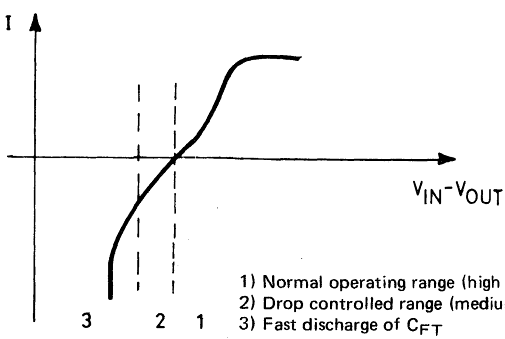
Where:
$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the transconductance of the OTA and by C_{FT}.
When the value of the ripple voltage is so high and its negative peak is fast enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharge the capacitor rapidously.
If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection; the device's again working as a filter (fast transient range).
With C_{FT}= 10 μF; f = 100 Hz a SVR of 35 is obtained.

Fig. 3 - Nonliner transfer characteristic of the drop control unit



1) Normal operating range (high ripple rejection)
2) Drop controlled range (medium ripple rejection)
3) Fast discharge of C_{FT}

S-9617/2

Fig. 4 - Supply voltage rejection vs. input voltage

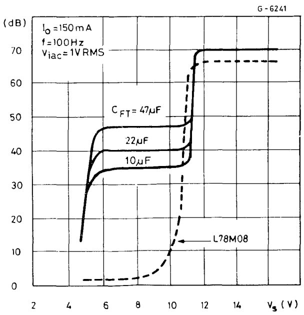


Fig. 5 - Supply voltage rejection vs. frequency

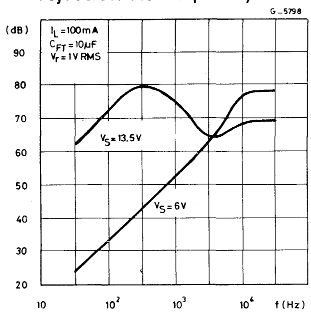


Fig. 6 - V_o vs. supply voltage

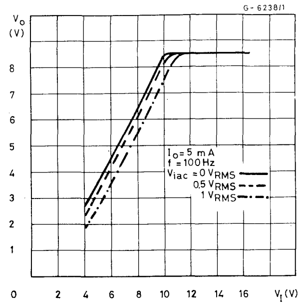


Fig. 7 - Quiescent current vs. input voltage

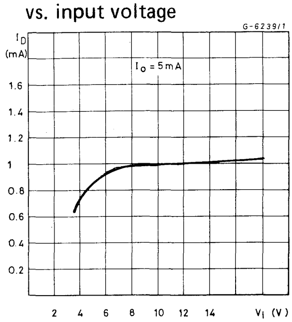


Fig. 8 - Dropout vs. load current

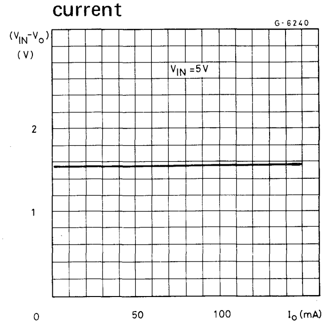
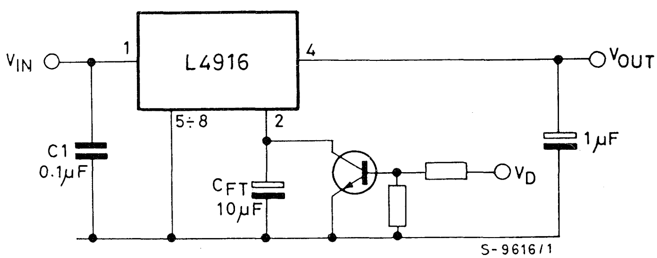


Fig. 9 - Inhibit function realized on C_{FT} pin.



SGS-THOMSON MICROELECTRONICS

SGS-THOMSON MICROELECTRONICS

L4918

VOLTAGE REGULATOR PLUS FILTER

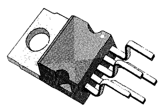
PRELIMINARY DATA

- FIXED OUTPUT VOLTAGE 8.5V
- 250mA OUTPUT CURRENT
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION

The L4918 combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wider input voltage range.

A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltages.

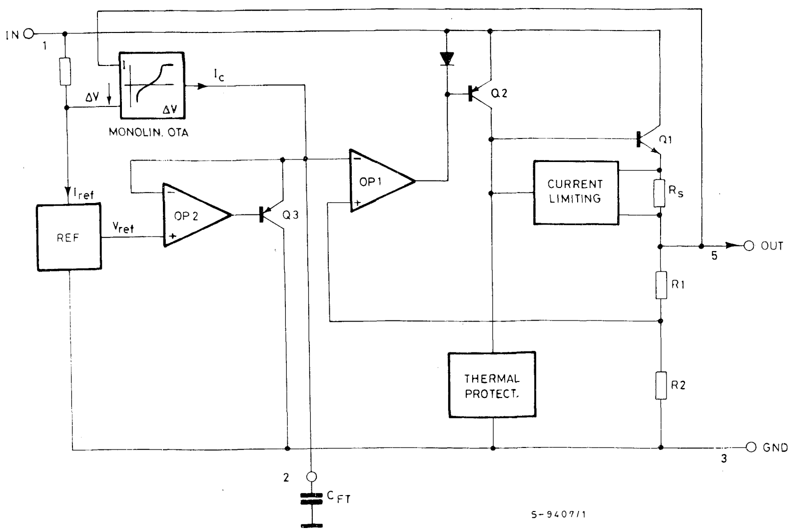
The non linear behaviour of this control circuitry allows a fast setting of the filter.



Pentawatt

ORDERING NUMBER: L4918

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Peak input voltage (300ms)	40	V
V_s	DC voltage	28	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(Top view)

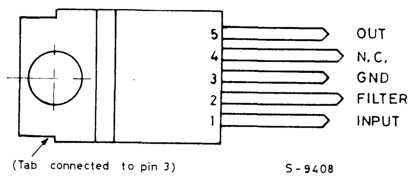
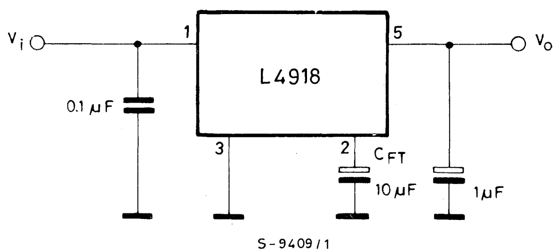


Fig. 1 - Application and test circuit



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_i = 13.5V unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	Input voltage				20	V
V_o	Output voltage	V_i = 12 to 18V I_o = 5 to 150mA	8.1	8.5	8.9	V
$\Delta V_{I/O}$	Controlled input-output dropout voltage	V_i = 5 to 10V I_o = 5 to 150mA		1.6	2.1	V
ΔV_o	Line regulation	V_i = 12 to 18V I_o = 10mA		1	20	mV
ΔV_o	Load regulation	I_o = 5 to 250mA t_{on} = 30µs t_{off} = ≥ 1ms			100	mV
ΔV_o	Load regulation	V_i = 8.5V I_o = 5 to 150mA t_{on} = 30µs t_{off} = ≥ 1ms		100	250	mV
I_q	Quiescent current	I_o = 5mA		1.0	2	mA
ΔI_q	Quiescent current change	V_i = 6 to 18V I_o = 5 to 150mA		0.05		mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 10mA		1.2		mV/°C
SVR	Supply voltage rejection	V_{iac} = 1V_{rms} f = 100Hz I_o = 150mA V_{IDC} = 12 to 18V V_{IDC} = 6 to 11V		71 35 (*)		dB dB
I_{SC}	Short circuit current		250	300		mA
t_{on}	Switch on time	I_o = 150mA V_i = 5 to 11V V_i = 11 to 18V		500 (*) 300		ms ms
T_{JSD}	Thermal shut down			150		°C

(*) Depending of the C_{FT} capacitor

PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{I\,MIN} = V_{OUT\,NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.
The series pass element use a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from a REF through the OP2 and Q3, acting as an active zener diode of value V_{REF}.
In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig. 2)
The output voltage is fixed to its nominal value:

$$V_{OUT\,NOM} = V_{REF}\left(1 + \frac{R1}{R2}\right) = V_{CFT}\left(1 + \frac{R1}{R2}\right)$$

$$\frac{R1}{R2} = \text{INTERNALLY FIXED RATIO} = 2.4$$

The ripple rejection is quite high (71 dB) and independent from C_{FT} value.
On the usual voltage regulators, when the input voltage goes below the nominal value, the regulation transistors (series element) saturate bringing the system out of regulation making it very sensible to every variation of the input voltage. On the contrary, a control loop on the L4918 consents to avoid the saturation of the series element by regulating the value of the reference voltage (pin 2). In fact, whenever the input voltage decreases below $V_{I\,MIN}$ the supervisor loop, utilizing a non linear OTA, forces the reference voltage at pin 2 to decrease by discharging C_{FT}. So, during the static mode, when the input voltage goes below V_{MIN} the drop out is kept fixed to about 1.6V. In this condition the device works as a low pass filter in the range (2) of the OTA characteristic. The ripple rejection is externally adjustable acting on C_{FT} as follows:

$$SVR\,(jw) = \left|\frac{V_I\,(jw)}{V_{out}\,(jw)}\right| = \left|1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}}\left(1 + \frac{R1}{R2}\right)}\right|$$

Where:
$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the tranconductance of the OTA and by C_{FT}.
When the value of the ripple voltage is so high and its negative peak is fast/enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharge the capacitor rapidously.
If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection; the device's again working as a filter (fast transient range).
With C_{FT}= 10 μF; f = 100 Hz a SVR of 35 is obtained.

Fig. 2 - Nonliner transfer characteristic of the drop control unit

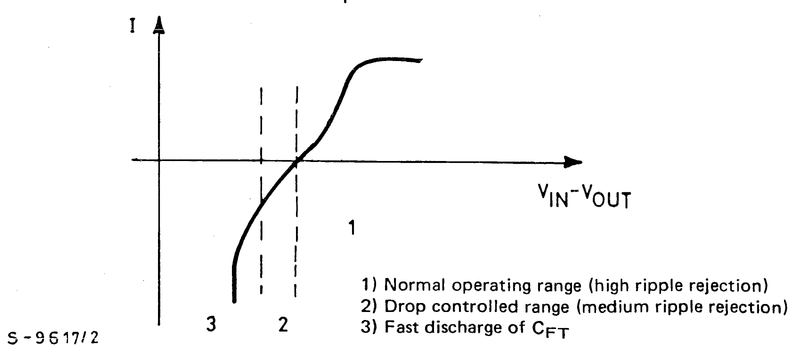


Fig. 3 - Supply voltage rejection vs. frequency

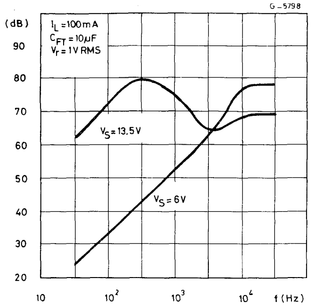


Fig. 4 - Supply voltage rejection vs. input voltage

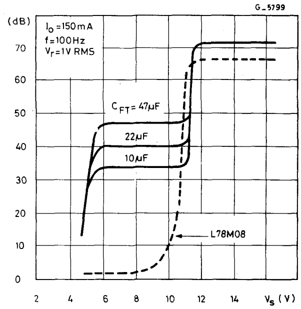
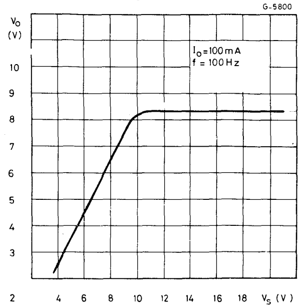
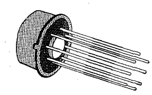


Fig. 5 - Output voltage vs input voltage

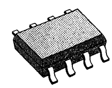


HIGH PERFORMANCE DUAL OPERATIONAL AMPLIFIER

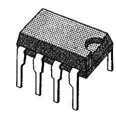
- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



TO-99



SO-8J



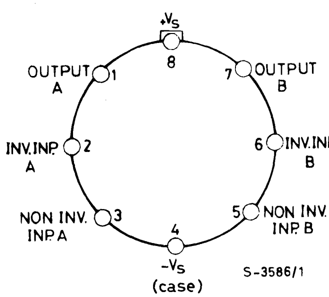
MINIDIP
(Plastic)

DESCRIPTION

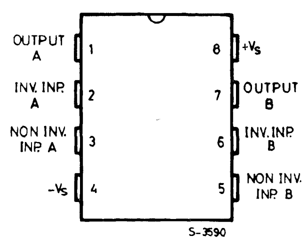
The LS204 is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products.

The circuit presents very stable electrical characteristics over the entire supply voltage range, and it particularly intended for professional and telecom applications (active filters, etc).

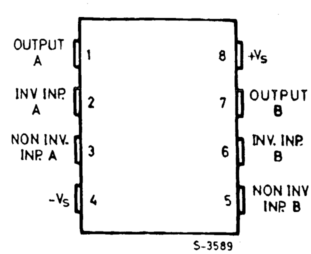
PIN CONNECTIONS (top views)



TO-99



Minidip

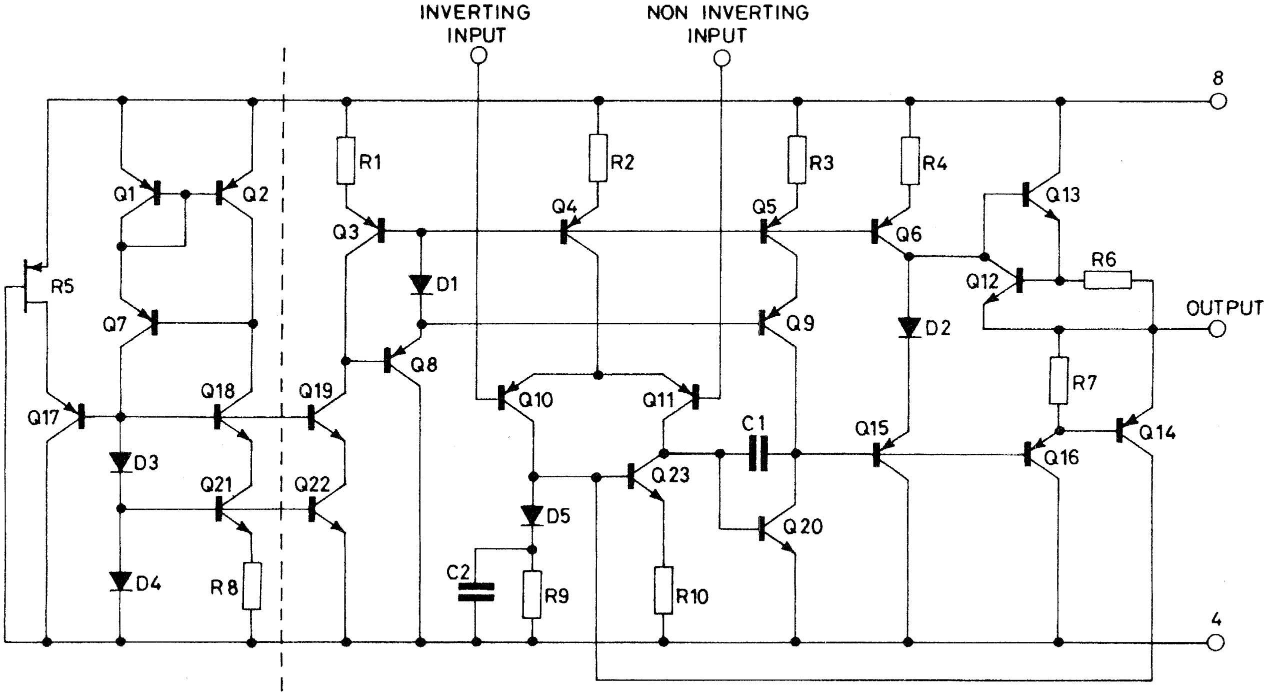


SO-8

ORDER CODES

Type	TO-99	Minidip	SO-8
LS204	LS204TB	–	LS204M
LS204A	LS204ATB	–	–
LS204C	LS204CTB	LS204CB	LS204CM

SCHEMATIC DIAGRAM



S-2104

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		TO-99	Minidip	μPackage
V_s	Supply Voltage		± 18V		
V_i	Input Voltage		$\pm V_s$		
V_i	Differential Input Voltage		$\pm (V_s - 1)$		
T_{op}	Operating Temperature for	**LS204** **LS204A** **LS204C**	– 25 to 85°C – 55 to 125°C 0 to 70°C		
P_{tot}	Power Dissipation at T_{amb} = 70°C		520mW	665mW	400mW
T_j	Junction Temperature		150°C	150°C	150°C
T_{stg}	Storage Temperature		– 65 to 150°C	– 55 to 150°C	– 55 to 150°C

THERMAL DATA

			TO-99	Minidip	SO-8J
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	155°C/W	120°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = ± 15V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	LS204/LS204A			LS204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply Current			0.7	1.2		0.8	1.5	mA
I_b	Input Bias Current			50	150		100	300	nA
		$T_{min} < T_{op} < T_{max}$			300			700	nA
R_i	Input Resistance	f = 1KHz		1			0.5		MΩ
V_{os}	Input Offset Voltage	$R_g \le 10K\Omega$		0.5	2.5		0.5	3.5	mV
		$R_g \le 10K\Omega$ $T_{min} < T_{op} < T_{max}$			3.5			5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input Offset Voltage Drift	$R_g = 10K\Omega$ $T_{min} < T_{op} < T_{max}$		5			5		μV/°C
I_{os}	Input Offset Current			5	20		12	50	nA
		$T_{min} < T_{op} < T_{max}$			40			100	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input Offset Current Drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		nA/°C
I_{sc}	Output Short Circuit Current			23			23		mA
G_v	Large Signal Open Loop Voltage Gain	$T_{min} < T_{op} < T_{max}$ $R_L = 2K\Omega$ $V_s = \pm 15V$ $V_s = \pm 4V$	90	100 95		86	100 95		dB
B	Gain-bandwidth Product	f = 20KHz	1.8	3		1.5	2.5		MHz
e_N	Total Input Noise Voltage	f = 1KHz $R_g = 50\Omega$ $R_g = 1K\Omega$ $R_g = 10K\Omega$		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	LS204/LS204A			LS204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
d	Distortion	G_V = 20dB R_L = 2KΩ V_o = 2V_{PP} f = 1KHZ		0.03	0.1		0.03	0.1	%
V_o	DC Output Voltage Swing	R_L = 2KΩ V_s = ± 15V V_s = ± 4V	± 13	± 3		± 13	± 3		V
V_o	Large Signal Voltage Swing	R_L = 10KΩ f = 10KHz		28			28		V_{pp}
SR	Slew Rate	Unity Gain R_L = 2KΩ	0.8	1.5			1		V/µs
CMR	Common Mode Rejection	V_i = 10V $T_{min} < T_{op} < T_{max}$	90			86			dB
SVR	Supply Voltage Rejection	V_i = 1V f = 100Hz $T_{min} < T_{op} < T_{max}$	90			86			dB
CS	Channel Separation	f = 1KHz 100	120			120			dB

Note :

Temp.	LS204	LS204A	LS204C
$T_{min.}$	– 25°C	– 55°C	0°C
$T_{max.}$	+ 85°C	+ 125°C	+ 70°C

Figure 1: Supply Current vs. Supply Voltage.

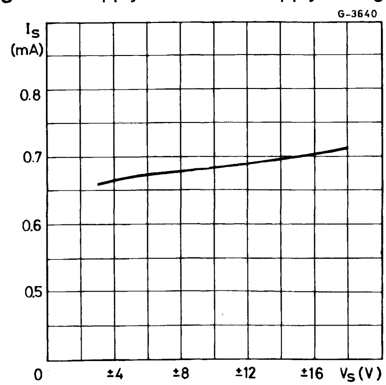


Figure 2 : Supply Current vs. Ambient Temperature.

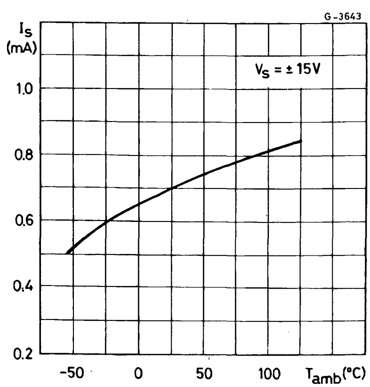


Figure 3 : Output Short Circuit Current vs. Ambient Temperature.

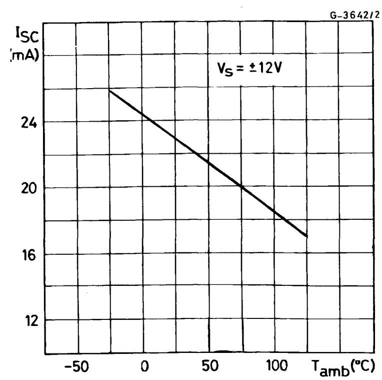


Figure 4: Open Loop Frequency and Phase Response.

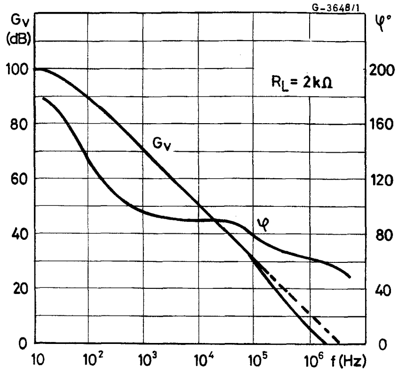


Figure 5: Open Loop Gain vs. Ambient Temperature.

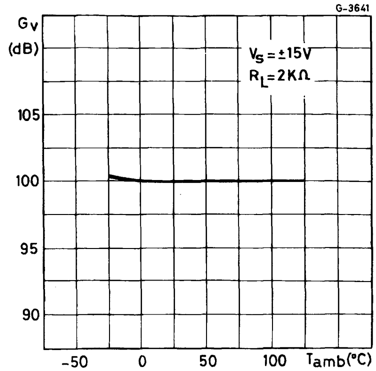


Figure 6 : Supply Voltage Rejection vs. Frequency.

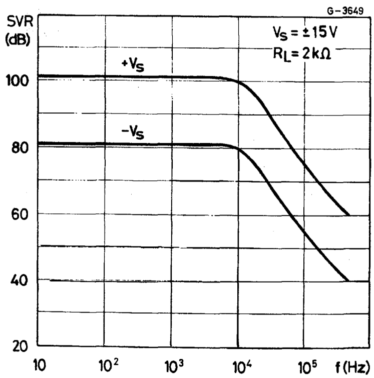


Figure 7 : Large Signal Frequency Response.

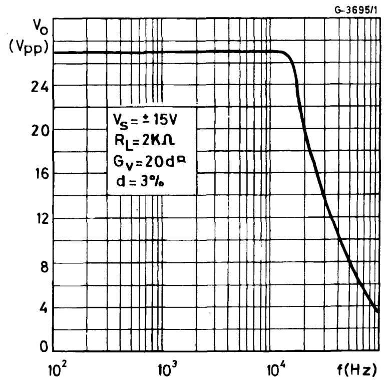


Figure 8 : Output Voltage Swing vs. Load Resistance.

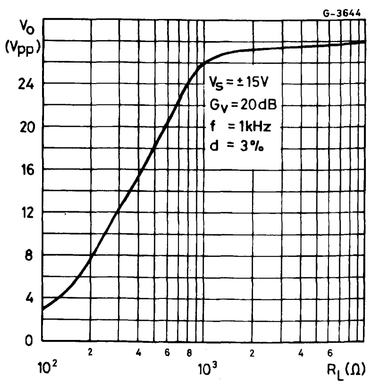
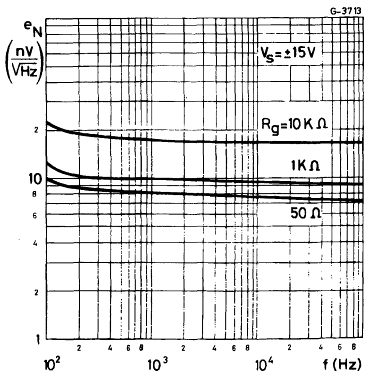


Figure 9 : Total Input Noise vs. Frequency.



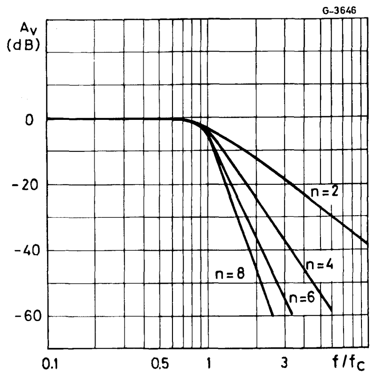
APPLICATION INFORMATION

Active low-pass filter :

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_C, is the frequency at which the amplitude response is down 3 dB. The attenuation rate beyond the cutoff frequency is n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics :
- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

Figure 10 : Amplitude Response.



BESSEL

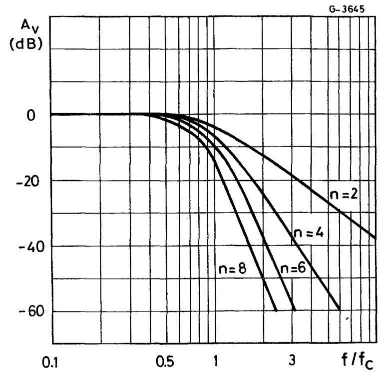
The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, fc, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the – 3dB frequency of the filter.

	2 pole	4 Pole	6 Pole	8 Pole
– 3dB Frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics :
- Selectivity not as great as Chebyschev or Butterworth.
- Very little overshoot response to step inputs.
- Fast rise time.

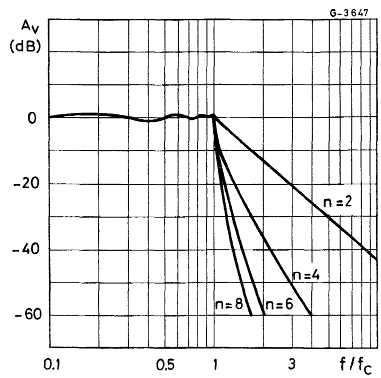
Figure 11 : Amplitude Response.



CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.

Figure 12 : Amplitude Response (± 1dB ripple).



APPLICATION INFORMATION (continued)

Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.

Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

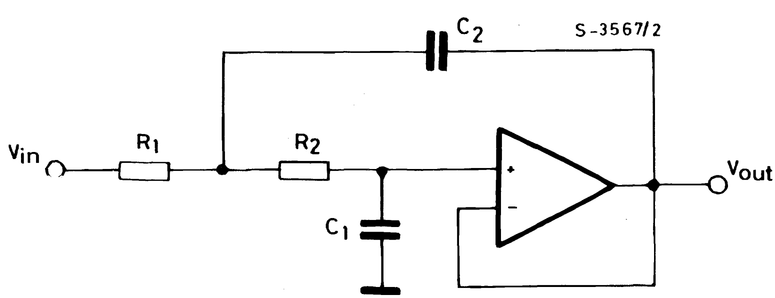
Other characteristics :
- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	Number of Poles	Peak Overshoot	Settling Time (% of final value)		
		% Overshoot	± 1%	± 0 .1%	± 0.01%
Butterworth	2	4	$1.1/f_c$sec.	$1.7/f_c$sec.	$1.9/f_c$sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
Bessel	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
Chebyschev (ripple ± 0.25dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
Chebyschev (ripple ± 1dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

Design of 2nd order active low pass filter (Sallen and Key configuration unity gain-op-amp).

Figure 13 : Filter Configuration.



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_C} + \frac{S^2}{\omega_C^2}}$$

Where :

$\omega_c = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

Three parameters are needed to characterise the frequency and phase response of a 2nd order active filter : the gain (G_V), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).

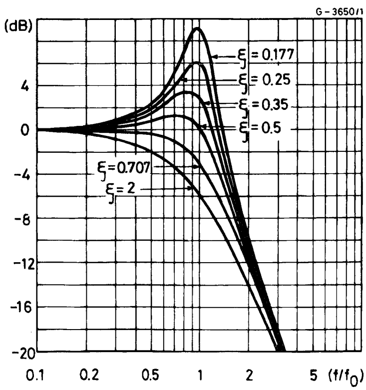
The higher order responses are obtained wit a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table).

Table 1.

Filter Response	ξ	Q	Cutoff Frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which Phase Shift is – 90°C
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at Which G_V = – 3dB
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band.

Figure 14 : Filter Response vs. Damping Factor.



Fixed R = R1 = R2, we have (see fig. 13)

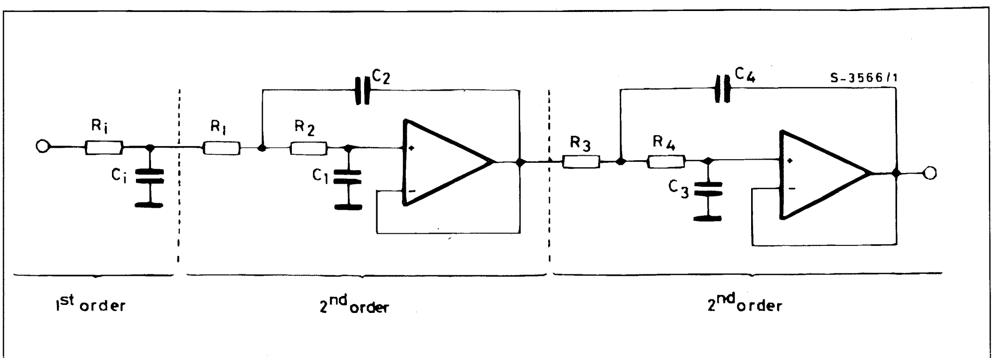
$$C_1 = \frac{1}{R} \quad \frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R} \quad \frac{1}{\xi\omega_c}$$

The diagram of fig.14 shows the amplitude response for different values of damping factor ξ in

EXAMPLE

Figure 15 : 5th Order Low Pass Filter (Butterworth) with Unity Gain Configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for $f_c = 3.4$ KHz and $R_i = R_1 = R_2 = R_3 = R_4 = 10\ K\Omega$, we obtain :

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For $f_c = 5$ KHz and $C_i = C_1 = C_2 = C_3 = C_4 = 1$ nF we obtain :

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5K\Omega$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6K\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2K\Omega$$

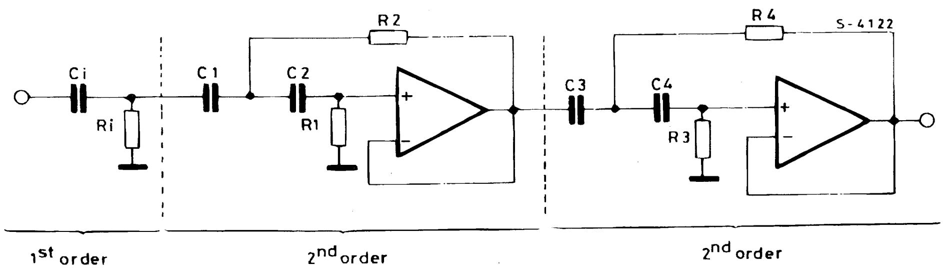
$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103K\Omega$$

$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6K\Omega$$

Table 2 : Damping Factor for Low-pass Butterworth Filters.

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

Figure 16 : 5_{th} Order High-pass Filter (Butterworth) with Unity Gain Configuration.



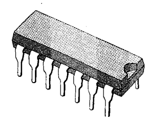
HIGH PERFORMANCE QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION

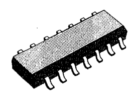
DESCRIPTION

The LS404 is a high performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth product. The circuit presents very stable electrical characteristics over the entire supply voltage range, and it is particularly intended for professional and telecom applications (active filters, etc.).

The patented input stage circuit allows small input signal swings below the negative supply voltage and prevents phase inversion when the input is over driven.



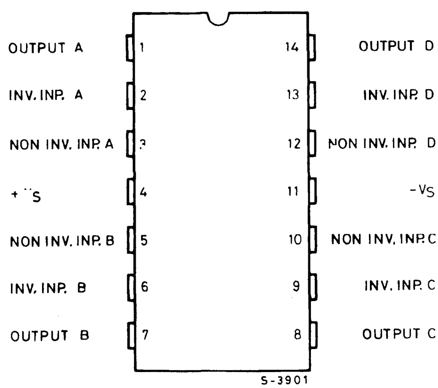
DIP14
(Plastic 0.25)



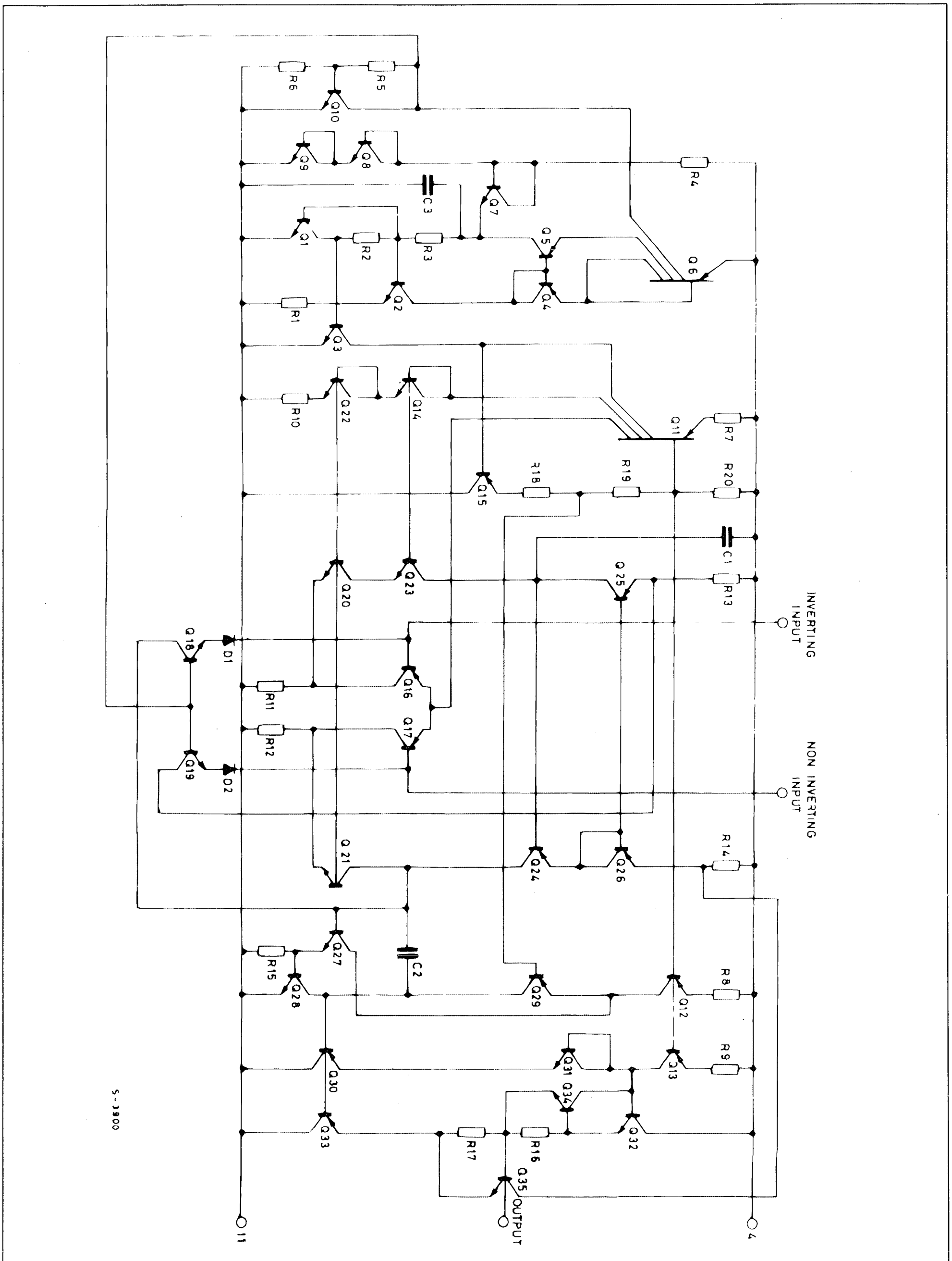
SO-14J

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)

Type	DIP 14	SO-14
LS404 LS404C	– LS404CB	LS404D1 LS404CD1
LS 8404 LS8404C	– –	LS 8404M LS 89404CM



SCHEMATIC DIAGRAM (one section)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_s	Supply Voltage		± 18	V
V_i	Input Voltage	(positive) (negative)	+ V_s – V_s – 0.5	V
V_i	Differential Input Voltage		± (V_s – 1)	
T_{op}	Operating Temperature	**LS404** **LS404C**	– 25 to + 85 0 to + 70	°C °C
P_{tot}	Power Dissipation	(T_{amb} = 70°C)	400	mW
T_{stg}	Storage Temperature		– 55 to + 150	°C

THERMAL DATA

			DIP 14	SO–14 J
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	200°C/W	200°C/W

(*) Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

ELECTRICAL CHARACTERISTICS (V_s = ± 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions		LS404 Min.	LS404 Typ.	LS404 Max.	LS404C Min.	LS404C Typ.	LS404C Max.	Unit
I_s	Supply Current				1.3	2		1.5	3	mA
I_b	Input Bias Current				50	200		100	300	nA
R_i	Input Resistance	f = 1 KHz			0.7	2.5		0.5	5	MΩ
V_{os}	Input Offset Voltage	R_g = 10 KΩ			1			1		mV
$\frac{\Delta V_{os}}{\Delta T}$	Input Offset Voltage Drift	R_g = 10 KΩ $T_{min} < T_{op} < T_{max}$			5			5		μV/°C
I_{os}	Input Offset Current				10	40		20	80	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input Offset Current Drift	$T_{min} < T_{op} < T_{max}$			0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output Short Circuit Current				23			23		mA
G_v	Large Signal Open Loop Voltage Gain	R_L = 2 KΩ	V_s = ± 12 V V_s = ± 4 V	90	100 95		86	100 95		dB
B	Gain-bandwidth Product	f = 20 KHz		1.8	3		1.5	2.5		MHz
e_N	Total Input Noise Voltage	f = 1 KHz R_g = 50 Ω R_g = 1 KΩ R_g = 10 KΩ			 8 10 18	 15		 10 12 20		$\frac{nV}{\sqrt{Hz}}$
d	Distortion	Unity Gain R_L = 2 KΩ V_o = 2 V_{PP}	 f = 1 KHz f = 20 KHz		 0.01 0.03	 0.04		 0.01 0.03		%
V_o	DC Output Voltage Swing	R_L = 2 KΩ	V_s = ± 12 V V_s = ± 4 V	± 10	 ± 3		± 10	 ± 3		V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	LS404			LS404C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Large Signal Voltage Swing	f = 10 KHz R_L = 10 KΩ R_L = 1 KΩ		22 20			22 20		V_{pp}
SR	Slew Rate	Unity Gain R_L = 2 KΩ	0.8	1.5			1		V/µs
CMR	Common Mode Rejection	V_i = 10 V	90	94		80	90		dB
SVR	Supply Voltage Rejection	V_i = 1 V f = 100 Hz	90	94		86	90		dB
CS	Channel Separation	f = 1 KHz	100	120			120		dB

Figure 1: Supply Current vs. Supply Voltage.

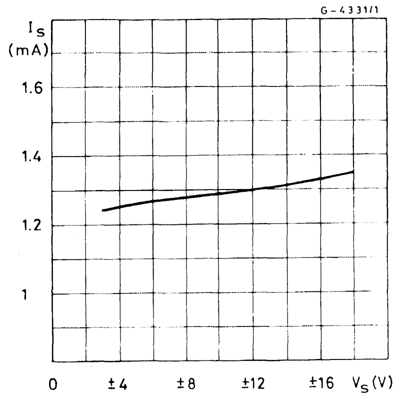


Figure 2 : Supply Current vs. Ambient Temperature.

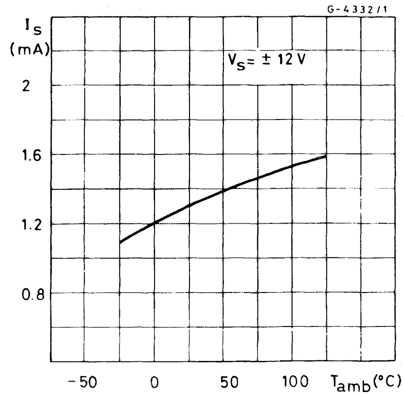


Figure 3 : Output Short Circuit Current vs. Ambient Temperature.

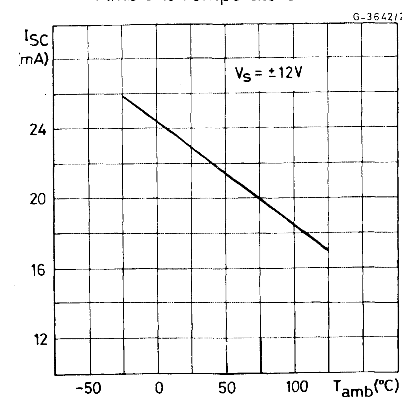


Figure 4: Open Loop Frequency and Phase Response.

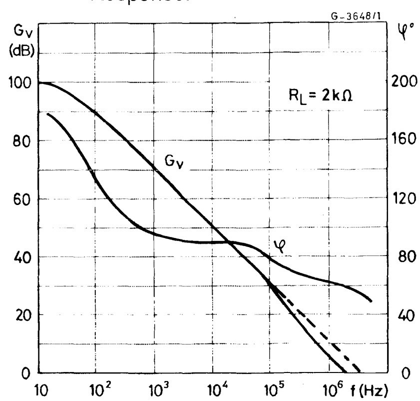


Figure 5: Open Loop Gain vs. Ambient Temperature.

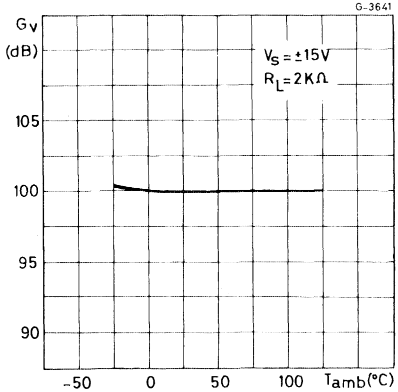


Figure 6 : Supply Voltage Rejection vs. Frequency.

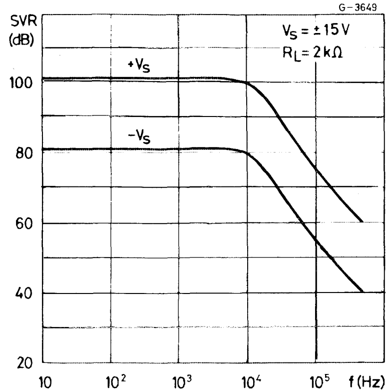


Figure 7 : Large Signal Frequency Response.

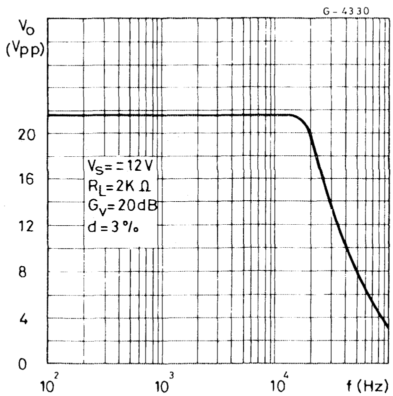


Figure 8 : Output Voltage Swing vs. Load Resistance.

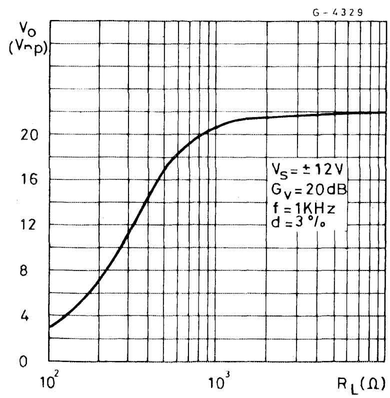
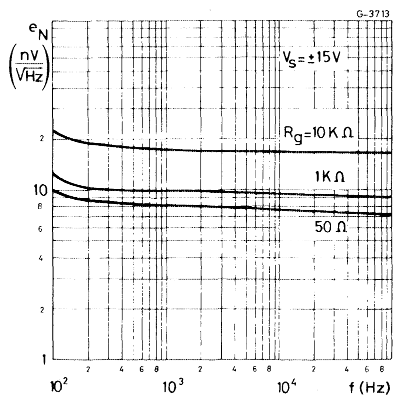


Figure 9 : Total Input Noise vs. Frequency.



APPLICATION INFORMATION

Active low-pass filter :

BUTTERWORTH

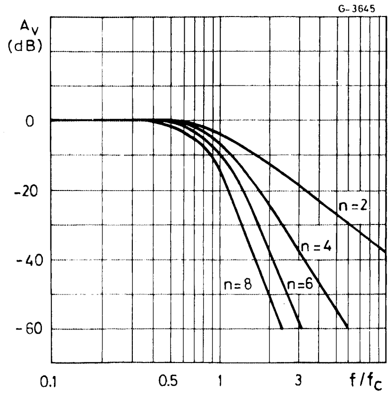
The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.

The cutoff frequency, f_C, is the frequency at which the amplitude response in down 3 dB. The attenuation rate beyond the cutoff frequency is - n6 dB per octave of frequency where n is the order (number of poles) of the filter.

Other characteristics :

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

Figure 10 : Amplitude Response.



BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

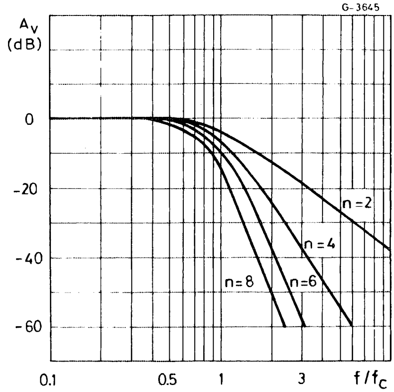
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_C, is defined as the frequency at which the phase shift is one half to this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the – 3 dB frequency of the filter.

	2 pole	**4 Pole**	**6 Pole**	**8 Pole**
– 3dB Frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics :

- Selectivity not as great as Chebyschev or Butterworth.
- Very small overshoot response to step inputs.
- Fast rise time.

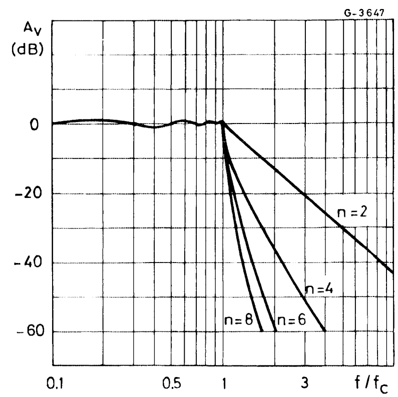
Figure 11 : Amplitude Response.



CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.

Figure 12 : Amplitude Response (± 1 dB ripple).



APPLICATION INFORMATION (continued)

Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.

Increased ripple in the passband allows increased attenuation above the cutoff frequency.

The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

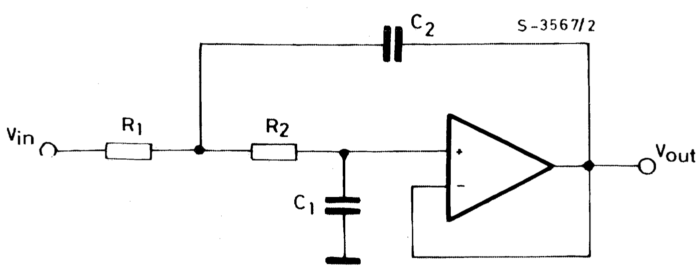
Other characteristics :
- Greater selectivity.
- Very nonlinear phase response.
- High overshoot response to step inputs.

The table below shows the typical overshoot and setting time response of the low pass filter to a step input.

	Number of Poles	Peak Overshoot	Settling Time (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
Butterworth	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
Bessel	2	0.4	0.8/fc	1.4/fc	1.7/fc
	4	0.8	1.0/fc	1.8/fc	2.4/fc
	6	0.6	1.3/fc	2.1/fc	2.7/fc
	8	0.3	1.6/fc	2.3/fc	3.2/fc
Chebyschev (ripple ± 0.25dB)	2	11	1.1/fc	1.6/fc	–
	4	18	3.0/fc	5.4/fc	–
	6	21	5.9/fc	10.4/fc	–
	8	23	8.4/fc	16.4/fc	–
Chebyschev (ripple ± 1dB)	2	21	1.6/fc	2.7/fc	–
	4	28	4.8/fc	8.4/fc	–
	6	32	8.2/fc	16.3/fc	–
	8	34	11.6/fc	24.8/fc	–

Design of 2^{nd} order active low pass filter (Sallen and Key configuration unity gain op-amp).

Figure 13 : Filter Configuration.



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

Where :

$\omega c = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter : the gain (G_V), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_C).

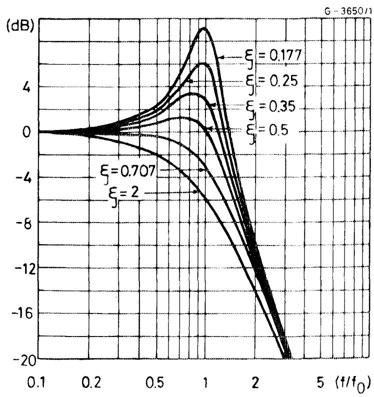
The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table).

Table 1.

Filter Response	ξ	Q	Cutoff Frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which Phase Shift is – 90°C
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which G_V = – 3dB
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band.

Figure 14 : Filter Response vs. Damping Factor.



Fixed R = R1 = R2, we have (see fig. 13)

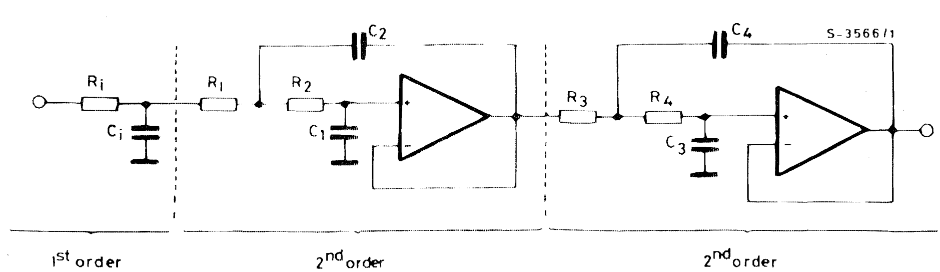
$$C_1 = \frac{1}{R} \frac{\xi}{\omega_C}$$

$$C_2 = \frac{1}{R} \frac{1}{\xi\omega_C}$$

The diagram of fig.14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE

Figure 15 : 5th Order Low Pass Filter (Butterworth) with Unity Gain Configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4$ =10 KΩ, we obtain :

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\text{nF}$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\text{ nF}$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\text{ nF}$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\text{ nF}$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\text{ nF}$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5 KHz and $C_i = C_1 = C_2 = C_3 = C_4$ = 1 nF we obtain :

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\text{ K}\Omega$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6\text{ K}\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2\text{ K}\Omega$$

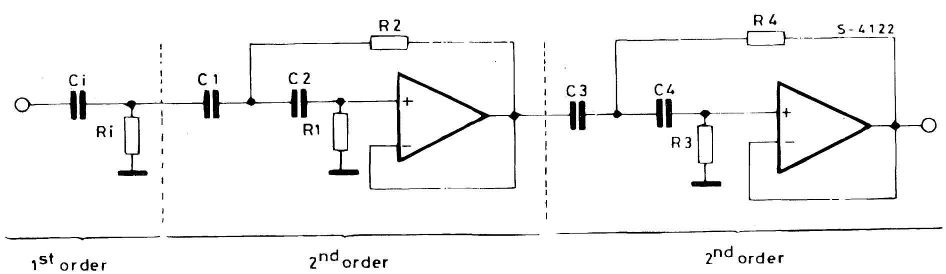
$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103\text{ K}\Omega$$

$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6\text{ K}\Omega$$

Table II : Damping Factor for Low-pass Butterworth Filters.

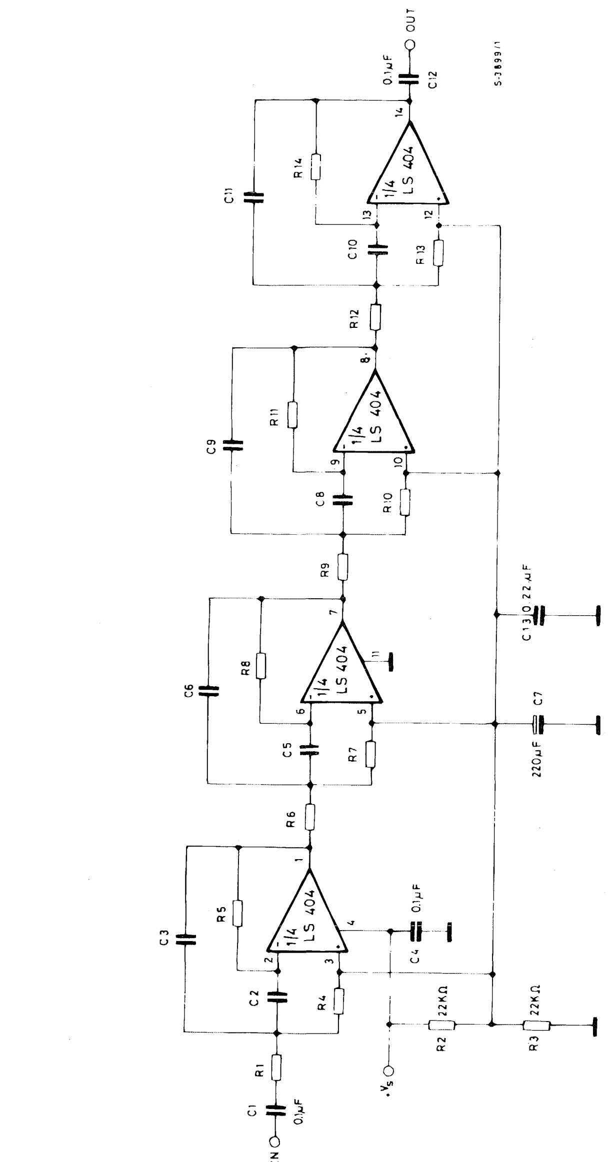
Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

Figure 16 : 5^{th} Order High-pass Filter (Butterworth) with Unity Gain Configuration.



APPLICATION INFORMATION (continued)

Figure 17 : Multiple Feedback 8-pole Bandpass Filter.



f_c = 1.180 Hz ; A = 1 ; $C_2 = C_3 = C_5 = C_6 = C_8 = C_9 = C_{10} = C_{11}$ = 3.300 pF ;

$R_1 = R_6 = R_9 = R_{12}$ = 160 KΩ ; $R_5 = R_8 = R_{11} = R_{14}$ = 330 KΩ ; $R_4 = R_7 = R_{10} = R_{13}$ = 5.3 KΩ

Figure 18 : Frequency Response of Band-pass Filter.

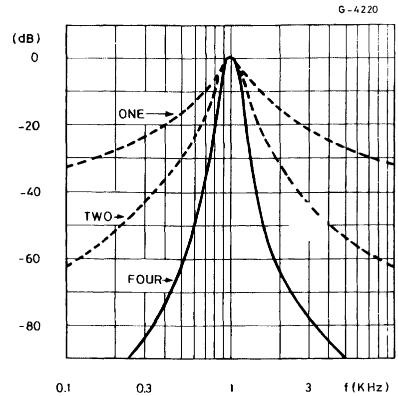


Figure 19 : Bandwidth of Band-pass Filter.

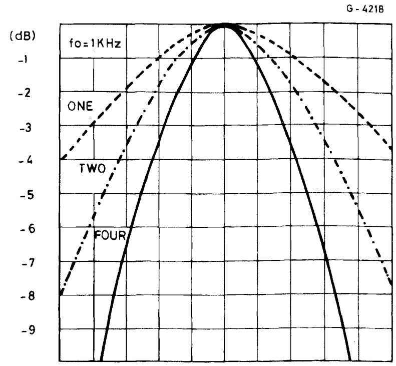
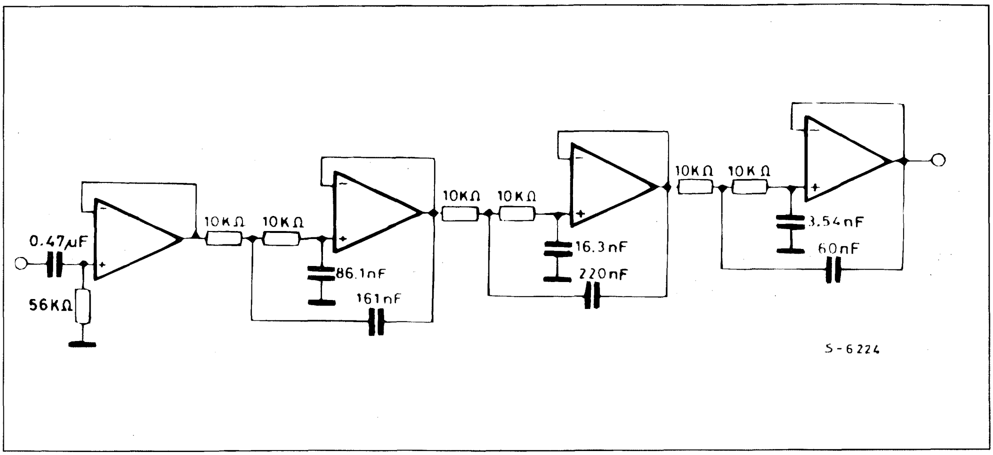
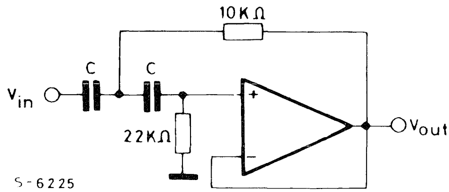


Figure 20 : Six-pole 355 Hz Low-pass Filter (chebychev type).



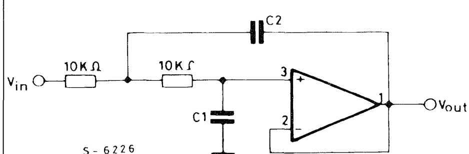
This is a 6-pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc.

Figure 21 : Subsonic Filter (G_V = 0 dB).



f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

Figure 22 : High Cut Filter (G_V = 0 dB).



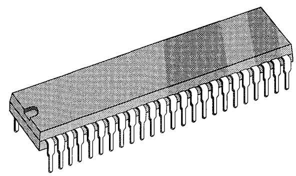
f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

SGS-THOMSON MICROELECTRONICS

M114A
M114AF

DIGITAL SOUND GENERATOR

- INPUT CLOCK FREQ: 4MHz (M114A)
  6MHz (M114AF)
- MAX EXTERNAL ADDRESSING MEMORY OF 256K
- 16 INDEPENDENT CHANNELS
- SOUND GENERATED BY READING TABLES CODED IN DELTA CODING OR IN ABSOLUTE VALUES
- 12 BIT EQUIVALENT D/A CONVERTER RESOLUTION (delta coding)
- 8 DIFFERENT TABLE LENGTHS AND 8 READING MODES GIVING A TOTAL OF 58 DISTINCT COMBINATIONS
- 16 DIFFERENT MIXABLE LAYERS BETWEEN TWO SEPARATE TABLES
- MULTIPLE READING PERMITS INTERPOLATION BETWEEN TWO ADJOINING SAMPLES ON THE SAME TABLE
- 4 SELECTABLE ANALOG OUTPUTS
- 10 BIT INTERNAL ATTENUATOR WITH GRADUAL AMPLITUDE VARIATION
- ROM ENABLE OUTPUT TO MINIMISE EXTERNAL MEMORY POWER CONSUMPTION
- POSSIBILITY OF SYNCHRONOUS AND ASYNCHRONOUS FREQUENCY-TABLE CHANGE AT THE END OF THE READING TABLE



DIP-48

ORDERING NUMBERS: M114A1
M114AF (6MHz version)

The M114A/AF is a 16 channel digital polyphonic, politimbric sound generator, designed for electronic musical instruments.

It is available in two versions, differing in the clock speed: M114A (4MHz input clock frequency) and M114AF (6MHz)

The M114A/AF must be driven by a microprocessor and needs an external memory.

With this device it is possible to synthesize a large range of sounds by simply transcribing the most significant periods of the sound to be reproduced into an external memory and programming a suitable reading sequence for these periods with the use of a microprocessor.

The M114S/SF is realized on a single monolithic silicon chip using low threshold N-channel silicon gate MOS technology and is assembled in plastic DIP 48.

PIN CONNECTION (Top view)

Signal	Pin	Pin	Signal
GND (digital)	1	48	EOT
EA1	2	47	EA 0
ROM ADDR 0	3	46	BUS STROBE
ROM ADDR 1	4	45	BUS 0
ROM ADDR 2	5	44	BUS 1
ROM ADDR 3	6	43	BUS 2
ROM ADDR 4	7	42	BUS 3
ROM ADDR 5	8	41	BUS 4
EA3	9	40	BUS 5
EA2	10	39	ROM DATA 7
ROM ADDR 6	11	38	ROM DATA 6
ROM ADDR 7	12	37	ROM DATA 5
ROM ADDR 8	13	36	ROM DATA 4
ROM ADDR 9	14	35	ROM DATA 3
ROM ADDR 10	15	34	ROM DATA 2
ROM ADDR 11	16	33	ROM DATA 1
ROM ADDR 12	17	32	ROM DATA 0
VDD (digital)	18	31	ROM ENABLE
CLOCK	19	30	ANALOG OUT3
RESET	20	29	ANALOG OUT2
GND (analog)	21	28	ANALOG OUT1
VDDA (analog)	22	27	N.C.
VREF	23	26	ANALOG OUT 0
TAB1/TAB2	24	25	+12V OUT

M91M114AF-02

ABSOLUTE MAXIMUM RATINGS

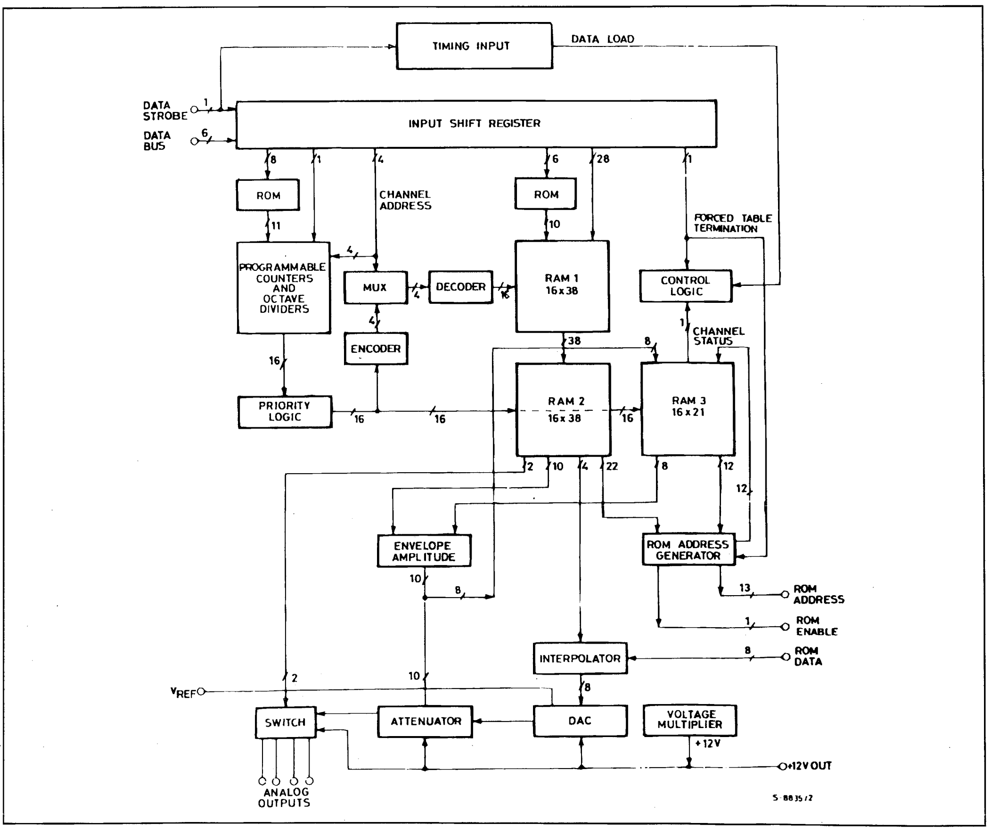
Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7	V
V_I	Input Voltage	– 0.3 to V_{DD}	V
V_O	Output Voltage	– 0.3 to V_{DD}	V
P_{tot}	Total Package Power Dissipation	1000	mW
T_{stg}	Storage Temperature	– 40 to + 150	°C
T_{op}	Operating Temperature	0 to + 60	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

THERMAL DATA

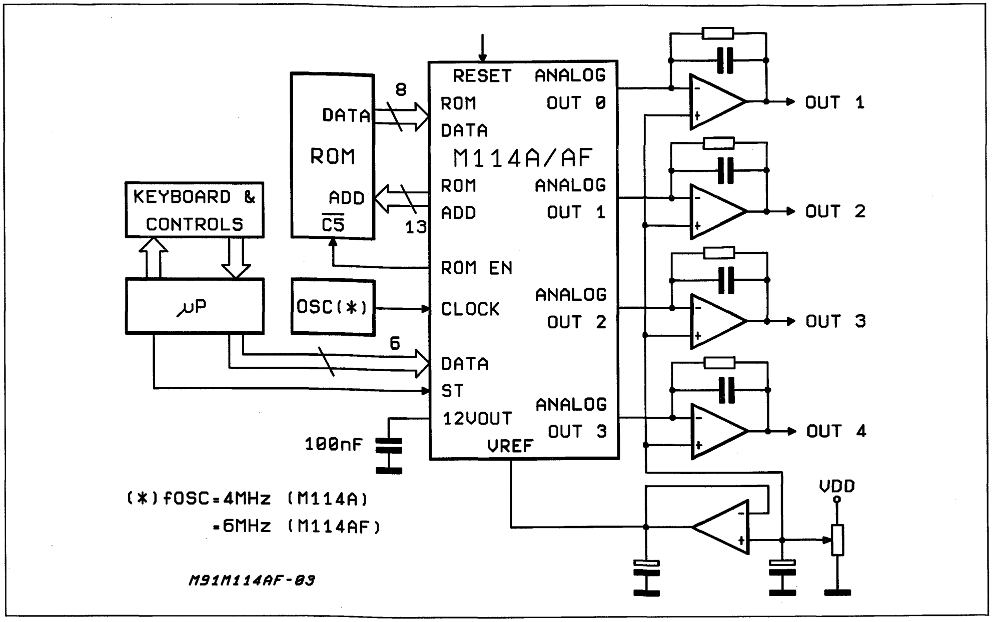
Symbol	Description	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient max.	100	°C/W

Figure 1. Block Diagram



SGS-THOMSON MICROELECTRONICS

Figure 2: System Configuration



STATIC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 5 %, T_{amb} = 25 °C, V_{DD} = V_{DDA})

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
INPUTS: RESET (pin 20), CLOCK (pin 19), ROM DATA (pins 32-39), DATA BUS (pins 40-45), DATA ST. (pin 46)						
V_{IL}	Low Input Level				0.8	V
V_{IH}	High Input Level		2.2			V
I_I	Input Leakage Current	V_I = V_{DD} to GND			± 1	µA
DIGITAL OUTPUTS: (high impedance*): ROM-ADD (pins 3-8; 11-17), EA (pins 2, 9, 10, 47), ROM-EN. (pin 31), EOT (pin 48), Tab1/Tab2 (pin 24)						
V_{OL}	Low Output Level	I_{OL} = 1 mA			0.4	V
V_{OH}	High Output Level	I_{OH} = 100 µA	2.4			V
ANALOG OUTPUTS: (pins 26, 28, 29, 30), V_{REF} (pin 23)						
V_{REF}	Voltage Reference Output	I_O = ± 1mA	2.4	2.5	2.6	V
I_O	Output Current (current generator)	Zero Attenuation Max Input Code to the DAC		± 1		mA
POWER DISSIPATION						
I_{DD}	Supply Current Digital	V_{DD} = 5.25V f = 4MHz (M114A) V_{DD} = 5.25V f = 6MHz (M114AF)		100 100	120 130	mA mA
I_{DDA}	Supply Current Analog	V_{DA} = 5.25V		5	10	mA

* High impedance means that, when the addresses are off, the digital output is connected with an internal resistive pull-up of 10kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 5 %, T_{amb} = 25 °C, V_{DD} = V_{DDA})

Symbol	Parameter	Test Conditions	Value						Unit
			M114S			M114SF			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CLOCK									
t_{CK}	Input Clock Frequency			4.000			6000		kHz
t_r, t_f	Rise and Fall Time	10 % to 90 %			20			15	ns
t_{WH}, t_{WL}	High and Low Pulse Width		80			60			ns
RESET									
t_{wRES}	Pulse Width		10			6			ms
t_f	Fall Time	10 % to 90 %			20			15	ns
DATA BUS									
$t_{w\ DATA}$	Pulse Width		1250			830			ns
$t_{set\text{-}up\ DATA}$	Set-up Time to Data Strobe		0			0			ns
$t_{hold\ DATA}$	Hold Time from Data Strobe		1250			830			ns
DATA STROBE									
t_{WST}	Pulse Width		1.5		128	1		85	µs
t_{WRST}	Pulse Width for Internal Reset Generation		128			85			µs
t_r, t_f	Rise and Fall Times				40			20	µs
ROM ENABLE									
t_{LOW}				600			400		ns
t_{HIGH}				350			220		ns
$t_{set\text{-}up\ EN}$(*)	Set-up Time ROM-EN		70			55			ns

(*) $t_{set\text{-}up\ EN}$. Time means that the data coming from ext. ROM must be stable at least 70ns before the rising edge of ROM enable.

PIN FUNCTIONS

PIN 1 - GND (Digital)
Digital ground is linked to this pin.

PIN 21 - GND (Analog)
Analog ground is linked to this pin.

PIN 3 - 8 and 11 - 17 ROM-ADD
13 PUSH-PULL type output pins for external memory address. When the output is off (doesn't exist an address) the output is connected to an internal resistive pull-up of about 10KΩ.

PINS 2, 9, 10, 47 - EA
These four pins give in output the channel number that is reading the external memory. When the output is off (doesn't exist an address) the output is connected to an internal pull-up. With these 4 pins the memory is expanded up to 128 Kbyte (8 Kbyte/channel).

PIN 24 - TAB1/TAB2
It shows which one of the two tables (TAB1 or TAB2) is read. Pin 24 permits to double the memory so reading 256 Kbyte addressing memory (top configuration).

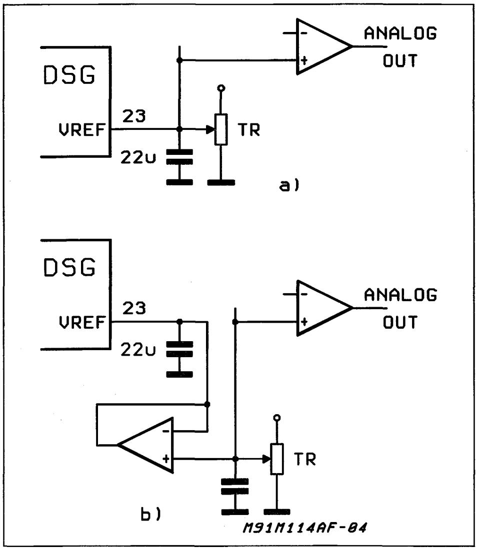
PIN 19 - CLOCK 4 MHz (M114A), 6 MHz (M114AF)
For correct functioning the duty cycle must be very close to 50 %. Internal circuits are dynamic, so the clock is continuously required to maintain internal information.

PIN 20 - RESET
All channels are reset by rising this pin. The 13 external ROM address outputs together with the 4 sound outputs are placed in a high impedance state.

PIN 22 - ANALOG POWER SUPPLY
The power supply for all analog parts, i.e. DAC, attenuator, etc ...., are linked to this pin. It is therefore important that this power supply should be very stable and well smoothed. The internal power supply chip separation allows a great improvement of signal/noise ratio.

PIN 23 - VOLTAGE REFERENCE (V_{REF})
VREF is the average value of the DAC output. With Vsupply = 5 V VREF is nominally 2.5 V but could vary by chip to chip (± 100mV). At the integrator output the DC level can change when a channel turns-on or turns-off. To minimize this drop it is necessary to trim the value of VREF by TR trimmer (fig. 3A, 3B). The solution of fig 3B is more efficient than in fig.3A: in fact the behaviour is as better as less is the seen impedance at the VREF pin.

Figure 3



PINS 26, 28, 29, 30 - ANALOG OUT
These outputs are under current with an output impedance of approximately 1 KΩ and the filter, or external integrator, must have a low input impedance. This means that the voltage drop between output pin and V_{REF} must be negligeable so as to obtain a good signal linearity. An integrator is necessary if the tables have been "DELTA" coded. If on the other hand they have been coded in absolute values then only a low pass filter is needed.

PINS 31 - ROM-ENABLE (Low active)
This is a PUSH-PULL-TYPE-OUTPUT and is used to set the external memory in stand-by so as to reduce consumption whenever it is not read.

PINS 32 - 39 - ROM-DATA
8 input pins for data from external memory.

PINS 40 - 45 - DATA-BUS
6 input pins for data from the microprocessor. 8 of these data groups make up a complete piece of information (48 bit).

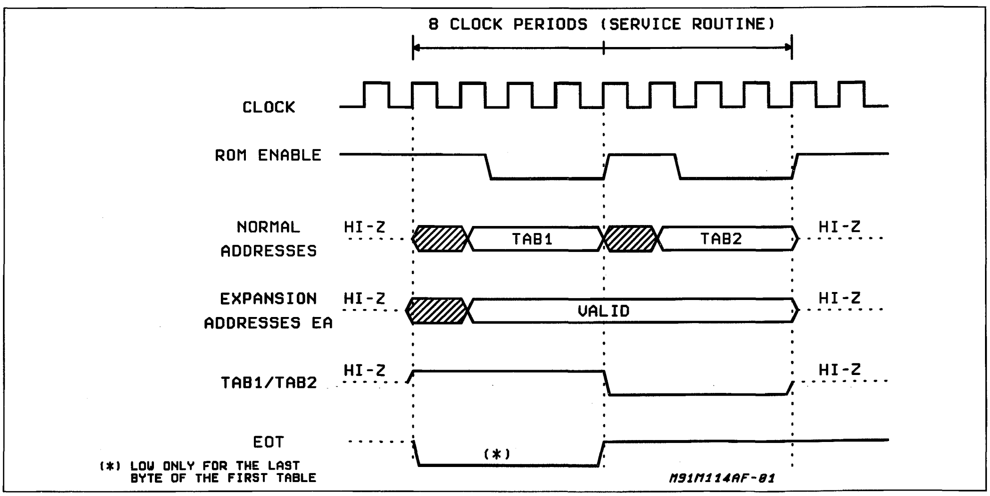
PIN 46 - BUS STROBE
A signal from the microprocessor must arrive at this input in order to memorise the present code onto the DATA-BUS. Memorization occurs on both edges.

PIN 27 - N.C.

PIN 18 - DIGITAL POWER SUPPLY
The power supply for all digital parts, i.e. counters, memories, etc ...., are linked to this pin.

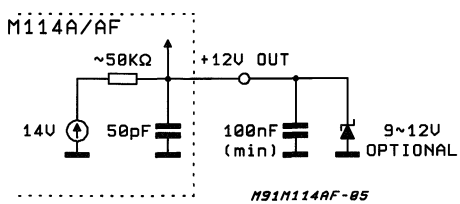
PIN 48 - End of table
A low level pulse 4 clock cycles long, is output by this pin every time the last byte of the first table is read. The channel/number can be read from the EA outputs (See Fig.4).

Figure 4: Memory Interface Timing



PIN 25 (+ 12 V out)
This pin is the output of an internal 5V/14V DC-DC converter and it needs of an external filtering capacitance (min. 100 nF). The performance of DAC and attenuator are very improved with an external zener that clamps the voltage elevator output (see fig. 5).

Figure 5



GENERAL DESCRIPTION

The M114A/AF is a device that allows digital sound synthesis. The essential system needed consists of a microprocessor, an M114A/AF and an external memory with a maximum of 256 Kbytes . Sound generation is based on cyclic reading of tables corresponding to waveforms (periods) of the timbre to be reproduced.

As the waveform and therefore also the spectrum frequently change, a series of tables of form and frequency appropriate to the sound are cyclically scanned during sound reproduction.

The effect caused by the sudden passage from one table to the next would be unpleasant unless there is such a large number of tables to allow a smooth unnoticeable change from one table to the following.

A favourable compromise between number of tables and quality of sound, that has been implemented in the M114A/AF is the following : a limited number of tables which may even diverge from one another are chosen during an initial phase of analysis after which, during the reproduction phase, always two tables are read simultaneously by extracting a percentage of one and the remaining percentage of the other. Therefore by starting with 100 % of one and zero of the other and successively increasing the second while decreasing the first, a smooth passage is achieved. In the M114A/AF this passage is made up of a maximum of 16 steps.

The tables are stored in an external memory and may be of eight different lengths ranging from 16 to 2048 bytes. The tables may be coded using waveform's absolute value or by the difference between adjoining samples, that is, in a incremental manner (Delta coding). The table samples must be in 8 bits format, complement with 2. The Delta coding increases the equivalent resolution. The typical resolution is 12 bit with a sinusoidal wave coded in a 16-byte table.

OUTPUT RECONSTRUCTION

An external low pass filter (absolute value coding) or an integrator (Delta coding) are sufficient to reconstruct the original sound. The difference is only the value of the feedback network. The Delta coding allows easy interpolation. By simply reading the same data n time and dividing the amplitude of each reading by n, a ramp of n small steps is obtained instead of a large single step. The value of n may be 1, 2 or 4. When a waveform is coded in this way (Delta-Coding or incrementally), the sum of the samples in an entire period must always be equal to zero or there would be a DC offset which could even saturate the external integrator.

MEMORY EXPANSION

With the 13 pins ROM-ADD is possible to address 8 Kbyte of memory. The 4 pins named EA permit an expansion to 128 Kbyte, while with the pin TAB1/TAB2 we have 256 Kbyte for the top configuration . A decoding section for the address, programmable by microprocessor, can be arranged in such a way to readdress each channel on any number, very great too, of 16 Kbytes memory blocks.

The frequency of the generated samples is a whole multiple of the table lenght. In this way any problem caused by intermodulation is eliminated but a noise due to "collision" is produced. As there is a single output circuit for all channels, (interpolar, D/A converter, attenuator, ecc.), each time more than one channel requires access to these circuits one, or more, other channel must wait.

The amount of time necessary for the output circuit to process each table, that is the period of time for which each channel uses the circuit during each sample reading cycle, is of 2 µs for the M114A (1.5 µs for the M114AF). The delay will therefore be proportional to the number of channels operating simultaneously and to the frequency that they are generating. As these parameters casually vary, so will the delay thus producing a casual alteration of the original waveform. ("collision noise") Simulation has proved that under worst possible conditions the signal/noise ratio due to this problem is around 60 dB.

The sound amplitude envelope has to be controlled by the microprocessor which, at suitable intervals, must forward the desired attenuation coefficient. There are 64 possible attenuations each with steps of approximately 0.75 dB ; These passage from one level to another may be immediate or to gradual increments of 1/256 of the maximum amplitude at a frequency proportional to external table reading frequency.

OPERATION

The M114A/AF receives from the μP a single programming sequence at a time. This programming sequence is made up of 48 bits. The μP must send a 48 bit set for every M114A/AF active channel (16 independent channels). Each M114A/AF channel continuously generates the same signal: it reads the same table, with the same mixing coefficient, with the same amplitude, ecc., until the microprocessor forwards a different programming sequence (variation of one or more parameters characterising the sound to be generated within a single channel). Timbre amplitude evolution and any other slight frequency changes must be handled in real-time by the microprocessor.

Each channel reads two samples from two tables, at the sampling frequency, sums them according to the mixing coefficient and forwards the result to the DAC whose suitably attenuated output goes to the previously selected output pin (fig. 6).

This operation requires 2 μs (1.5 μs in the M114AF) and as there is a single output circuit for all channels it is certain that one or more channels will simultaneously request the use of the circuit. Thus a priority order has been assigned to each channel.

This order is fixed: channel zero has greatest priority followed in order by the others. When more than one channel is simultaneously active at the output pin there will be an overlap of impulses (the impulse of the lower priority channel will be delayed) The example of Fig.7 shows an output signal with 2 active channels, CH1 has greater priority then CH2.

The signal will change from impulsive to continuous by passing through:

- a low pass filter if the table have been coded using absolutes values.
- an integrator if in delta coding

AMPLITUDE ENVELOPE GENERATOR

When the microprocessor programs one channel with a new attenuation level, different from the preceding one, this new level can be reached immediately or by a smooth move (depends from the setting of the amplitude control bit described elsewhere). The M114A/AF envelope generator only controls and changes the 8 MSB among the 10 bit of the attenuation code. The gradual movement from the present level to that just programmed takes place by increasing or decreasing these 8 MSB of attenuation with the same frequency with which the external memory tables are being scanned if the difference in level is greater than 128 steps, or with 1/2 of this frequency if grater than 64 steps or 1/4 if greater than 32, or 1/8 if smaller than or equal to 32.

INPUT INTERFACE WITH THE MICROPROCESSOR

The M114A/AF has been designed to easily interface with every microprocessor. The microprocessor interface has a 6-bit data bus and a single control line, the DATA strobe. 48 bits subdivided into 8 groups of 6 bit each must be forwarded in order to programme a single channel.

Figure 6

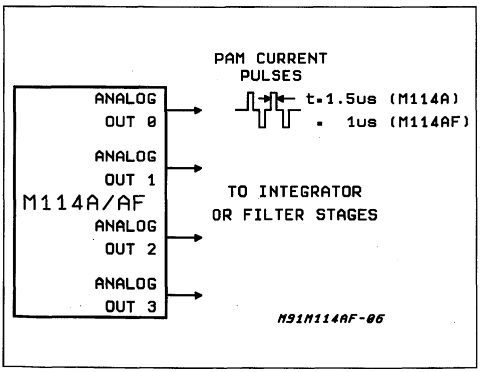
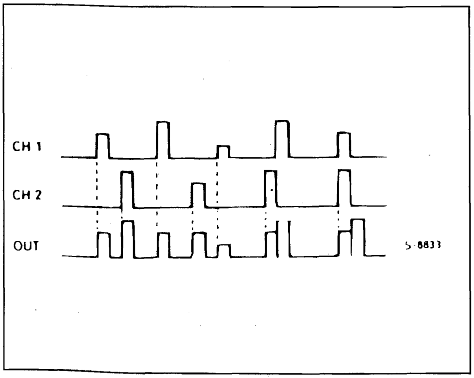


Figure 7



A group of 6 bits is memorized on every data STROBE switch front. As the data bus is read approximately 250ns after strobe transition, the 6 data bits may be sent simultaneously with the strobe. The whole set of 48 bit have to be entered for any channel programming operation. The entering order is indicated in table A.

MEANING OF THE 48 PROGRAMMABLE BITS IN THE PROGRAMMING SEQUENCE

Channel Address (4 bits)

These four bits indicate to which of the 16 M114A/AF channel the remaining 44 bits will be forwarded.

Frequency Code (8 bits)

The 4 most significant bits cover 15 semitones (HEX code from 0 to E) The graph of fig. 8 shows the time lapse that must be assigned to these signal for correct functioning. No more than 128 μs (85 in the M114AF) must pass between one data Strobe transition and the next during transmission of the 8 groups of data or else synchronisation is lost due to the device internal automatic reset.

There is no upper limit for the elapsed time between two programming sequence, that is between the last data strobe transition of a programming sequence and the first data strobe transition of the next programming sequence.

The remaining 4 bits provide eleven frequency variations of one tywelfth of semitone and four variations of ±1/1000 and ± 2/1000 of semitone. (± 0.05% accuracy). Vibrato, glissando, chorus effect etc. can be easily implemented.

Table B and Table C show the 240 frequencies obtainable by setting the external clock to 4MHz (M114A) and 6MHz (M114AF) respectively with table lenght of 16 bytes, single reading and without inserting the octave divisor. These are the highest octave frequencies provided by the device. In practice double, quadruple, etc... frequencies may be obtained by writing 2, 4, etc. complete waveform periods in the table.

Lower frequencies can be generated by programming higher table lengths and/or repeated reading (see table E). The last 16 frequency codes are intended for test purposes and for special useful commands:

- forced-table-termination (FF hex code)
- frequency synchronization (F9, FA, FB, codes)

Figure 8 Microprocessor Interface Timing

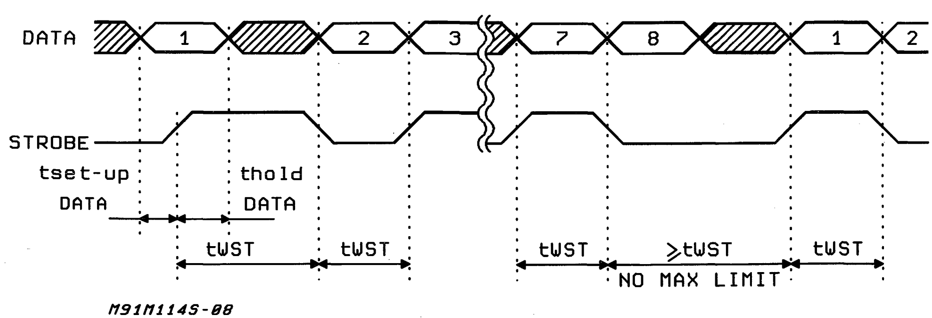


Table A: Data Programming Order

BYTE \ N. PIN	34	35	36	37	38	39
1st	ATTENUATION					
	A5	A4	A3	A2	A1	A0
2nd	4 OUTPUTS		TABLE 1 ADDRESS		TABLE 2 ADDRESS	
	1	0	7	6	7	6
3rd	TABLE 2 ADDRESS					
	5	4	3	2	1	0
4th	TABLE 1 ADDRESS					
	5	4	3	2	1	0
5th	TABLE LENGTH			READING METHOD		
	L2	L1	L0	M2	M1	M0
6th	INTERPOLATION				ENVELOPE EN/DISAB	OCTAVE DIVISOR
	3	2	1	0	0	0
7th	CHANNEL NUMBER				FREQUENCY	
	3	2	1	0	1	0
8th	FREQUENCY					
	7	6	5	4	3	2

– previously selected frequency (FC code)

– ROMID (F8 code)

These commands are explained elsewhere in detail.

Octave Divisor Bit (1bit)

This bit is used to pass from the octave to another without changing the table length. If octave divisor bit is set to 1 the programming frequency is divided by two.

Attenuator (6 bits)

These bits define the attenuation superimposed on all the signal samples produced by the selected channel. The six binary code (0 to 63) is interpreted as a dB value of attenuation (see table D). The programmed six bit code is internally decoded into a 10 bit linear value. After processing by a suitable circuit in order to obtain a gradual amplitude variation, the attenuation data is sent to the internal attenuator.

The only method to stop a running channel is to program into it the maximum attenuation code (63 = 3F Hex). Code 62 = 3E Hex states for max attenuation but it leaves the channel active.
Code 0 = 00 Hex states for no attenuation.

Amplitude Envelope Control Bit (1Bbit)

Enables/Disables an internal amplitude envelope generator. When set to 0 it orders instant passage from the present amplitude to that programmed. It happens as soon as the current waveform table scanning has finished.

If set to 1 the programmed attenuation value will be reached smootly starting from the current attenuation level. Again this smooth move takes place only after the current waveform table scanning has finished. If a FTT (Forced-Table-Termination) command is used then the attenuator update (either with the smooth move or not) will begin immediately.

Analog Output Pin Selection (2 bits)

These two bits indicate to which of the 4 analog output pins the corresponding channel signal must be forwarded. More than one channel (even all 16 channels) can be routed to the same output pin. The reconstructed analog signal will be the mix of all the single component signal. The availability of 4 outputs allows to obtain stereophonic effect or to separate channels used for accompanyment from those or "solo" etc.

1^. Table Address (8 bits)

These bits determine the most significant part of the starting address (13 bits) of the first waveform table (Tab.1) in external ROM. The remaining bits of the starting address are automatically set to logical zero (except when the table length is set to 16 byte: in this case the fifth bit is set to one, while the 4 LSB's are set to zero). Depending on the selected table length, some of these bits can be Don't Care bits.

2^. Table Address (8 bits)

Exactly as before, but referring to the second waveform table (Tab. 2)

Table Lenght And Reading Mode (6 bits)

These bits specify the length of the first waveform table, the length ratio between the two waveform tables, and their reading mode. A total of 58 distinct combinations are available. See table E.

The three most significant bits characterize the table lengths (from 16 samples up 2048 samples) while the other three characterize the length ratio between tables and the number of repeated readings.

Interpolation (4bits)
These bits define the interpolation coefficent between the two values read from the two waveform tables. This allows for the mixing of two programmed timbres in any integer ratio from 16/0 to 1/15.

The operation carried out is the following :

$D = (D1 * (K + 1)/16) + (D2 * (15 - K)/16)$ where :

- D is the data at the input of the DAC (8 bits in complement with 2)
- D1 is the data read from the 1^{st} table (8 bits in complement with 2)
- D2 is the data read from the 2^{nd} table (8 bits in complement with 2)
- K is a 4 bit interpolation coefficient (from 0 to 15)

Obviously only the first waveform will be output if K = 15. The first table can only assume a minimum percentage value of 1/16 of the max. value. To obtain only the second table values the first and the second table addresses must be exchanged. Another method to produce a sound with only one table would be to specify the same address for both the first and the second table programming parameters, and giving what ever interpolation coefficent you want, so effectively interpolating a table with itself.

F8 Hex: ROM-Identification
This command just sets the device frequency counters to a very short counting modulo, useless for musical purposes.

FC Hex: Previously Selected-Frequency
It is provided to ease writing the control program software for the M114A/AF

FF Hex: Forced-Table-Termination
This command allows a suddenly move from one table to another without waiting the end of the present table scanning. It simulates an end-of-table condition. A dedicated flip-flop is provided to service all the 16 channels

a pending FTT command is serviced according to the channel priority. (maximum delay of 32 μs at 4MHz clock). Note that each new programming sequence resets the flip-flop indicating "pending FFT", so to avoid losing the FTT command you need to wait at least that 32 μs, (24 μs in the M114AF) before issuing any new programming sequence after the FTT command. However, on average, it should be sufficient to wait only half that time.

Using this command you can store a whole new set of data (table addresses, table lenghts, reading modes, attenuation level, interpolation, etc.) except a new frequency value for that channel (nor a new value for the octave control bit). All the sound parameters of a channel can be changed without waiting for the end of the current first waveform table, if a normal programming sequence is issued immediately before the FTT command.

The normal programming sequence must contain the new frequency code + all other new sound parameters.

It is not possible to start a stopped channel with this command, because it has no frequency information within itself, so this command has an effect on a channel only if that channel is already running.

The FTT command is always performed on the first table address.
IMPORTANT - DO NOT USE THE FTT COMMAND SPECIFYING A CHANNEL WHICH IS

LAST SIXTEEN FREQUENCY CODES: SPECIAL COMMANDS
Among the last 16 frequency codes there are six intended for special commands

Freq. Code	Abbreviation	Command Explanation
F8 Hex	ROMID	ROM Identification
F9 Hex	RSG	Set-Synchro-Global
FA Hex	RSS	Reverse-Synchro-Status (only for next programming operation)
FB Hex	SSG	Reset-Synchro-Global (as after a hardware reset)
FC Hex	PSF	Previously Selected Frequency
FF Hex	FFT	Forced-Table-Termination

ACTUALLY STOPPED !
it has no effect on that channel but, it takes its effect on the NEXT normal command on a running channel

\# Using the FTT command in Delta coding it is impossible to maintain a zero mean value in the reconstructed signal. Though only for a short time a transient in the mean DC output level occurs, because the currently scanned table is terminated early at an unpredictable moment. This special command is intended for percussive sounds, or when working with waveform tables coded in absolute (PCM) mode, or for special effects.

\# This command can be useful to terminate instantaneously a sound: just program that channel with the FTT command, specifying maximum attenuation AND instantaneous variation of the attenuation.

ASYNCHRONOUS MODE

Normally the M114A/AF chip is working in asynchronous mode (set up at reset). In this working mode the programmed frequency becomes active immediately, without waiting for the running table to end while the table addresses and all the other parameters are changed only when the running table has been completely scanned (end of table condition).

This operative mode is useful for producing vibrato effects on long tables, thanks to the fact that some bytes of the previously programmed table will be read at the newly programmed frequency rate.

SYNCHRONOUS MODE

It is possible to synchronize the frequency change with the end of the first waveform table, so avoiding to read a table in part with the old frequency and in part with the new one.

This way-to-operate is useful in the reproduction of deep vibrato on notes placed at the octave boundary, for glide effects and in any case when it is necessary to go beyond the octave boundary without discontinuity (to avoid clicks).

The commands for synchronization are:

SSG F9 Hex: SET-SYNCHRO-GLOBAL
Activates the global synchronous mode (frequency change at the table end).

RSG FB Hex: RESET-SYNCHRO-GLOBAL
This command disables the global synchronous mode.

RSS FA Hex: REVERSE-SYNCHRO-STATUS
This command inverts the synchronism state only for the next programming sequence.

Everyone of these commands is accomplished by sending a complete programming sequence with F9/FA/FB frequency codes respectively.

They affect the whole working mode of the device (all its channels). All the remaining bits are ignored.

Note that RSS command can be obtained by sending eight times the 6-bit data 111110.

WAVEFORM TABLES ADDRESS

In the programming sequence there are 8 + 8 bits devoted to forming the addresses of the 1^ and 2^ waveform tables from each of which a byte is read into the chip to form a single output sample.

The basic address space for waveform tables is 8 Kbytes, as there are 13 address lines managed by the chip. With external circuitry the address space can be doubled. The 8 + 8 bits in the programming sequence only define the starting addresses of the two tables.

The M114A/AF forms addresses according to the table lengths and the reading mode.

The principle is very simple: given a table length the M114A/AF will automatically managed a corresponding number of least significant bits to step from all zero to all ones in a binary sequence, while the remaining most significant bits of the address will be taken from the MSB's of the eight bit code programmed for that table.

In most cases some of eight programmed bits are Don't Care bits. The following examples can better explain how the addresses are generated.

1° EXAMPLE

Suppose TAB 1 = 32 bytes long, then the 5 LSB bits will be managed by the M114A/AF while the remaining 13 – 5 = 8 MSB bits will be exactly those programmed as the first table address.

Let be TAB1 (7:0) = 11111100 then the address sequence is:

11111100	00000	(start address = 1F80 Hex)
11111100	00001	
11111100	00010	
11111100	11101	
11111100	11110	
11111100	11111	(table termination) (last address = 1F9F Hex)
11111100	00000	(start address = 1F80 Hex)
11111100	00001	
etc.		

If the chosen read mode requires the first table be read 2 or 4 times, then each address will be repeated along 2 or 4 consecutive "service cycles" before skipping to the next address.

The same applies in making the second table address.

2° EXAMPLE

If TAB 1 = 16 bytes long, then the 4 LSB bits will be managed by the M114A/AF, THE FIFTH BIT WILL BE ALWAYS SET AT LOGIC ONE, while the remaining 13 – 5 = 8 MSB bits will be exactly those programmed as the first table address.

Let be TAB1 (7:0) = 11001100 then the address sequence is:

11001100	1	0000	(start address = 1990 Hex)
11001100	1	0001	
11001100	1	0010	
11001100	1	1101	
11001100	1	1110	
11001100	1	1111	(table termination) (last address = 199F Hex)
10011100	1	0000	(start address = 1990 Hex)
11001100	1	0001	
etc.			

If the chosen read mode requires the first table be read 2 or 4 times, then each address will be repeated along 2 or 4 consecutive "service cycles" before skipping to the next address.

The same applies in making the second table address.

3° EXAMPLE

If TAB 1 = 64 bytes long, then the 6 LSB bits will be managed by the M114A/AF while the remaining 13 – 6 = 7 MSB bits will be exactly the 7 MSB bits of the eight programmed as the first table address and the LSB bits is discarded (it is a Don't Care bit).

Let be TAB1 (7:0) = 1010110X then the address sequence is:

1010110	000000	(start address = 1580 Hex)
1010110	000001	
1010110	000010	
1010110	111101	
1010110	111110	
1010110	111111	(table termination) (last address = 15BF Hex)
1010110	000000	(start address = 1580 Hex)
1010110	000001	
etc.		

If the chosen read mode requires the first table be read 2 or 4 times, then each address will be repeated along 2 or 4 consecutive "service cycles" before skipping to the next address.

The same applies in making the second table address.

4° EXAMPLE

If TAB 1 = 2048 bytes long, then the 11 LSB bits will be managed by the M114A/AF while the remaining 13 – 11 = 2 MSB bits of the eight programmed as the first table address and the other 6 LSB bits are discarded (they are a Don't Care bits).

Let be TAB1 (7:0) = 10XXXXXX then the address sequence is:

10	00000000000	(start address = 1000 Hex)
10	00000000001	
10	00000000010	
10	11111111101	
10	11111111110	
10	11111111111	(table termination) (last address = 17FF Hex)
10	00000000000	(start address = 1000 Hex)
10	00000000001	
etc.		

If the chosen read mode requires the first table be read 2 or 4 times, then each address will be repeated along 2 or 4 consecutive "service cycles" before skipping to the next address.

The same applies in making the second table address.

5° EXAMPLE

Choose the six bits of table length and read mode as follow:

M (2:0) = 100 L (2:0) = 001

As you can see from TABLE E this corresponds to:

TAB1 = 32, each byte being read once
TAB2 = 16, each byte being read twice

Let be TAB1 (7:0) = 11100010 and TAB2 (7:0) = 00110011 then the address sequences for the two tables are:

TAB 1			TAB 2			
11100010	00000	(1C40 Hex)	00110011	1	0000	(0670 Hex) (start)
11100010	00001		00110011	1	0000	
11100010	00010		00110011	1	0001	
11100010	00011		00110011	1	0001	
11100010	00100		00110011	1	0010	
11100010	00101		00110011	1	0010	
11100010	11100		00110011	1	1110	
11100010	11101		00110011	1	1110	
11100010	11110		00110011	1	1111	
11100010	11111	(1C5F Hex)	00110011	1	1111	(067F Hex) (1 table termination)
11100010	00000	(1C40 Hex)	00110011	1	0000	(0670 Hex) (start)
11100010	00001		00110011	1	0000	
11100010	00010		00110011	1	0001	
11100010	00011		00110011	1	0001	
etc.						

SUMMARY

1) The waveform tables whose length is 16 (and also in the special cases when they are 8 or 4 bytes long), must begin at memory location multiple of 32 plus an offset of 16, i.e. the starting address must satisfy the equation [16 + n.32] with n = 0, 1, 2,...

2) The Waveform tables whose lengths is 32, 64,..., 1024, 2048, (i.e. their lenghts 2^ K with K = 5, 6..., 10, 11) must begin at memory locations multiple of 2^ K, that is, the starting address must satisfy the equation [n. 2^ K] with n=0, 1, 2, ...

TABLE B - FREQUENCIES (fosc = 4MHz) M114A

Note	Deviation	– 6/12	– 5/12	– 4/12	– 3/12	– 2/12	– 1/12	– 2/1000	– 1/1000
	(hex)	0	1	2	3	4	5	6	7
C	0	1016.78	1021.45	1026.69	1031.46	1036.27	1041.67	1044.39	1045.48
C#	1	1077.01	1082.25	1087.55	1092.90	1098.30	1103.14	1106.81	1107.42
D	2	1140.90	1146.79	1152.07	1158.08	1163.47	1168.91	1172.33	1173.71
D#	3	1209.19	1215.07	1221.00	1226.99	1232.29	1238.39	1242.24	1243.78
E	4	1281.23	1287.00	1293.66	1299.55	1305.48	1312.34	1315.79	1317.52
F	5	1356.85	1363.33	1369.86	1376.46	1383.13	1389.85	1393.73	1395.67
F#	6	1437.81	1445.09	1451.38	1458.79	1466.28	1472.75	1478.20	1479.29
G	7	1523.23	1530.22	1538.46	1545.60	1552.80	1560.06	1564.95	1566.17
G#	8	1614.21	1622.06	1629.99	1638.00	1644.74	1652.89	1658.37	1659.75
A	9	1709.40	1781.21	1727.12	1734.61	1743.68	1751.31	1757.47	1759.01
A#	A	1811.59	1819.84	1829.83	1838.24	1846.72	1855.29	1860.47	1862.20
B	B	1919.39	1928.64	1937.98	1947.42	1956.95	1966.57	1972.39	1974.33
2C	C	2032.52	2042.90	2053.39	2063.98	2072.54	2083.33	2087.68	2089.86
2C#	D	2155.17	2164.50	2176.28	2185.79	2195.39	2207.51	2212.39	2214.84
2D	E	2283.11	2293.58	2304.15	2314.81	2325.58	2339.18	2344.67	2347.42
	F	Testing	Testing	Testing	Testing	Testing	Testing	Testing	Testing

Note	Deviation	0	+ 1/1000	+ 2/1000	+ 1/12	+ 2/12	+ 3/12	+ 4/12	+ 5/12
	(hex)	8	9	A	B	C	D	E	F
C	0	1046.57	1047.67	1048.77	1051.52	1056.52	1061.57	1066.67	1071.81
C#	1	1108.65	1109.88	1111.11	1114.21	1119.19	1124.86	1130.58	1135.72
D	2	1174.40	1175.78	1177.16	1180.64	1186.24	1191.90	1197.60	1203.37
D#	3	1244.56	1245.33	1246.88	1250.78	1256.28	1262.63	1269.04	1274.70
E	4	1318.39	1319.26	1321.00	1324.50	1331.56	1337.79	1344.09	1350.44
F	5	1396.65	1397.62	1398.60	1403.51	1410.44	1417.43	1424.50	1430.62
F#	6	1480.38	1481.48	1482.58	1486.99	1494.77	1501.50	1508.30	1516.30
G	7	1567.40	1568.63	1569.86	1576.04	1583.53	1591.09	1598.72	1606.43
G#	8	1661.13	1662.51	1663.89	1669.45	1677.85	1684.92	1693.48	1702.13
A	9	1760.56	1762.11	1763.89	1768.35	1777.78	1785.71	1793.72	1803.43
A#	A	1863.93	1865.67	1867.41	1874.41	1883.24	1892.15	1901.14	1910.22
B	B	1976.28	1978.24	1980.20	1984.13	1994.02	2004.01	2014.10	2024.29
2C	C	2092.05	2094.24	2096.44	2103.05	2114.16	2123.14	2134.47	2143.62
2C#	D	2217.29	2219.76	2222.22	2227.17	2239.64	2249.72	2259.89	2272.73
2D	E	2350.18	2352.94	2355.71	2361.28	2372.48	2383.79	2395.21	2406.74
	F	ROMID	SSG	RSS	RSG	Previously Selected Frequency	Testing	Testing	Forced Table Terminat.

TABLE C - FRQUENCIES (fosc = 5.99456 MHz) M114AF

Note	Deviation	– 6/12	– 5/12	– 4/12	– 3/12	– 2/12	– 1/12	– 2/1000	– 1/1000
	(hex)	0	1	2	3	4	5	6	7
G	0	1523.78	1523.79	1538.64	1545.79	1552.99	1561.08	1565.16	1566.80
G#	1	1614.04	1621.90	1629.84	1637.86	1645.95	1653.22	1658.71	1659.62
A	2	1709.80	1718.62	1726.54	1735.54	1743.62	1751.77	1758.91	1758.97
A#	3	1812.14	1820.95	1829.84	1838.82	1846.75	1855.90	1861.66	1863.98
B	4	1920.10	1928.75	1938.73	1947.55	1956.45	1966.72	1971.89	1974.49
2C	5	2033.43	2043.14	2052.93	2062.82	2072.82	2082.89	2088.70	2091.61
2C#	6	2154.77	2165.66	2175.09	2186.20	2197.42	2207.13	2215.28	2216.92
2D	7	2282.77	2293.25	2305.60	2316.29	2327.08	2337.97	2345.29	2347.13
2D#	8	2419.11	2430.88	2442.77	2454.77	2464.87	2477.09	2485.31	2487.37
2E	9	2561.78	2574.98	2588.32	2599.55	2613.15	2624.59	2633.81	2636.13
2F	A	2714.93	2727.28	2742.25	2754.85	2767.57	2780.41	2788.17	2790.76
2F#	B	2876.47	2890.34	2904.34	2918.48	2932.76	2947.18	2955.90	2958.82
2G	C	3046.02	3061.57	3077.29	3093.17	3105.99	3122.17	3128.68	3131.95
2G#	D	3229.83	3243.81	3261.46	3275.72	3290.10	3308.26	3315.58	3319.25
2A	E	3421.55	3437.25	3453.09	3469.07	3485.21	3505.59	3513.81	3517.93
	F	Testing	Testing	Testing	Testing	Testing	Testing	Testing	Testing

Note	Deviation	0	+ 1/1000	+ 2/1000	+ 1/12	+ 2/12	+ 3/12	+ 4/12	+ 5/12
	(hex)	8	9	A	B	C	D	E	F
G	0	1568.44	1570.08	1571.73	1575.86	1583.35	1590.91	1598.55	1606.26
G#	1	1661.46	1663.31	1665.16	1669.79	1677.27	1685.76	1694.34	1702.03
A	2	1760.00	1762.07	1764.14	1769.35	1777.75	1786.22	1794.78	1803.42
A#	3	1865.14	1866.30	1868.63	1874.47	1882.71	1892.22	1901.83	1910.31
B	4	1975.79	1977.10	1979.71	1984.95	1995.53	2004.87	2014.30	2023.82
2C	5	2093.07	2094.54	2096.00	2103.35	2113.74	2124.22	2134.81	2143.98
2C#	6	2218.56	2220.21	2221.85	2228.46	2240.12	2250.21	2260.39	2272.39
2D	7	2348.97	2350.81	2352.65	2361.92	2373.14	2384.47	2395.91	2407.45
2D#	8	2489.44	2491.50	2493.58	2501.90	2514.50	2525.09	2537.92	2550.88
2E	9	2638.45	2640.78	2643.10	2650.11	2664.25	2676.14	2688.14	2702.69
2F	A	2793.06	2795.97	2798.58	2809.07	2822.30	2835.65	2849.13	2862.73
2F#	B	2961.74	2964.67	2967.60	2973.49	2988.31	3003.29	3018.41	3033.68
2G	C	3135.23	3138.51	3141.80	3151.71	3168.37	3181.83	3198.80	3212.52
2G#	D	3322.93	3326.61	3330.31	3337.73	3356.42	3371.52	3386.76	3406.00
2A	E	3522.07	3526.21	3530.37	3538.70	3555.49	3572.44	3589.56	3606.84
	F	ROMID	SSG	RSS	RSG	Previously Selected Frequency	Testing	Testing	Forced Table Terminat.

TABLE D - ATTENUATION

N = six bit attenuation code decimal value (0:63)
V = internally decoded linear ten bit value (0:1023)
A = theoretical attenuation value in decibels
= 20 . Log ((V + 1)/1024)

N	V	A
0	1023	0.00
1	939	0.74
2	863	1.48
3	791	2.23
4	727	2.96
5	667	3.71
6	611	4.47
7	559	5.24
8	515	5.95
9	471	6.73
10	431	7.50
11	395	8.25
12	363	8.98
13	335	9.68
14	307	10.43
15	283	11.14
16	259	11.91
17	235	12.75
18	215	13.52
19	199	14.19
20	183	14.91
21	166	15.75
22	152	16.51
23	140	17.22
24	128	17.99
25	117	18.77
26	107	19.54
27	98	20.29
28	90	21.03
29	83	21.72
30	76	22.48
31	69	23.30
.	.	.
.	.	.
.	.	.
63	0	STOP

TABLE E - READING MODES

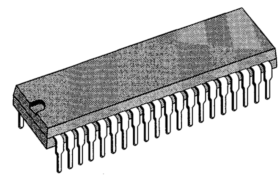
Mode M	Mode L	Length T1	Length T2	Read N. T1	Read N. T2
000	000	16	16	2	2
000	001	32	32	2	2
000	010	64	64	2	2
000	011	128	128	2	2
000	100	256	256	2	2
000	101	512	512	2	2
000	110	1024	1024	2	2
000	111	2048	1048	2	2
001	000	16	16	1	1
001	001	32	32	1	1
001	010	64	64	1	1
001	011	128	128	1	1
001	100	256	256	1	1
001	101	512	512	1	1
001	110	1024	1024	1	1
001	111	2048	2048	1	1
010	000	16	16	4	4
010	001	32	32	4	4
010	010	64	64	4	4
010	011	128	128	4	4
010	100	256	256	4	4
010	101	512	512	4	4
010	110	1024	1024	4	4
010	111	1024*	1024	4	4
011	000	16	16$	1	1
011	001	32	32	1	1
011	010	64	64	1	1
011	011	128	128	1	1
011	100	256	256	1	1
011	101	512	512	1	1
011	110	1024	1024	1	1
011	111	2048	2048	1	1

Mode M	Mode L	Length T1	Length T2	Read N. T1	Read N. T2
100	000	16	8	1	2
100	001	32	16	1	2
100	010	64	32	1	2
100	011	128	64	1	2
100	100	256	128	1	2
100	101	512	256	1	2
100	110	1024	512	1	2
100	111	2048	1024	1	2
101	000	16	16$	1	1
101	001	32	16$	1	1
101	010	64	16	1	1
101	011	128	32	1	1
101	100	256	64	1	1
101	101	512	128	1	1
101	110	1024	256	1	1
101	111	2048	512	1	1
110	000	16	4	1	4
110	001	32	8	1	4
110	010	64	16	1	4
110	011	128	32	1	4
110	100	256	64	1	4
110	101	512	128	1	4
110	110	1024	256	1	4
110	111	2048	512	1	4
111	000	16	16$	1	1
111	001	32	16$	1	1
111	010	64	16$	1	1
111	011	128	16	1	1
111	100	256	32	1	1
111	101	512	64	1	1
111	110	1024	128	1	1
111	111	2048	256	1	1

* REPETITION
$ EXCEPTION

DIGITAL SOUND GENERATOR

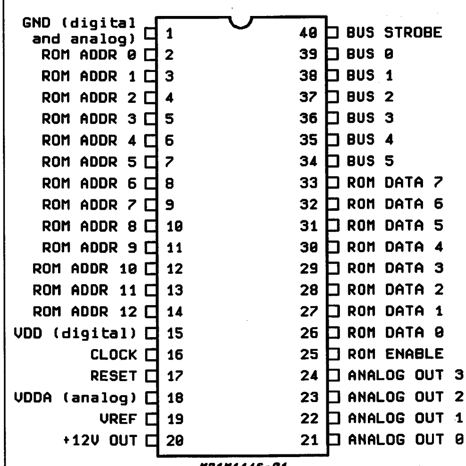
- INPUT CLOCK FREQ: 4MHz (M114S)
  6MHz (M114SF)
- SOUND GENERATED BY READING TABLES CODED IN DELTA CODING OR IN ABSOLUTE VALUES SITUATED IN AN EXTERNAL MEMORY OF 16 K MAX
- 16 INDEPENDENT CHANNELS
- 12 BIT EQUIVALENT D/A CONVERTER RESOLUTION (delta coding)
- 8 DIFFERENT TABLE LENGTHS AND 8 READING MODES GIVING A TOTAL OF 58 DISTINCT COMBINATIONS
- 16 DIFFERENT MIXABLE LAYERS BETWEEN TWO SEPARATE TABLES
- MULTIPLE READING PERMITS INTERPOLATION BETWEEN TWO ADJOINING SAMPLES ON THE SAME TABLE
- 4 SELECTABLE ANALOG OUTPUTS
- 10 BIT INTERNAL ATTENUATOR WITH GRADUAL AMPLITUDE VARIATION
- ROM ENABLE OUTPUT TO MINIMISE EXTERNAL MEMORY POWER CONSUMPTION
- POSSIBILITY OF SYNCHRONOUS AND ASYNCHRONOUS FREQUENCY-TABLE CHANGE AT THE END OF THE READING TABLE



DIP40

ORDERING NUMBERS: M114S1
M114SF (6MHz version)

PIN CONNECTION (Top wiew)



The M114S/SF is a 16 channel digital polyphonic, politimbric sound generator designed for electronics musical instruments.

It is available in two versions, differing in the clock speed: M114S (4MHz input clock frequency) and M114SF (6MHz)

The M114S/SF must be driven by a microprocessor and needs an external memory.

With this device it is possible to synthesize a large range of sounds by simply transcribing the most significant periods of the sound to be reproduced into an external memory and programming a suitable reading sequence for these periods with the use of a microprocessor.

The M114S/SF is realized on a single monolithic silicon chip using low threshold N-channel silicon gate MOS technology and is assembled in plastic DIP 40.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	0.3 to + 7	V
V_I	Input Voltage	0.3 to V_{DD}	V
V_O	Output Voltage	0.3 to V_{DD}	V
P_{tot}	Total Package Power Dissipation	1000	mW
T_{stg}	Storage Temperature	– 40 to + 150	°C
T_{op}	Operating Temperature	0 to + 60	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the oparetional sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

THERMAL DATA

Symbol	Description	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient max.	100	°C/W

Figure 1. Block Diagram

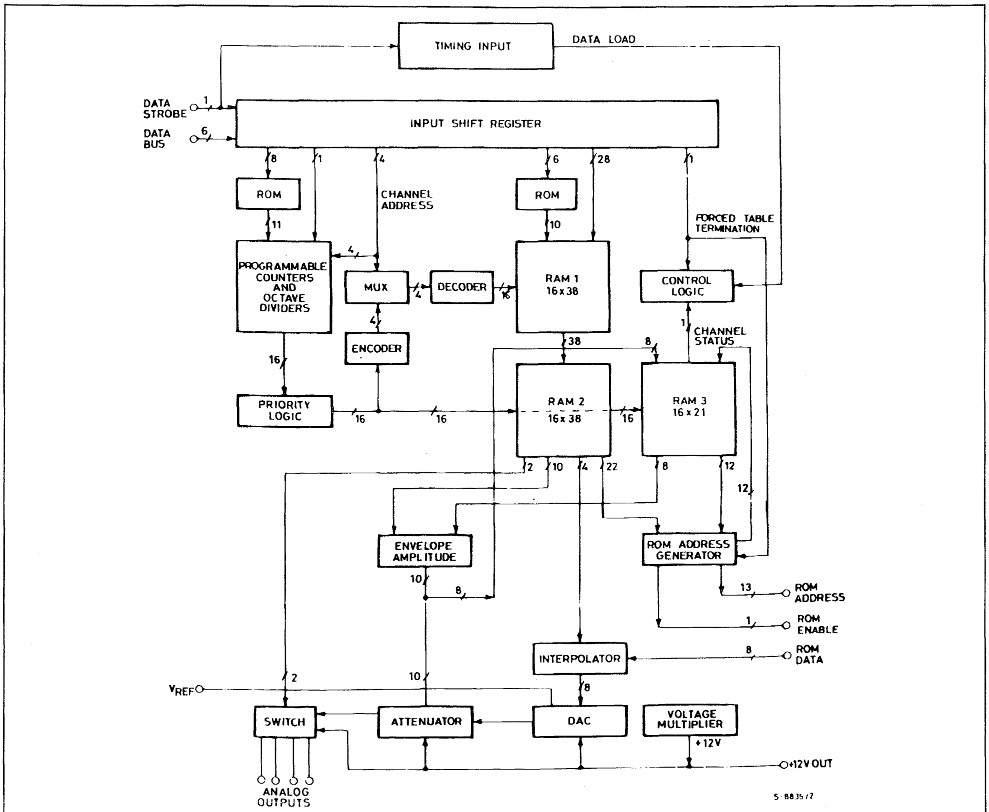
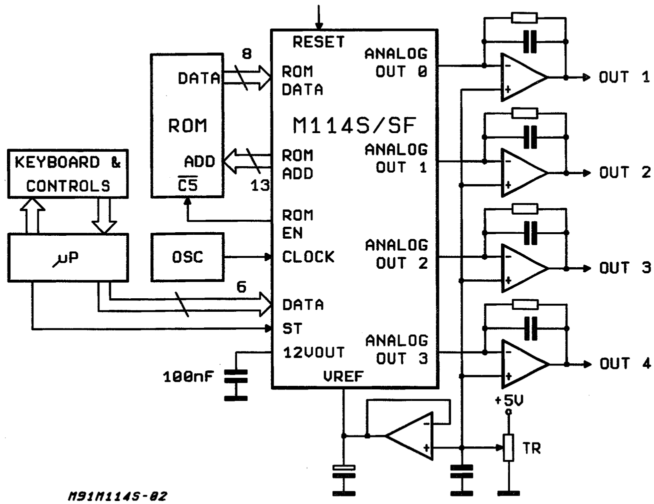


Figure 2: System Configuration



STATIC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 5 %, T_{amb} = 25 °C, V_{DD} = V_{DDA} analog)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
INPUTS: RESET (pin 17), CLOCK (pin 16), ROM DATA (pins 26-33), DATA BUS (pins 34-39), DATA ST. (pin 40)						
V_{IL}	Low Input Level				0.8	V
V_{IH}	High Input Level		2.2			V
I_I	Input Leakage Current	V_I = V_{DD} to GND			± 1	µA
DIGITAL OUTPUTS: (high impedance*): ROM-ADD (pins 2-14) ROM-EN (pin 25)						
V_{OL}	Low Output Level	I_{OL} = 1 mA			0.4	V
V_{OH}	High Output Level	I_{OH} = 100 µA	2.4			V
ANALOG OUTPUTS: (pins 21, 22, 23, 24), V_{REF} (pin 19)						
V_{REF}	Voltage Reference Output	I_O = ± 1mA	2.4	2.5	2.6	V
I_O	Output Current (current generator)	Zero Attenuation Max Input Code to the DAC		± 1		mA
POWER DISSIPATION						
I_{DD}	Supply Current Digital	V_{DD} = 5.25V f = 4MHz (M114S) V_{DD} = 5.25V f = 6MHz (M114SF)		100 100	120 130	mA mA
I_{DDA}	Supply Current Analog	V_{DDA} = 5.25V		5	10	mA

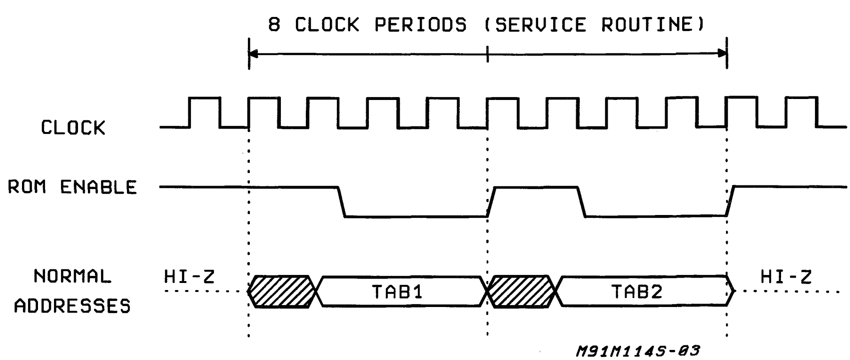
* High impedance means that, when the addresses are off, the digital output is connected with an internal resistive pull-up of 10kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 5 %, T_{amb} = 25 °C, V_{DD} = V_{DDA})

Symbol	Parameter	Test Conditions	Value						Unit
			M114S			M114SF			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CLOCK									
t_{CK}	Input Clock Frequency			4.000			6000		kHz
t_r, t_f	Rise and Fall Time	10 % to 90 %			20			15	ns
t_{WH}, t_{WL}	High and Low Pulse Width		90			60			ns
RESET									
t_{wRES}	Pulse Width		10			6			ms
t_f	Fall Time	10 % to 90 %			20			15	ns
DATA BUS									
$t_{w\ DATA}$	Pulse Width		1250			830			ns
$t_{set\text{-}up\ DATA}$	Set-up Time to Data Strobe		0			0			ns
$t_{hold\ DATA}$	Hold Time from Data Strobe		1250			830			ns
DATA STROBE									
t_{WST}	Pulse Width		1.5		128	1		85	µs
t_{WRST}	Pulse Width for Internal Reset Generation		128			85			µs
t_f	t_r	Pulse and Fall Times			40			20	ns
ROM ENABLE (see fig. 3)									
t_{LOW}				600			400		ns
t_{HIGH}				350			220		ns
$t_{set\text{-}up\ EN}$(*)	Set-up Time ROM-EN		70			55			ns

(*) $t_{set\text{-}up\ EN}$. Time means that the data coming from ext. ROM must be stable at least 70ns before the rising edge of ROM enable.

Figure 3: Memory Read/Write Timing



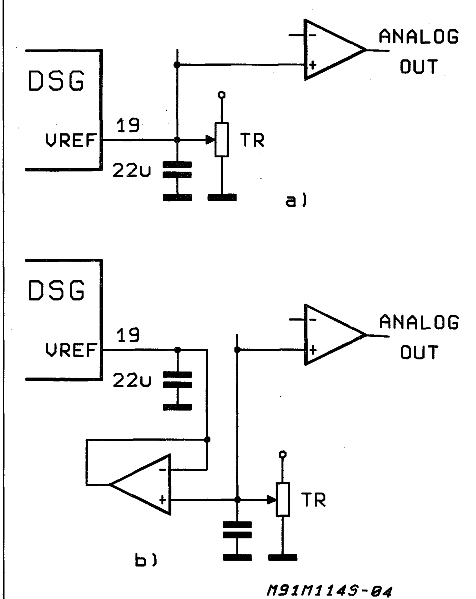
PIN FUNCTIONS

PIN 1 - GND (Analog and Digital)
Analog ground and digital ground are both linked to this pin.

PINS 21-24 - ANALOG OUTPUTS
These outputs are under current with an output impedance of approximately 1 KΩ and the filter or external integrator must have a low input impedance. This means that the voltage drop between output pin and V_{REF} must be negligeable so as to obtain a good signal linearity. An integrator is necessary if the tables have been "DELTA" coded. If on the other hand they have been coded in absolute values then only a low pass filter is needed.

PIN 19 - VOLTAGE REFERENCE OUTPUT (V_{REF})
V_{REF} is the average value of the DAC output. With V_{supply} = 5 V V_{REF} is nominally 2.5 V but could vary by chip to chip (± 100 mV). At the integrator output the DC level can change when channel turns-on or turns-off. To minimize this drop it is necessary to trim the value of V_{REF} by TR trimmer (fig. 4A, 4B). The solution of fig 4B is more efficent than that in fig.4A: in fact the behavoir is as better as less is the seen impedance at the V_{REF} pin.

Figure 4.



PIN 18 - ANALOG POWER SUPPLY
The power supply for all analog parts, i.e. DAC, attenuator, etc ...., are linked to this pin. It is therefore important that this power supply should be very stable and well smoothed. The internal power supply chip separation allows a great improvement of signal/noise ratio.

PIN 15 - DIGITAL POWER SUPPLY
The power supply for all digital parts, i.e. counters, memories, etc ...., are linked to this pin.

PIN 17 - RESET
All channels are reset by rising this pin. The 13 external ROM address outputs together with the 4 sound outputs are placed in a high impedance state.

PIN 16 - CLOCK 4 MHz (M114S), 6 MHz (M114SF)
For correct functioning the duty cycle must be very close to 50 %. Internal circuits are dynamic, so the clock is continuously required to mantein internal information.

PIN 20 (+ 12 V out)
This pin is the output of an internal voltage elevator and it needs of an external filtering capacitance (min. 100 nF). The performance of DAC and attenuator are very improved with an external zener that clamps the voltage elevator output (see fig. 5).

PINS 2 & 14 - ROM-ADDRESS
13 PUSH-PULL type output pins for external memory address (8k Bytes).

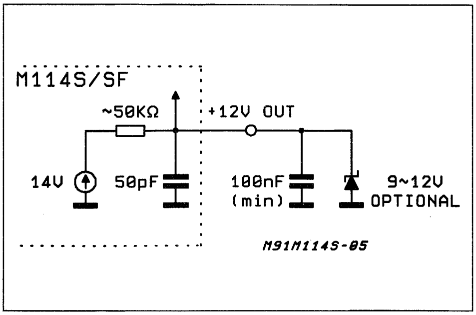
PINS 25 - ROM-ENABLE (Low active)
This is a PUSH-PULL type output and is used to set the external memory in stand-by so as to reduce consumption whenever it is not read. It is possible to double the addressable memory size (16 Kbyte by connecting this pin to the MSB address line of the external memory thru a Flip-Flop).

PINS 26 & 33 - ROM-DATA
8 input pins for data from external memory.

PINS 34-39 - DATA-BUS
6 input pins for data from the microprocessor. 8 of these data groups make up a complete piece of information (48 bit).

PIN 40 - DATA-BUS STROBE
A signal from the microprocessor must arrive at this input in order to memorise the present code onto the DATA-BUS. Memorization occurs on both edges.

Figure 5



GENERAL DESCRIPTION

The M114S/SF is a device that allows digital sound synthesis. The essential system needed consists of a microprocessor, an M114S/SF and an external memory with a maximum of 8192 bytes (16Kbytes by use of an external Flip-Flop - See fig.6). Sound generation is based on cyclic reading of tables corresponding to waveforms (periods) of the timbre to be reproduced.

As the waveform and therefore also the spectrum frequently change, a series of tables of form and frequency appropriate to the sound are cyclically scanned during sound reproduction.

The effect caused by the sudden passage from one table to the next would be unpleasant unless there is such a large number of tables to allow a smooth unnoticeable change from one table to the following.

A favourable compromise between number of tables and quality of sound, that has been implemented in the M114S/SF is the following : a limited number of tables which may even diverge from one another are chosen during an initial phase of analysis after which, during the reproduction phase, always two tables are read simultaneously by extracting a percentage of one and the remaining percentage of the other.

Therefore by starting with 100 % of one and zero of the other and successively increasing the second while decreasing the first, a smooth passage is achieved. In the M114S/SF this passage is made up of a maximum of 16 steps.

The tables are stored in an external memory and may be of eight different lengths ranging from 16 to 2048 bytes. The tables may be coded using waveform's absolute value or by the difference between adjoining samples, that is, in a incremental manner (Delta coding). The table samples must be in 8 bits format, complement with 2. The Delta coding increases the equivalent resolution. The typical resolution is 12 bit with a sinusoidal wave coded in a 16-byte table.

OUTPUT RECONSTRUCTION

An external low pass filter (absolute value coding) or an integrator (Delta coding) are sufficient to reconstruct the original sound. The difference is only the value of the feedback network. The Delta coding allows easy interpolation. By simply reading the same data n time and dividing the amplitude of each reading by n, a ramp of n small steps is obtained instead of a large single step. The value of n may be 1, 2 or 4.

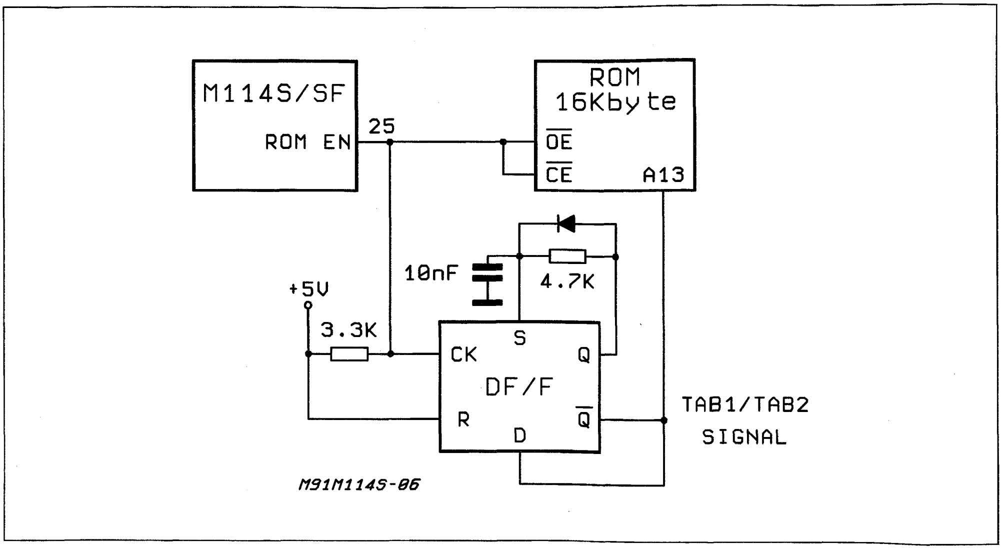
When a waveform is coded in this way (Delta-Coding or incrementally), the sum of the samples in an entire period must always be equal to zero or there would be a DC offset which could even saturate the external integrator.

The frequency of the generated samples is a whole multiple of the table lenght. In this way any problem caused by intermodulation is eliminated but a noise due to "collision" is produced. As there is a single output circuit for all channels, (interpolar, D/A converter, attenuator, ecc.), each time more than one channel requires access to these circuits one, or more, other channel must wait.

The amount of time necessary for the output circuit to process each table, that is the period of time for which each channel uses the circuit during each sample reading cycle, is of 2 µs for the M114S (1.5 µs for the M114SF). The delay will therefore be proportional to the number of channels operating simultaneously and to the frequency that they are generating. As these parameters casually vary, so will the delay thus producing a casual alteration of the original waveform. ("collision noise") Simulation has proved that under worst possible conditions the signal/noise ratio due to this problem is around 60 dB.

The sound amplitude envelope has to be controlled by the microprocessor which, at suitable intervals, must forward the desired attenuation coefficient. There are 64 possible attenuations each with steps of approximately 0.75 dB ; These passage from one level to another may be immediate or to gradual increments of 1/256 of the maximum amplitude at a frequency proportional to external table reading frequency.

Figure 6: The M114S/SF can handle up to 16Kbyte of memory with this application circuit



OPERATION

The M114S/SF receives from the µP a single programming sequence at a time. This programming sequence is made up of 48 bits. The µP must send a 48 bit set for every M114S/SF active channel (16 independent channels). Each M114S/SF channel continuously generates the same signal: it reads the same table, with the same mixing coefficient, with the same amplitude, ecc., until the microprocessor forwards a different programming sequence (variation of one or more parameters characterising the sound to be generated within a single channel). Timbre amplitude evolution and any other slight frequency changes must be handled in real-time by the microprocessor.

Each channel reads two samples from two tables, at the sampling frequency, sums them according to the mixing coefficient and forwards the result to the DAC whose suitably attenuated output goes to the previously selected output pin (fig. 7).

This operation requires 2 µs (1.5 µs in the M114SF) and as there is a single output circuit for all channels it is certain that one or more channels will simultaneously request the use of the circuit. Thus a priority order has been assigned to each channel.

This order is fixed: channel zero has greatest priority followed in order by the others. When more than one channel is simultaneously active at the output pin there will be an overlap of impulses (the impulse of the lower priority channel will be delayed) The example of Fig.8 shows an output signal with 2 active channels, CH1 has greater priority then CH2:

Figure 7

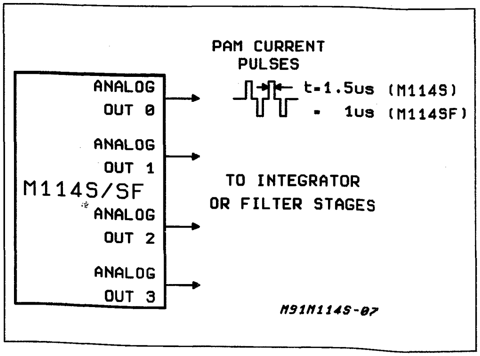
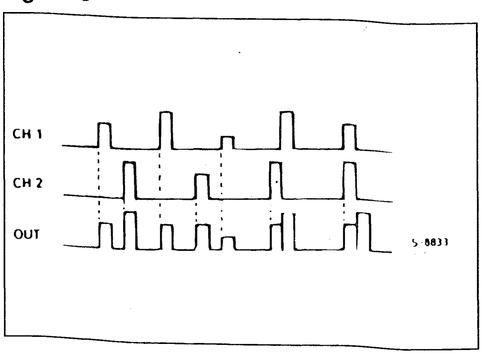


Figure 8



The signal will change from impulsive to continuous by passing through:

- a low pass filter if the table have been coded using absolutes values.
- an integrator if in delta coding

AMPLITUDE ENVELOPE GENERATOR

When the microprocessor programs one channel with a new attenuation level, different from the preceding one, this new level can be reached immediately or by a smooth move (depends from the setting of the amplitude control bit described elsewhere). The M114S/SF envelope generator only controls and changes the 8 MSB among the 10 bit of the attenuation code. The gradual movement from the present level to that just programmed takes place by increasing or decreasing these 8 MSB of attenuation with the same frequency with which the external memory tables are being scanned if the difference in level is greater than 128 steps, or with 1/2 of this frequency if greater than 64 steps or 1/4 if greater than 32, or 1/8 if smaller than or equal to 32.

INPUT INTERFACE WITH THE MICROPROCESSOR

The M114S/SF has been designed to easily interface with every microprocessor. The microprocessor interface has a 6-bit data bus and a single control line, the DATA strobe. 48 bits subdivided into 8 groups of 6 bit each must be forwarded in order to programme a single channel.

A group of 6 bits is memorized on every data STROBE switch front. As the data bus is read approximately 250ns after strobe transition, the 6 data bits may be sent simultaneously with the strobe. The whole set of 48 bit have to be entered for any channel programming operation. The entering order is indicated in table A.

MEANING OF THE 48 PROGRAMMABLE BITS IN THE PROGRAMMING SEQUENCE

Channel Address (4 bits)

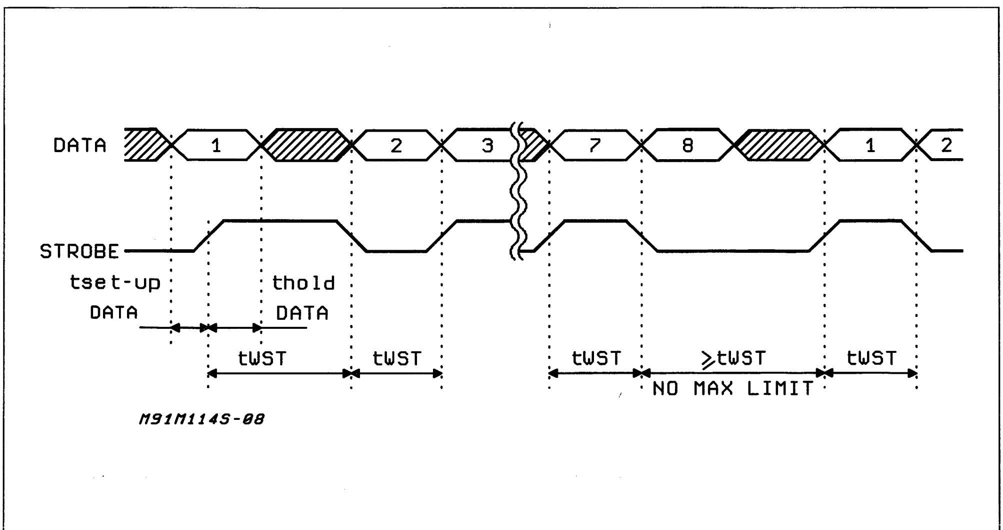
These four bits indicate to which of the 16 M114S/SF channel the remaining 44 bits will be forwarded.

Frequency Code (8 bits)

The 4 most significant bits cover 15 semitones (HEX code from 0 to E) The graph of fig. 9 shows the time lapse that must be assigned to these signal for correct functioning. No more than 128 μs (85 in the M114SF) must pass between one data Strobe transition and the next during transmission of the 8 groups of data or else synchronization is lost due to the device internal automatic reset.

There is no upper limit for the elapsed time between two programming sequence, that is between the last data strobe transition of a programming sequence and the first data strobe transition of the next programming sequence.

Figure 9 Microprocessor Interface Timing



DATA PROGRAMMING ORDER

BYTE \ N. PIN	34	35	36	37	38	39
1st	ATTENUATION					
	A5	A4	A3	A2	A1	A0
2nd	4 OUTPUTS		TABLE 1 ADDRESS		TABLE 2 ADDRESS	
	1	0	7	6	7	6
3rd	TABLE 2 ADDRESS					
	5	4	3	2	1	0
4th	TABLE 1 ADDRESS					
	5	4	3	2	1	0
5th	TABLE LENGTH			READING METHOD		
	L2	L1	L0	M2	M1	M0
6th	INTERPOLATION				ENVELOPE EN/DISAB.	OCTAVE DIVISOR
	3	2	1	0	0	0
7th	CHANNEL NUMBER				FREQUENCY	
	3	2	1	0	1	0
8th	FREQUENCY					
	7	6	5	4	3	2

The remaining 4 bits provide eleven frequency variations of one tywelfth of semitone and four variations of ±1/1000 and ±2/1000 of semitone. (±0.05% accuracy). Vibrato, glissando, chorus effect etc. can be easily implemented.

Table B and Table C show the 240 frequencies obtainable by setting the external clock to 4MHz (M114S) and 6MHz (M114SF) respectively with table lenght of 16 bytes, single reading and without inserting the octave divisor. These are the highest octave frequencies provided by the device. In practice double, quadruple, etc... frequencies may be obtained by writing 2, 4, etc. complete waveform periods in the table.

Lower frequencies can be generated by programming higher table lengths and/or repeated reading (see table E). The last 16 frequency codes are intended for test purposes and for special useful commands:

- forced-table-terminaiton (FF hex code)
- frequency synchronization (F9, FA, FB, codes)
- previously selected frequency (FC code)
- ROMID (F8 code)

These commands are explained elsewhere in detail.

Octave Divisor Bit (1bit)

This bit is used to pass from the octave to another without changing the table length. If octave divisor bit is set to 1 the programming frequency is divided by two.

Attenuator (6 bits)

These bits define the attenuation superimposed on all the signal samples produced by the selected channel. The six binary code (0 to 63) is interpreted as a dB value of attenuation (see table D). The programmed six bit code is internally decoded into a 10 bit linear value. After processing by a suitable circuit in order to obtain a gradual amplitude variation, the attenuation data is sent to the internal attenuator.

The only method to stop a running channel is to program into it the maximum attenuation code (63 = 3F Hex).
Code 62 = 3E Hex states for max attenuation but it leaves the channel active.
Code 0 = 00 Hex states for no attenuation.

Amplitude Envelope Control Bit (1Bbit)

Enables/Disables an internal amplitude envelope generator. When set to 0 it orders instant passage from the present amplitude to that programmed. It happens as soon as the current waveform table scanning has finished.

If set to 1 the programmed attenuation value will be reached smootly starting from the current attenuation level. Again this smooth move takes place only after the current waveform table scanning has finished.

If a FTT (Forced-Table-Termination) command is used then the attenuator update (either with the smooth move or not) will begin immediately.

Analog Output Pin Selection (2 bits)

These two bits indicate to which of the 4 analog output pins the corresponding channel signal must be forwarded. More than one channel (even all 16 channels) can be routed to the same output pin. The reconstructed analog signal will be the mix of all the single component signal. The availability of 4 outputs allows to obtain stereophonic effect or to separate channels used for accompanyment from those or "solo" etc.

1^. Table Address (8 bits)

These bits determine the most significant part of the starting address (13 bits) of the first waveform table (Tab.1) in external ROM. The remaining bits of the starting address are automatically set to logical zero (except when the table length is set to 16 byte: in this case the fifth bit is set to one, while the 4 LSB's are set to zero) depending on the selected table length, some of these bits can be Don't Care bits.

2^. Table Address (8 bits)

Exactly as before, but referring to the second waveform table (Tab. 2)

Table Lenght And Reading Mode (6 bits)

These bits specify the length of the first waveform table, the length ratio between the two waveform tables, and their reading mode. A total of 58 distinct combinations are available. See table E.

The three most significant bits characterize the table lengths (from 16 samples up 2048 samples) while the other three characterize the length ratio between tables and the number of repeated readings.

Interpolation (4bits)

These bits define the interpolation coefficent between the two values read from the two waveform tables. This allows for the mixing of two programmed timbres in any integer ratio from 16/0 to 1/15.

The operation carried out is the following :

$D = (D1 * (K + 1)/16) + (D2 * (15 - K)/16)$ where :

- D is the data at the input of the DAC (8 bits in complement with 2)
- D1 is the data read from the 1st table (8 bits in complement with 2)
- D2 is the data read from the 2nd table (8 bits in complement with 2)
- K is a 4 bit interpolation coefficient (from 0 to 15)

Obviously only the first waveform will be output if K = 15. The first table can only assume a minimum percentage value of 1/16 of the max. value. To obtain only the second table values the first and the second table addresses must be exchanged. Another method to produce a sound with only one table would be to specify the same address for both the first and the second table programming parameters, and giving what ever interpolation coefficent you want, so effectively interpolating a table with itself.

F8 Hex: ROM-Identification

This command just sets the device frequency counters to a very short counting modulo, useless for musical purposes.

FC Hex: Previously Selected-Frequency

It is provided to ease writing the control program software for the M114S/SF

FF Hex: Forced-Table-Termination

This command allows a suddenly move from one table to another without waiting the end of the present table scanning. It simulates an end-of-table condition. A dedicated flip-flop is provided to service all the 16 channels

a pending FTT command is serviced according to the channel priority. (maximum delay of 32 µs at 4MHz clock). Note that each new programming sequence resets the flip-flop indicating "pending FFT", so to avoid losing the FTT command you

LAST SIXTEEN FREQUENCY CODES: SPECIAL COMMANDS

Among the last 16 frequency codes there are six intended for special commands

Freq. Code	Abbreviation	Command Explanation
F8 Hex	ROMID	ROM Identification
F9 Hex	RSG	Set-Synchro-Global
FA Hex	RSS	Reverse-Synchro-Status (only for next programming operation)
FB Hex	SSG	Reset-Synchro-Global (as after a hardware reset)
FC Hex	PSF	Previously Selected Frequency
FF Hex	FFT	Forced-Table-Termination

need to wait at least that 32 µs, (24 µs in the M114SF) before issuing any new programming sequence after the FTT command. However, on average, it should be sufficient to wait only half that time.

Using this command you can store a whole new set of data (table addresses, table lenghts, reading modes, attenuation level, interpolation, etc.) except a new frequency value for that channel (nor a new value for the octave control bit). All the sound parameters of a channel can be changed without waiting for the end of the current first waveform table, if a normal programming sequence is issued immediately before the FTT command.

The normal programming sequence must contain the new frequency code + all other new sound parameter.

It is not possible to start a stopped channel with this command, because it has no frequency information within itself, so this command has an effect on a channel only if that channel is already running.

The FTT command is always performed on the first table address.
IMPORTANT - DO NOT USE THE FTT COMMAND SPECIFYING A CHANNEL WHICH IS ACTUALLY STOPPED !
it has no effect on that channel but, it takes its effect on the NEXT normal command on a running channel

Using the FTT command in Delta coding it is impossible to maintain a zero mean value in the reconstructed signal. Though only for a short time a transient in the mean DC output level occurs, because the currently scanned table is terminated early at an unpredictable moment. This special command is intended for percussive sounds, or when working with waveform tables coded in absolute (PCM) mode, or for special effects.

This command can be useful to terminate instantaneously a sound: just program that channel with the FTT command, specifying maximum attenuation AND instantaneous variation of the attenuation.

ASYNCHRONOUS MODE

Normally the M114S/SF chip is working in asynchronous mode (set up at reset). In this working mode the programmed frequency becomes active immediately, without waiting for the running table to end while the table addresses and all the other parameters are changed only when the running table has been completely scanned (end of table condition).

This operative mode is useful for producing vibrato effects on long tables, thanks to the fact that some bytes of the previously programmed table will be read at the newly programmed frequency rate.

SYNCHRONOUS MODE

It is possible to synchronize the frequency change with the end of the first waveform table, so avoiding to read a table in part with the old frequency and in part with the new one.

This way-to-operate is useful in the reproduction of deep vibrato on notes placed at the octave boundary, for glide effects and in any case when it is necessary to go beyond the octave boundary without discontinuity (to avoid clicks).

The commands for synchronization are:

SSG F9 Hex: SET-SYNCHRO-GLOBAL
Activates the global synchronize mode (frequency change at the table end.)

RSG FB Hex: RESET-SYNCHRO-GLOBAL
This command disables synchronous mode.

RSS FA Hex: REVERSE-SYNCHRO-STATUS
This command inverts the synchronism state only for the next programming sequence.

Everyone of these commands is accomplished by sending a complete programming sequence with F9/FA/FB frequency codes respectively.

They affect the whole working mode of the device (all its channels). All the remaining bits are ignored.

Note that RSS command can be obtained by sending eight times the 6-bit data 111110.

WAVEFORMS TABLES ADDRESS

In the programming sequence there are 8 + 8 bits devoted to forming the addresses of the 1^ and 2^ waveform tables from each of which a byte is read into the chip to form a single output sample.

The basic address space for waveform tables is 8 Kbytes, as there are 13 address lines managed by the chip. With external circuitry the address space can be doubled. The 8 + 8 bits in the programming sequence only define the starting addresses of the two tables.

The M114S/SF forms addresses according to the table lengths and the reading mode.

The principle is very simple: given a table length the M114S/SF will automatically manage a corresponding number of least significant bits to step from all zero to all ones in a binary sequence, while the remaining most significant bits of the address will be taken from the MSB's of the eight bit code programmed for that table.

In most cases some of eight programmed bits are Don't Care bits. The following examples can better explain how the addresses are generated.

1° EXAMPLE

Suppose TAB 1 = 32 bytes long, then the 5 LSB bits will be managed by the MS114S/SF while the remaining 13 – 5 = 8 MSB bits will be exactly those programmed as the first table address.

Let be TAB1 (7:0) = 11111100 then the address sequence is:

11111100	00000	(start address = 1F80 Hex)
11111100	00001	
11111100	00010	
11111100	11101	
11111100	11110	
11111100	11111	(table termination) (last address = 1F9F Hex)
11111100	00000	(start address = 1F80 Hex)
11111100	00001	
etc.		

If the chosen read mode requires the first table be read 2 or 4 times, then each address will be repeated along 2 or 4 consecutive "service cycles" before skipping to the next address.

The same applies in making the second table address.

2° EXAMPLE

If TAB 1 = 16 bytes long, then the 4 LSB bits will be managed by the MS114S/SF, THE FIFTH BIT WILL BE ALWAYS SET AT LOGIC ONE, while the remaining 13 – 5 = 8 MSB bits will be exactly those programmed as the first table address.

Let be TAB1 (7:0) = 11001100 then the address sequence is:

11001100	1	0000	(start address = 1990 Hex)
11001100	1	0001	
11001100	1	0010	
11001100	1	1101	
11001100	1	1110	
11001100	1	1111	(table termination) (last address = 199F Hex)
10011100	1	0000	(start address = 1990 Hex)
11001100	1	0001	
etc.			

If the chosen read mode requires the first table be read 2 or 4 times, then each address will be repeated along 2 or 4 consecutive "service cycles" before skipping to the next address.

The same applies in making the second table address.

3° EXAMPLE

If TAB 1 = 64 bytes long, then the 6 LSB bits will be managed by the MS114S/SF while the remaining 13 – 6 = 7 MSB bits will be exactly the 7 MSB bits of the eight programmed as the first table address and the LSB bits is discarded (it is a Don't Care bit).

Let be TAB1 (7:0) = 1010110X then the address sequence is:

1010110	000000	(start address = 1580 Hex)
1010110	000001	
1010110	000010	
1010110	111101	
1010110	111110	
1010110	111111	(table termination) (last address = 15BF Hex)
1010110	000000	(start address = 1580 Hex)
1010110	000001	
etc.		

If the chosen read mode requires the first table be read 2 or 4 times, then each address will be repeated along 2 or 4 consecutive "service cycles" before skipping to the next address.

The same applies in making the second table address.

4° EXAMPLE

If TAB 1 = 2048 bytes long, then the 11 LSB bits will be managed by the MS114S/SF while the remaining 13 – 11 = 2 MSB bits of the eight programmed as the first table address and the other 6 LSB bits are discarded (they are a Don't Care bits).

Let be TAB1 (7:0) = 10XXXXXX then the address sequence is:

10	00000000000	(start address = 1000 Hex)
10	00000000001	
10	00000000010	
10	11111111101	
10	11111111110	
10	11111111111	(table termination) (last address = 17FF Hex)
10	00000000000	(start address = 1000 Hex)
10	00000000001	
etc.		

If the chosen read mode requires the first table be read 2 or 4 times, then each address will be repeated along 2 or 4 consecutive "service cycles" before skipping to the next address.

The same applies in making the second table address.

5° EXAMPLE

Choose the six bits of table length and read mode as follow:

M (2:0) = 100 L (2:0) = 001

As you can see from TABLE E this corresponds to:

TAB1 = 32, each byte being read once

TAB2 = 16, each byte being read twice

Let be TAB1 (7:0) = 11100010 and TAB2 (7:0) = 00110011 then the address sequences for the two tables are:

TAB 1			TAB 2			
11100010	00000	(1C40 Hex)	00110011	1	0000	(0670 Hex) (start)
11100010	00001		00110011	1	0000	
11100010	00010		00110011	1	0001	
11100010	00011		00110011	1	0001	
11100010	00100		00110011	1	0010	
11100010	00101		00110011	1	0010	
11100010	11100		00110011	1	1110	
11100010	11101		00110011	1	1110	
11100010	11110		00110011	1	1111	
11100010	11111	(1C5F Hex)	00110011	1	1111	(067F Hex) (1 table termination)
11100010	00000	(1C40 Hex)	00110011	1	0000	(0670 Hex) (start)
11100010	00001		00110011	1	0000	
11100010	00010		00110011	1	0001	
11100010	00011		00110011	1	0001	
etc.						

SUMMARY

1) The waveform tables whose length is 16 (and also in the special cases when they are 8 or 4 bytes long), must begin at memory location multiple of 32 plus an offset of 16, i.e. the starting address must satisfy the equation [16 + n.32] with n = 0, 1, 2,...

2) The Waveform tables whose lengths is 32, 64,..., 1024, 2048, (i.e. their lenghts 2^ K with K = 5, 6..., 10, 11) must begin at memory locations multiple of 2^ K, that is, the starting address must satisfy the equation [n. 2^ K] with n=0, 1, 2, ...

TABLE B - FREQUENCIES

Note	Deviation	– 6/12	– 5/12	– 4/12	– 3/12	– 2/12	– 1/12	– 2/1000	– 1/1000
	(hex)	0	1	2	3	4	5	6	7
C	0	1016.78	1021.45	1026.69	1031.46	1036.27	1041.67	1044.39	1045.48
C#	1	1077.01	1082.25	1087.55	1092.90	1098.30	1103.14	1106.81	1107.42
D	2	1140.90	1146.79	1152.07	1158.08	1163.47	1168.91	1172.33	1173.71
D#	3	1209.19	1215.07	1221.00	1226.99	1232.29	1238.39	1242.24	1243.78
E	4	1281.23	1287.00	1293.66	1299.55	1305.48	1312.34	1315.79	1317.52
F	5	1356.85	1363.33	1369.86	1376.46	1383.13	1389.85	1393.73	1395.67
F#	6	1437.81	1445.09	1451.38	1458.79	1466.28	1472.75	1478.20	1479.29
G	7	1523.23	1530.22	1538.46	1545.60	1552.80	1560.06	1564.95	1566.17
G#	8	1614.21	1622.06	1629.99	1638.00	1644.74	1652.89	1658.37	1659.75
A	9	1709.40	1781.21	1727.12	1734.61	1743.68	1751.31	1757.47	1759.01
A#	A	1811.59	1819.84	1829.83	1838.24	1846.72	1855.29	1860.47	1862.20
B	B	1919.39	1928.64	1937.98	1947.42	1956.95	1966.57	1972.39	1974.33
2C	C	2032.52	2042.90	2053.39	2063.98	2072.54	2083.33	2087.68	2089.86
2C#	D	2155.17	2164.50	2176.28	2185.79	2195.39	2207.51	2212.39	2214.84
2D	E	2283.11	2293.58	2304.15	2314.81	2325.58	2339.18	2344.67	2347.42
	F	Testing	Testing	Testing	Testing	Testing	Testing	Testing	Testing

Note	Deviation	0	+ 1/1000	+ 2/1000	+ 1/12	+ 2/12	+ 3/12	+ 4/12	+ 5/12
	(hex)	8	9	A	B	C	D	E	F
C	0	1046.57	1047.67	1048.77	1051.52	1056.52	1061.57	1066.67	1071.81
C#	1	1108.65	1109.88	1111.11	1114.21	1119.19	1124.86	1130.58	1135.72
D	2	1174.40	1175.78	1177.16	1180.64	1186.24	1191.90	1197.60	1203.37
D#	3	1244.56	1245.33	1246.88	1250.78	1256.28	1262.63	1269.04	1274.70
E	4	1318.39	1319.26	1321.00	1324.50	1331.56	1337.79	1344.09	1350.44
F	5	1396.65	1397.62	1398.60	1403.51	1410.44	1417.43	1424.50	1430.62
F#	6	1480.38	1481.48	1482.58	1486.99	1494.77	1501.50	1508.30	1516.30
G	7	1567.40	1568.63	1569.86	1576.04	1583.53	1591.09	1598.72	1606.43
G#	8	1661.13	1662.51	1663.89	1669.45	1677.85	1684.92	1693.48	1702.13
A	9	1760.56	1762.11	1763.89	1768.35	1777.78	1785.71	1793.72	1803.43
A#	A	1863.93	1865.67	1867.41	1874.41	1883.24	1892.15	1901.14	1910.22
B	B	1976.28	1978.24	1980.20	1984.13	1994.02	2004.01	2014.10	2024.29
2C	C	2092.05	2094.24	2096.44	2103.05	2114.16	2123.14	2134.47	2143.62
2C#	D	2217.29	2219.76	2222.22	2227.17	2239.64	2249.72	2259.89	2272.73
2D	E	2350.18	2352.94	2355.71	2361.28	2372.48	2383.79	2395.21	2406.74
	F	ROMID	SSG	RSS	RSG	Previously Selected Frequency	Testing	Testing	Forced Table Terminat.

TABLE C - FRQUENCIES (fosc = 5.99456 MHz)

Note	Deviation	– 6/12	– 5/12	– 4/12	– 3/12	– 2/12	– 1/12	– 2/1000	– 1/1000
	(hex)	0	1	2	3	4	5	6	7
G	0	1523.78	1523.79	1538.64	1545.79	1552.99	1561.08	1565.16	1566.80
G#	1	1614.04	1621.90	1629.84	1637.86	1645.95	1653.22	1658.71	1659.62
A	2	1709.80	1718.62	1726.54	1735.54	1743.62	1751.77	1758.91	1758.97
A#	3	1812.14	1820.95	1829.84	1838.82	1846.75	1855.90	1861.66	1863.98
B	4	1920.10	1928.75	1938.73	1947.55	1956.45	1966.72	1971.89	1974.49
2C	5	2033.43	2043.14	2052.93	2062.82	2072.82	2082.89	2088.70	2091.61
2C#	6	2154.77	2165.66	2175.09	2186.20	2197.42	2207.13	2215.28	2216.92
2D	7	2282.77	2293.25	2305.60	2316.29	2327.08	2337.97	2345.29	2347.13
2D#	8	2419.11	2430.88	2442.77	2454.77	2464.87	2477.09	2485.31	2487.37
2E	9	2561.78	2574.98	2588.32	2599.55	2613.15	2624.59	2633.81	2636.13
2F	A	2714.93	2727.28	2742.25	2754.85	2767.57	2780.41	2788.17	2790.76
2F#	B	2876.47	2890.34	2904.34	2918.48	2932.76	2947.18	2955.90	2958.82
2G	C	3046.02	3061.57	3077.29	3093.17	3105.99	3122.17	3128.68	3131.95
2G#	D	3229.83	3243.81	3261.46	3275.72	3290.10	3308.26	3315.58	3319.25
2A	E	3421.55	3437.25	3453.09	3469.07	3485.21	3505.59	3513.81	3517.93
	F	Testing	Testing	Testing	Testing	Testing	Testing	Testing	Testing

Note	Deviation	0	+ 1/1000	+ 2/1000	+ 1/12	+ 2/12	+ 3/12	+ 4/12	+ 5/12
	(hex)	8	9	A	B	C	D	E	F
G	0	1568.44	1570.08	1571.73	1575.86	1583.35	1590.91	1598.55	1606.26
G#	1	1661.46	1663.31	1665.16	1669.79	1677.27	1685.76	1694.34	1702.03
A	2	1760.00	1762.07	1764.14	1769.35	1777.75	1786.22	1794.78	1803.42
A#	3	1865.14	1866.30	1868.63	1874.47	1882.71	1892.22	1901.83	1910.31
B	4	1975.79	1977.10	1979.71	1984.95	1995.53	2004.87	2014.30	2023.82
2C	5	2093.07	2094.54	2096.00	2103.35	2113.74	2124.22	2134.81	2143.98
2C#	6	2218.56	2220.21	2221.85	2228.46	2240.12	2250.21	2260.39	2272.39
2D	7	2348.97	2350.81	2352.65	2361.92	2373.14	2384.47	2395.91	2407.45
2D#	8	2489.44	2491.50	2493.58	2501.90	2514.50	2525.09	2537.92	2550.88
2E	9	2638.45	2640.78	2643.10	2650.11	2664.25	2676.14	2688.14	2702.69
2F	A	2793.06	2795.97	2798.58	2809.07	2822.30	2835.65	2849.13	2862.73
2F#	B	2961.74	2964.67	2967.60	2973.49	2988.31	3003.29	3018.41	3033.68
2G	C	3135.23	3138.51	3141.80	3151.71	3168.37	3181.83	3198.80	3212.52
2G#	D	3322.93	3326.61	3330.31	3337.73	3356.42	3371.52	3386.76	3406.00
2A	E	3522.07	3526.21	3530.37	3538.70	3555.49	3572.44	3589.56	3606.84
	F	ROMID	SSG	RSS	RSG	Previously Selected Frequency	Testing	Testing	Forced Table Terminat.

TABLE D - ATTENUATION

N = six bit attenuation code decimal value (0:63)
V = internally decoded linear ten bit value (0:1023)
A = theoretical attenuation value in decibels
= 20 . Log ((V + 1)/1024)

N	V	A
0	1023	0.00
1	939	0.74
2	863	1.48
3	791	2.23
4	727	2.96
5	667	3.71
6	611	4.47
7	559	5.24
8	515	5.95
9	471	6.73
10	431	7.50
11	395	8.25
12	363	8.98
13	335	9.68
14	307	10.43
15	283	11.14
16	259	11.91
17	235	12.75
18	215	13.52
19	199	14.19
20	183	14.91
21	166	15.75
22	152	16.51
23	140	17.22
24	128	17.99
25	117	18.77
26	107	19.54
27	98	20.29
28	90	21.03
29	83	21.72
30	76	22.48
31	69	23.30
.	.	.
.	.	.
.	.	.
63	0	STOP

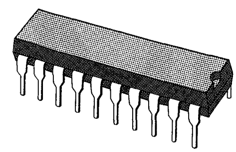
TABLE E - READING MODES

Mode		Length		Read N.	
M	L	T1	T2	T1	T2
000	000	16	16	2	2
000	001	32	32	2	2
000	010	64	64	2	2
000	011	128	128	2	2
000	100	256	256	2	2
000	101	512	512	2	2
000	110	1024	1024	2	2
000	111	2048	1048	2	2
001	000	16	16	1	1
001	001	32	32	1	1
001	010	64	64	1	1
001	011	128	128	1	1
001	100	256	256	1	1
001	101	512	512	1	1
001	110	1024	1024	1	1
001	111	2048	2048	1	1
010	000	16	16	4	4
010	001	32	32	4	4
010	010	64	64	4	4
010	011	128	128	4	4
010	100	256	256	4	4
010	101	512	512	4	4
010	110	1024	1024	4	4
010	111	1024*	1024	4	4
011	000	16	16$	1	1
011	001	32	32	1	1
011	010	64	64	1	1
011	011	128	128	1	1
011	100	256	256	1	1
011	101	512	512	1	1
011	110	1024	1024	1	1
011	111	2048	2048	1	1
100	000	16	8	1	2
100	001	32	16	1	2
100	010	64	32	1	2
100	011	128	64	1	2
100	100	256	128	1	2
100	101	512	256	1	2
100	110	1024	512	1	2
100	111	2048	1024	1	2
101	000	16	16$	1	1
101	001	32	16$	1	1
101	010	64	16	1	1
101	011	128	32	1	1
101	100	256	64	1	1
101	101	512	128	1	1
101	110	1024	256	1	1
101	111	2048	512	1	1
110	000	16	4	1	4
110	001	32	8	1	4
110	010	64	16	1	4
110	011	128	32	1	4
110	100	256	64	1	4
110	101	512	128	1	4
110	110	1024	256	1	4
110	111	2048	512	1	4
111	000	16	16$	1	1
111	001	32	16$	1	1
111	010	64	16$	1	1
111	011	128	16	1	1
111	100	256	32	1	1
111	101	512	64	1	1
111	110	1024	128	1	1
111	111	2048	256	1	1

* REPETITIONS
$ EXCEPTIONS

REMOTE CONTROL TRANSMITTER

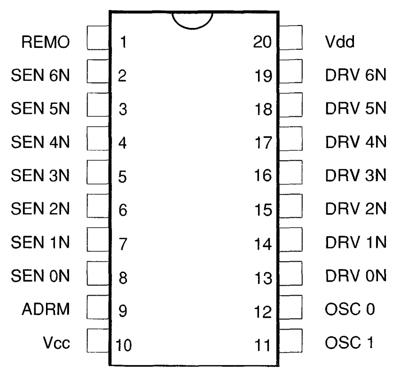
- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V ($-I_{OH}$ = 80mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2μA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 4 TO 11V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)



DIP20
(Plastic Package)

ORDER CODE : M3004AB1

PIN CONNECTIONS



91DSM3004AB1-01

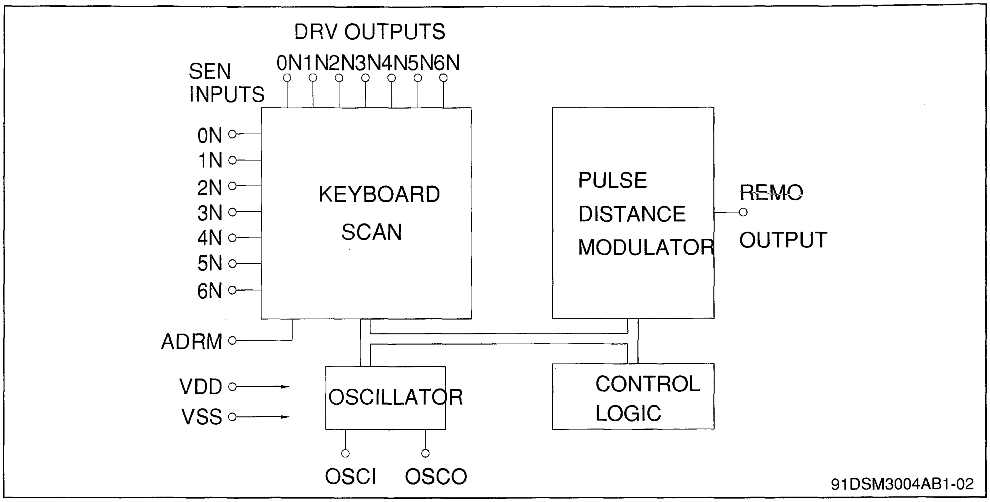
DESCRIPTION

The M3004AB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3004AB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmision.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.
In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function is an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.
The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1ms, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT / OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively.
Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.
In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.
In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.
There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.
The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing.

Mode	T_O (ms)	t_P (µs)	t_M (µs)	t_{ML} (µs)	t_{MH} (µs)	t_W (ms)
Flashed	2.53	8.8	-	-	-	121
Modulated	2.53	-	26.4	17.6	8.8	121

f_{OSC}	455kHz	t_{OSC} = 2.2µs
t_P	4 x t_{OSC}	Flashed Pulse Width
t_M	12 x t_{OSC}	Modulation Period
t_{ML}	8 x t_{OSC}	Modulation Period LOW
t_{MH}	4 x t_{OSC}	Modulation Period HIGH
T_O	1152 x t_{OSC}	Basic Unit of Pulse Distance
t_W	55296 x t_{OSC}	Word Distance

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O
Reference Time	3 x T_O

Table 3 : Transmission Mode and Sub-system Adress Selection.

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Adress				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
FLASHED	0	1	1	1							
	1	0	0	0	O						
	2	0	0	1	X	O					
	3	0	1	0	X	X	O				
	4	0	1	1	X	X	X	O			
	5	1	0	0	X	X	X	X	O		
	6	1	0	1	X	X	X	X	X	O	
MODULATED	0	1	1	1							O
	1	0	0	0	O						O
	2	0	0	1	X	O					O
	3	0	1	0	X	X	O				O
	4	0	1	1	X	X	X	O			O
	5	1	0	0	X	X	X	X	O		O
	6	1	0	1	X	X	X	X	X	O	O

O = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
V_{SS}	SEN1N	0	0	1	1	1	1	8 to 15
V_{SS}	SEN2N	0	1	0	1	1	1	16 to 23
V_{SS}	SEN3N	0	1	1	1	1	1	24 to 31
V_{SS}	SEN4N	1	0	0	1	1	1	32 to 39
V_{SS}	SEN5N	1	0	1	1	1	1	40 to 47
V_{SS}	SEN6N	1	1	0	1	1	1	48 to 55
V_{SS}	SEN5N and SEN6N	1	1	1	1	1	1	56 to 63

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 12	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 150	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C	4		12	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz REMO,Output unload V_{DD} = 6V		0.8	1.5	mA
		V_{DD} = 9V		1.5	3	mA
		• Inactive (stand-by mode) V_{DD} = 6V			2	µA
		V_{DD} = 9V			2	µA
f_{OSC}	Oscill. Frequency	V_{DD} = 4 to 11V (cer resonator)	350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N						
V_{IL}	Input Voltage Low	V_{DD} = 4 to 11V			0.2 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 4 to 11V	0.8 x V_{DD}			V
- I_I	Input Current	V_{DD} = 4V, V_I = 0V	25		250	µA
		V_{DD} = 11V, V_I = 0V	75		750	µA
I_I	Input Leakage Current	V_{DD} = 11V, V_I = VDD			1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N						
V_{OL}	Output Voltage "ON"	V_{DD} = 4V, I_O = 0.1mA			0.3	V
		V_{DD} = 11V, I_O = 1mA			0.5	V
I_O	Output Current "OFF"	V_{DD} = 11V, V_O = 11V			10	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.2 x V_{DD}	V
V_{IH}	Input Voltage High		0.8 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 4V V_{DD} = 11V	 25 75		 250 750	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond., V_{IN} = V_{DD} V_{DD} = 4V V_{DD} = 11V	 25 75		 250 750	 µA µA
DATA OUTPUT REMO						
- I_{OH}	Output Current High	V_{DD} = 6V, V_{OH} = 3V V_{DD} = 9V, V_{OH} = 6V	80 80			mA mA
I_{OL}	Output Current Low	V_{DD} = 6V, V_{OL} = 0.2V V_{DD} = 9V, V_{OL} = 0.1V			0.6 0.6	mA mA
t_{OH}	Pulse Length	V_{DD} = 6V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = 6V, OSC1 at V_{DD}	0.8		2.7	µA
V_{OH}	Output Voltage high	V_{DD} = 6V, - I_{OL} = 0.1mA			V_{DD} - 0.6	V
V_{OL}	Output Voltage Low	V_{DD} = 6V, I_{OH} = 0.1mA			0.6	V

Figure 1 : Typical Application.

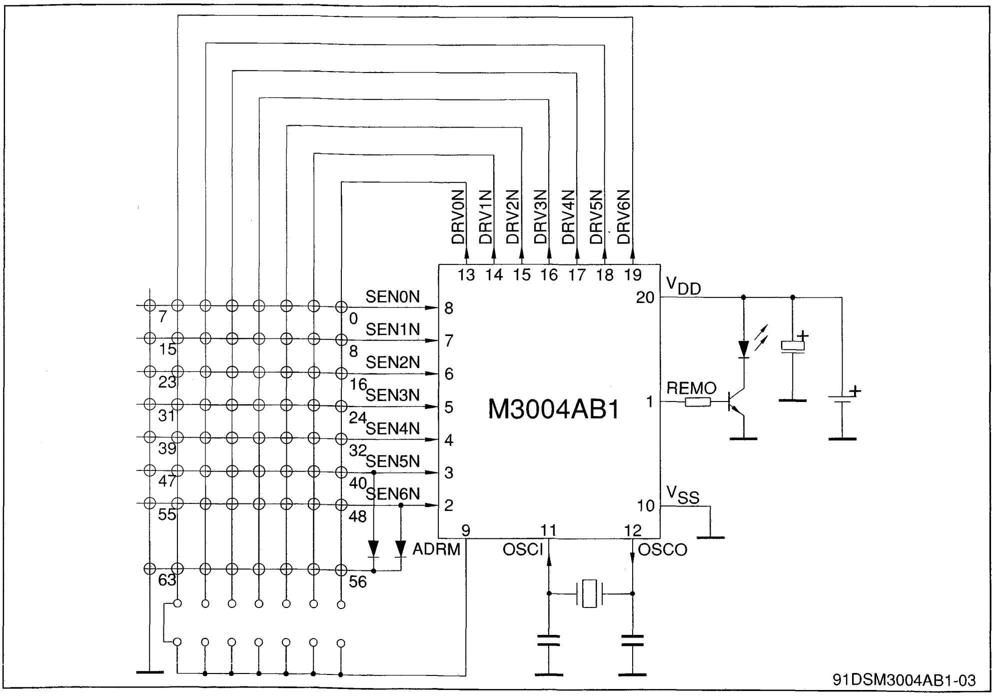


Figure 2 : Data Format of REMO Output; REF = Reference Time; T0 and T1 = Toggle bits; S0, S1 and S2 = System address; A, B, C, D, E and F = Command bits.
(a) flashed mode : transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed)
(b) modulated mode : transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).

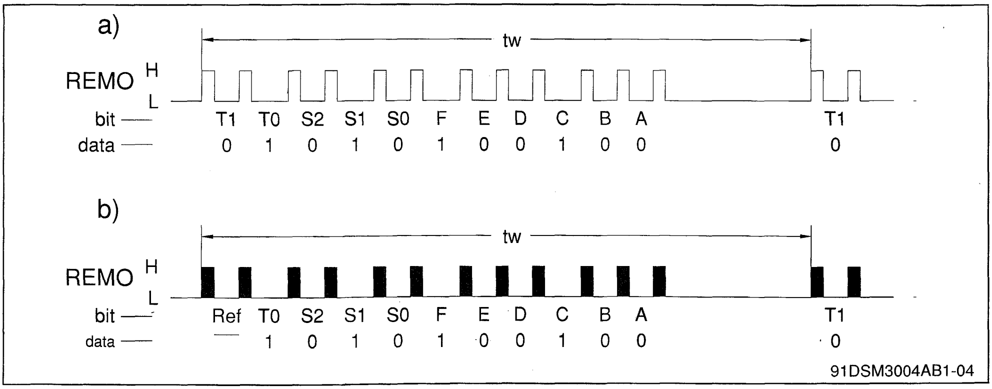


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse { $t_{PW} = (5 \times t_M) + t_{MH}$ }.

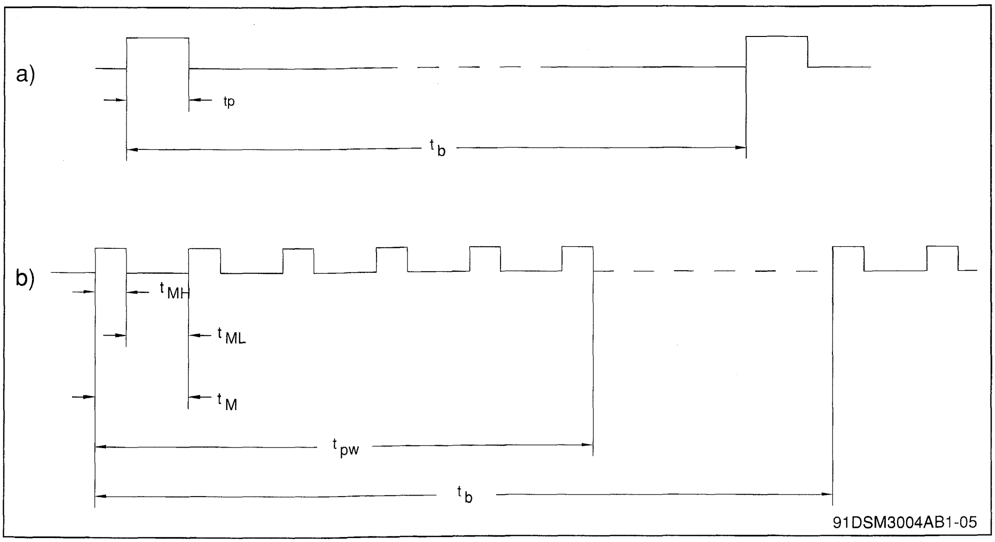


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O.

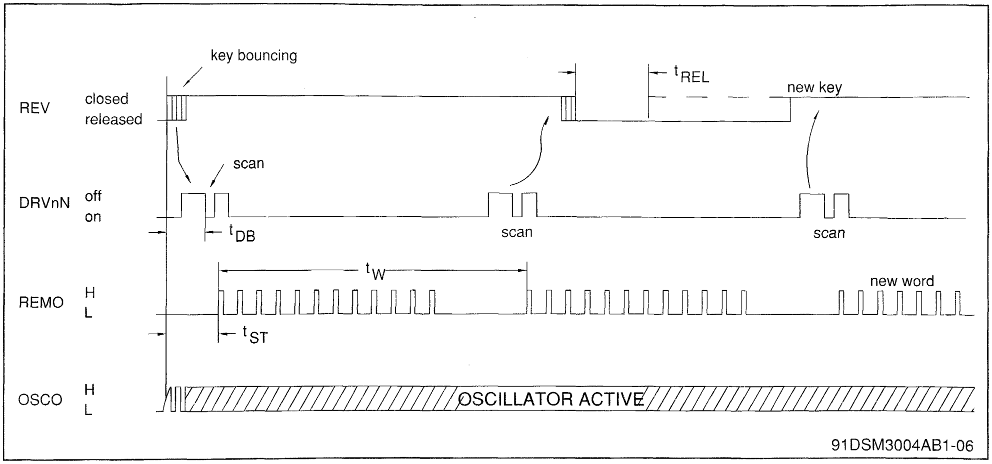
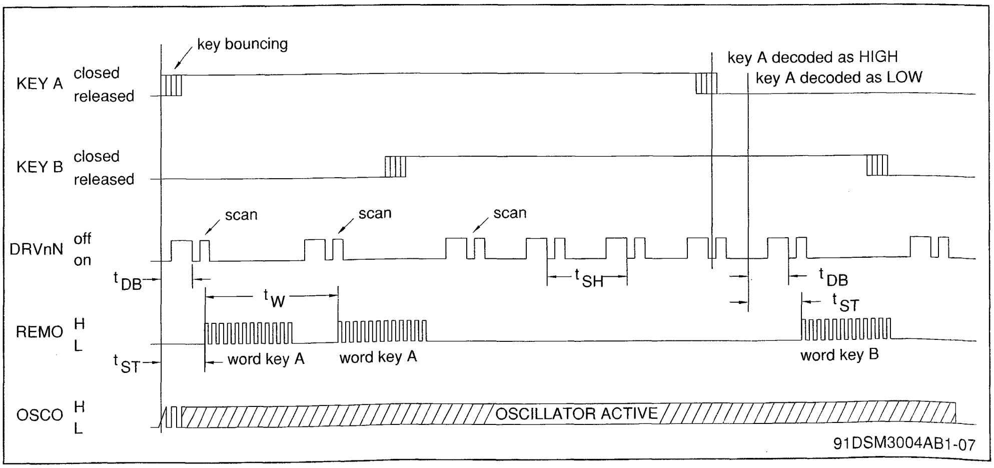
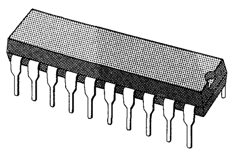


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O.



REMOTE CONTROL TRANSMITTER

- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V (– I_{OH} = 80mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2µA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 2 TO 6.5V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)



DIP20
(Plastic Package)

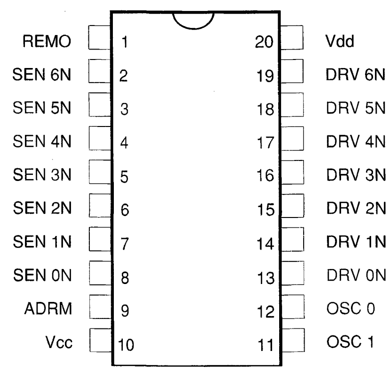
ORDER CODE : M3004LAB1

DESCRIPTION

The M3004LAB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3004LAB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

PIN CONNECTIONS



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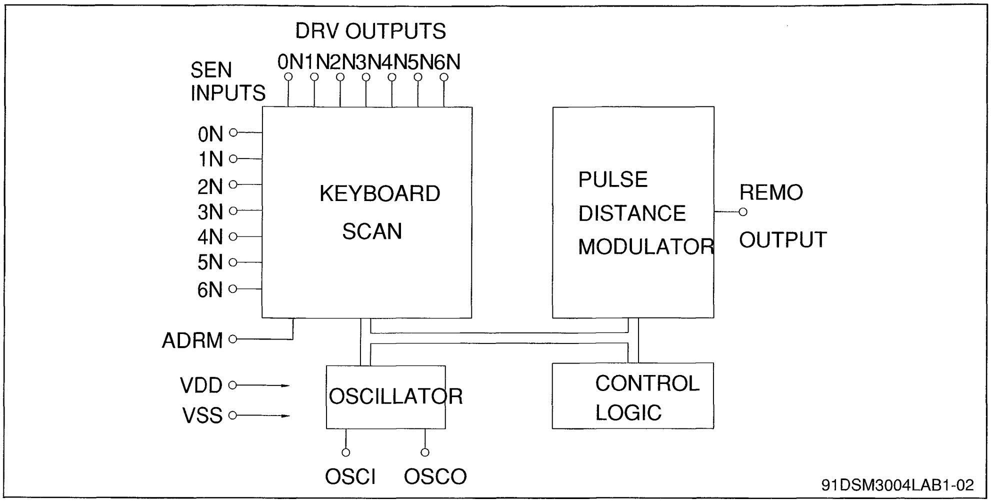
BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmision.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.
In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function is an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.
The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1ms, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT / OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively.
Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.
In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.
In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.
There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.
The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing.

Mode	T_O (ms)	t_P (μs)	t_M (μs)	t_{ML} (μs)	t_{MH} (μs)	t_W (ms)
Flashed	2.53	8.8	-	-	-	121
Modulated	2.53	-	26.4	17.6	8.8	121

f_{OSC}	455kHz	t_{OSC} = 2.2μs
t_P	4 x t_{OSC}	Flashed Pulse Width
t_M	12 x t_{OSC}	Modulation Period
t_{ML}	8 x t_{OSC}	Modulation Period LOW
t_{MH}	4 x t_{OSC}	Modulation Period HIGH
T_O	1152 x t_{OSC}	Basic Unit of Pulse Distance
t_W	55296 x t_{OSC}	Word Distance

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O
Reference Time	3 x T_O

Table 3 : Transmission Mode and Sub-system Adress Selection.

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Adress				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	O						
A	2	0	0	1	X	O					
S	3	0	1	0	X	X	O				
H	4	0	1	1	X	X	X	O			
E	5	1	0	0	X	X	X	X	O		
D	6	1	0	1	X	X	X	X	X	O	
M											
O	0	1	1	1							O
D	1	0	0	0	O						O
U	2	0	0	1	X	O					O
L	3	0	1	0	X	X	O				O
A	4	0	1	1	X	X	X	O			O
T	5	1	0	0	X	X	X	X	O		O
E	6	1	0	1	X	X	X	X	X	O	O
D											

O = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code F	E	D	C	B	A	Matrix Position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
V_{SS}	SEN1N	0	0	1	1	1	1	8 to 15
V_{SS}	SEN2N	0	1	0	1	1	1	16 to 23
V_{SS}	SEN3N	0	1	1	1	1	1	24 to 31
V_{SS}	SEN4N	1	0	0	1	1	1	32 to 39
V_{SS}	SEN5N	1	0	1	1	1	1	40 to 47
V_{SS}	SEN6N	1	1	0	1	1	1	48 to 55
V_{SS}	SEN5N and SEN6N	1	1	1	1	1	1	56 to 63

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 7	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 125	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C	2		6.5	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz REMO,Output unload V_{DD} = 3V		0.25	0.5	mA
		V_{DD} = 6V		1.0	2	mA
		• Inactive (stand-by mode) V_{DD} = 6V			2	µA
f_{OSC}	Oscill. Frequency	V_{DD} = 2 to 6.5V (cer resonator)	350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N						
V_{IL}	Input Voltage Low	V_{DD} = 2 to 6.5V			0.3 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 2 to 6.5V	0.7 x V_{DD}			V
- I_I	Input Current	V_{DD} = 2V, V_I = 0V	10		100	µA
		V_{DD} = 6.5V, V_I = 0V	100		600	µA
I_I	Input Leakage Current	V_{DD} = 6.5V, V_I = V_{DD}			1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N						
V_{OL}	Output Voltage "ON"	V_{DD} = 2V, I_O = 0.1mA			0.3	V
		V_{DD} = 6.5V, I_O = 1mA			0.6	V
I_O	Output Current "OFF"	V_{DD} = 6.5V, V_O = 11V			10	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.3 x V_{DD}	V
V_{IH}	Input Voltage High		0.7 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond.,V_{IN} = V_{DD} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
DATA OUTPUT REMO						
- I_{OH}	Output Current High	V_{DD} = 2V, V_{OH} = 0.8V V_{DD} = 6.5V, V_{OH} = 5V	60 80			mA mA
I_{OL}	Output Current Low	V_{DD} = 2V, V_{OL} = 0.4V V_{DD} = 6.5V, V_{OL} = 0.4V			0.6 0.6	mA mA
t_{OH}	Pulse Length	V_{DD} = 6.5V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = 2V V_{DD} = 6.5V, OSC1 at V_{DD}	 5		5 7	µA µA
V_{OH}	Output Voltage high	V_{DD} = 6.5V, - I_{OL} = 0.1mA	V_{DD} - 0.8			V
V_{OL}	Output Voltage Low	V_{DD} = 6.5V, I_{OH} = 0.1mA			0.7	V

Figure 1 : Typical Application.

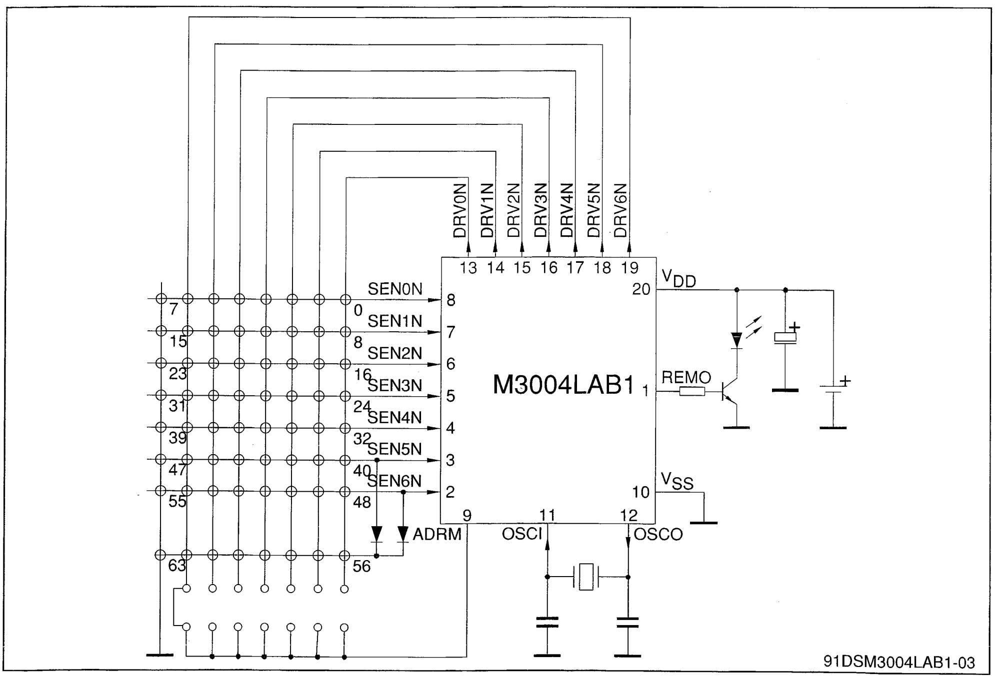


Figure 2 : Data Format of REMO Output; REF = Reference Time; T0 and T1 = Toggle bits; S0, S1 and S2 = System address; A, B, C, D, E and F = Command bits.
(a) flashed mode : transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed)
(b) modulated mode : transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).

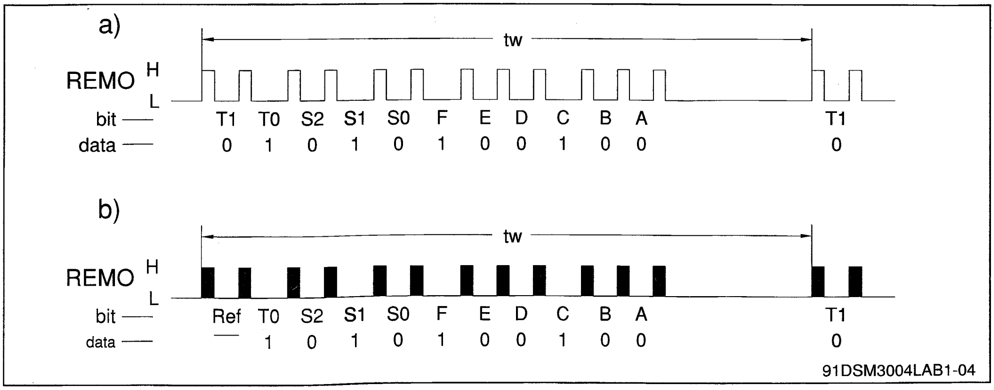


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse { $t_{PW} = (5 \times t_M) + t_{MH}$ }.

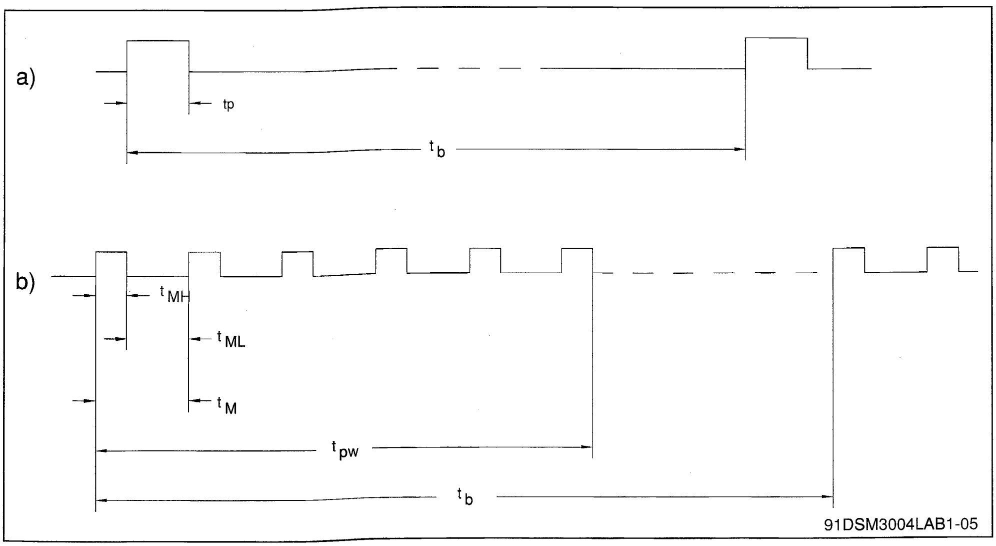


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O.

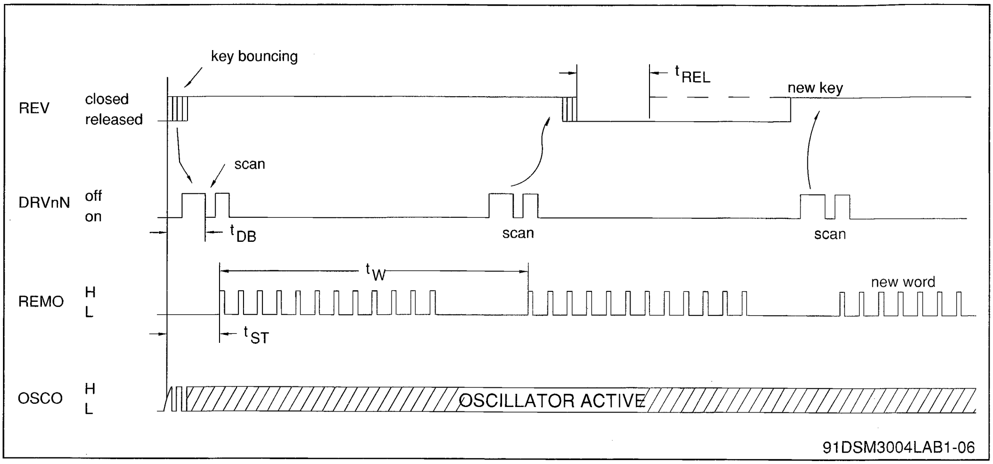
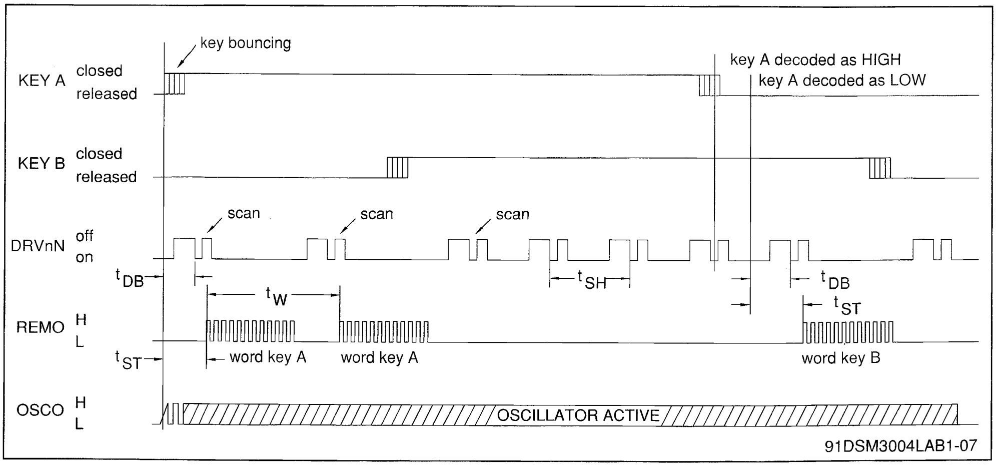
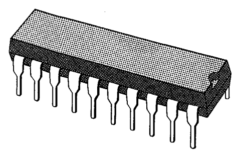


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O.



REMOTE CONTROL TRANSMITTER

- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V ($-I_{OH}$ = 80mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2µA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 4 TO 11V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)



DIP20
(Plastic Package)

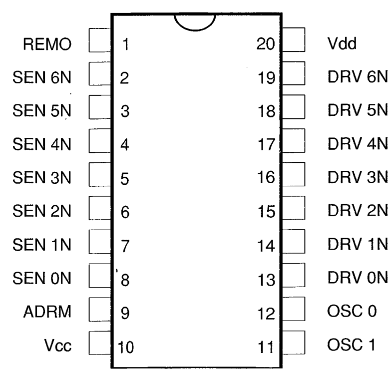
ORDER CODE : M3005AB1

DESCRIPTION

The M3005AB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

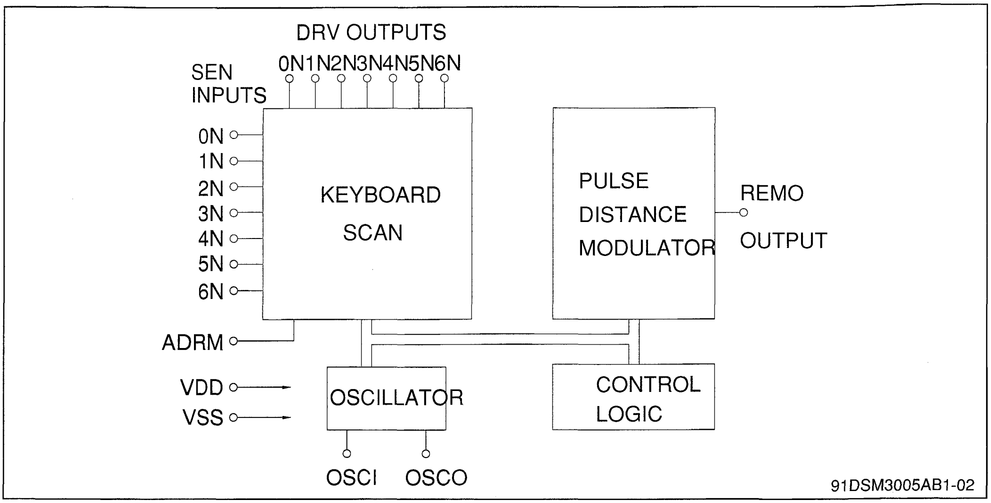
The M3005AB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

PIN CONNECTIONS



91DSM3005AB1-01

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmision.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.
In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function is an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.
The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1ms, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT / OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively.
Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.
In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.
In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.
There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.
The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing.

Mode	T_O (ms)	t_P (μs)	t_M (μs)	t_W (ms)
Flashed	2.53	8.8	-	121
Modulated	2.53	-	t_{osc}	121

	Flash Mode	Carrier Mode	
f_{OSC}	455kHz	600kHz	
t_P	4 x t_{osc}		Flashed Pulse Width
t_M		t_{osc}	Modulation Period
N		8*	Number of Modulation Pulses
T_O	1152 x t_{osc}	1536 x tOSC	Basic Unit of Pulse Distance
t_W	55296 x t_{osc}	73728 x tOSC	Word Distance

The following number of pulses may be selected by Metal option : N = 8, 12, 16.

Note : The different dividing ratio for T_O and t_W between flash mode and carrier mode is obtained by changing the modulo of a particular divider from divide by 3 during flash mode to divide by 4 during carrier mode. This allows the use of a 600kHz ceramic resonator during carrier mode to obtain a better noise immunity for the receiver without a significant change in T_O and t_W. For first samples, the correct divider ration is obtained by a metal mask option. For final parts, this is automatically done together with the selection of flash-/carrier mode.

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O

Table 3 : Transmission Mode and Sub-system Adress Selection.

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Adress				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	O						
A	2	0	0	1	X	O					
S	3	0	1	0	X	X	O				
H	4	0	1	1	X	X	X	O			
E	5	1	0	0	X	X	X	X	O		
D	6	1	0	1	X	X	X	X	X	O	
M											
O	0	1	1	1							O
D	1	0	0	0	O						O
U	2	0	0	1	X	O					O
L	3	0	1	0	X	X	O				O
A	4	0	1	1	X	X	X	O			O
T	5	1	0	0	X	X	X	X	O		O
E	6	1	0	1	X	X	X	X	X	O	O
D											

O = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code F	E	D	C	B	A	Matrix Position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
V_{SS}	SEN1N	0	0	1	1	1	1	8 to 15
V_{SS}	SEN2N	0	1	0	1	1	1	16 to 23
V_{SS}	SEN3N	0	1	1	1	1	1	24 to 31
V_{SS}	SEN4N	1	0	0	1	1	1	32 to 39
V_{SS}	SEN5N	1	0	1	1	1	1	40 to 47
V_{SS}	SEN6N	1	1	0	1	1	1	48 to 55
V_{SS}	SEN5N and SEN6N	1	1	1	1	1	1	56 to 63

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 12	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 150	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C	4		11	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz, V_{DD} = 6V REMO,Output unload, V_{DD} = 9V • Inactive (stand-by mode), V_{DD} = 6V V_{DD} = 9V		0.8 1.5	1.5 3 2 2	mA mA µA µA
f_{OSC}	Oscill. Frequency	V_{DD} = 4 to 11V (cer resonator)	350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N						
V_{IL}	Input Voltage Low	V_{DD} = 4 to 11V			0.2 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 4 to 11V	0.8 x V_{DD}			V
- I_I	Input Current	V_{DD} = 4V, V_I = 0V V_{DD} = 11V, V_I = 0V	25 75		250 750	µA µA
I_I	Input Leakage Current	V_{DD} = 11V, V_I = VDD			1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N						
V_{OL}	Output Voltage "ON"	V_{DD} = 4V, I_O = 0.1mA V_{DD} = 11V, I_O = 1mA			0.3 0.5	V V
I_O	Output Current "OFF"	V_{DD} = 11V, V_O = 11V			10	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.2 x V_{DD}	V
V_{IH}	Input Voltage High		0.8 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 4V V_{DD} = 11V	 25 75		 250 750	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond.,V_{IN} = V_{DD} V_{DD} = 4V V_{DD} = 11V	 25 75		 250 750	 µA µA
DATA OUTPUT REMO						
- I_{OH}	Output Current High	V_{DD} = 6V, V_{OH} = 3V V_{DD} = 9V, V_{OH} = 6V	80 80			mA mA
I_{OL}	Output Current Low	V_{DD} = 6V, V_{OL} = 0.2V V_{DD} = 9V, V_{OL} = 0.1V			0.6 0.6	mA mA
t_{MH}/t_{OSC}	Pulse Duty Cycle	During Carrier Mode	0.4	0.5	0.6	
t_{OH}	Pulse Length	V_{DD} = 6V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = 6V, OSC1 at V_{DD}	0.8		2.7	µA
V_{OH}	Output Voltage high	V_{DD} = 6V, - I_{OL} = 0.1mA			V_{DD} - 0.6	V
V_{OL}	Output Voltage Low	V_{DD} = 6V, I_{OH} = 0.1mA			0.6	V

Figure 1 : Typical Application.

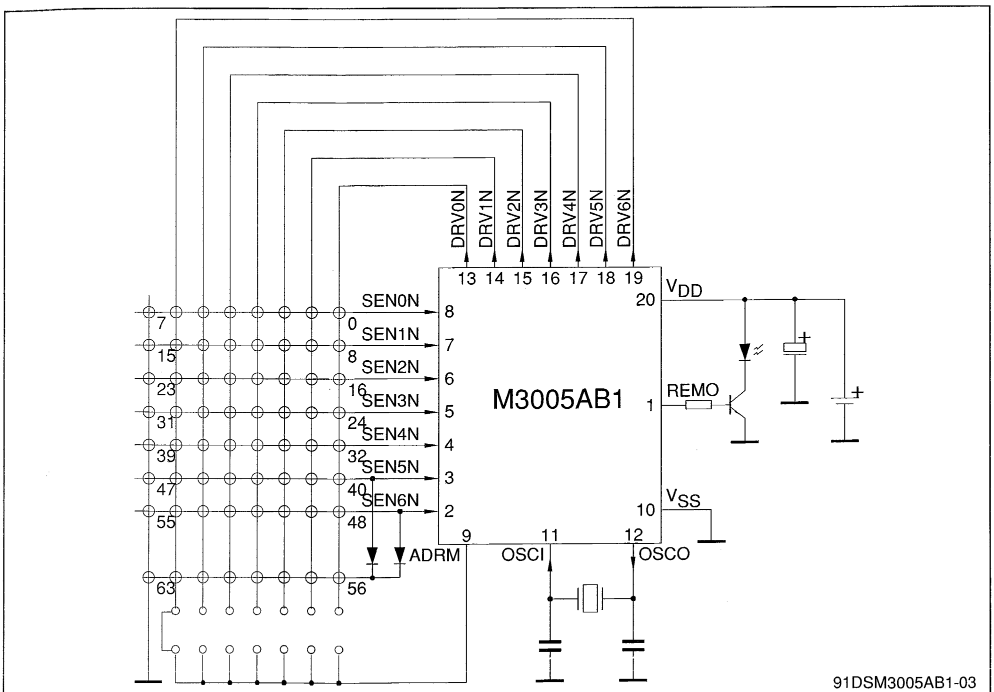


Figure 2 : Data Format of REMO Output

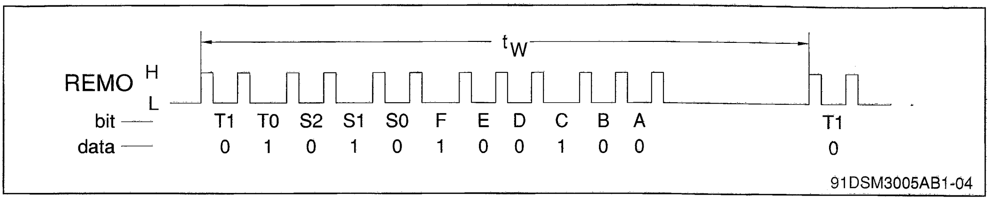


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse

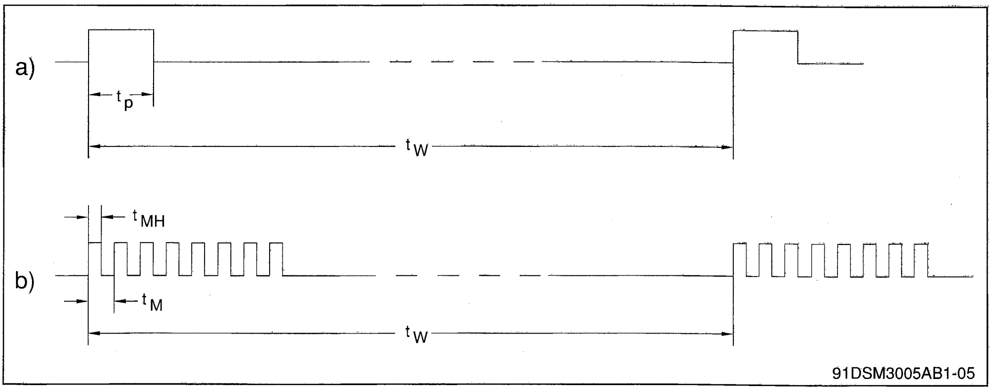


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O.

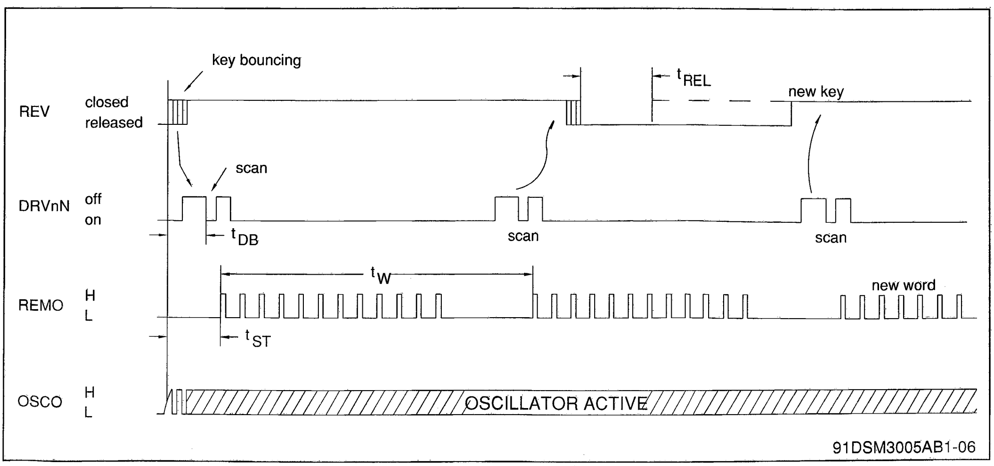
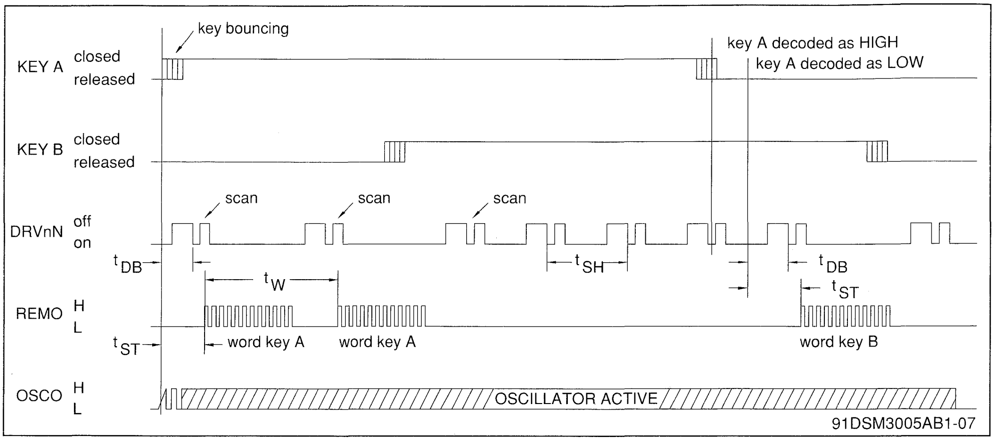
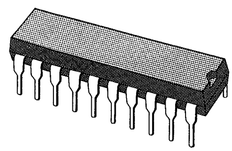


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O.



REMOTE CONTROL TRANSMITTER

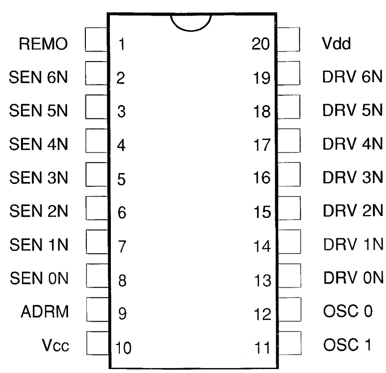
- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V ($-I_{OH}$ = 80mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2μA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 2 TO 6.5V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)



DIP20
(Plastic Package)

ORDER CODE : M3005LAB1

PIN CONNECTIONS



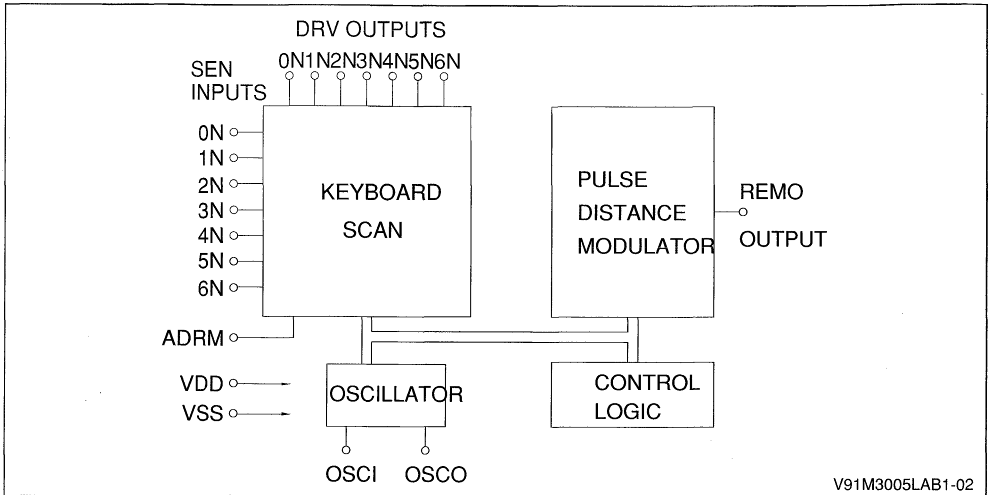
91DS3005LAB1-01

DESCRIPTION

The M3005LAB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3005LAB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmision.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.

In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function is an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.

The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1ms, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT / OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.

In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing.

Mode	T_O (ms)	t_P (µs)	t_M (µs)	t_W (ms)
Flashed	2.53	8.8	-	121
Modulated	2.53	-	t_{OSC}	121

	Flash Mode	Carrier Mode	
f_{OSC}	455kHz	600kHz	
t_P	4 x t_{OSC}		Flashed Pulse Width
t_M	12 x t_{OSC}	tOSC	Modulation Period
N		8*	Number of Modulation Pulses
T_O	1152 x t_{OSC}	1536 x tOSC	Basic Unit of Pulse Distance
t_W	55296 x t_{OSC}	73728 x tOSC	Word Distance

The following number of pulses may be selected by Metal option : N = 8, 12, 16.

Note : The different dividing ratio for T_O and t_W between flash mode and carrier mode is obtained by changing the modulo of a particular divider from divide by 3 during flash mode to divide by 4 during carrier mode. This allows the use of a 600kHz ceramic resonator during carrier mode to obtain a better noise immunity for the receiver without a significant change in T_O and t_W. For first samples, the correct divider ration is obtained by a metal mask option. For final parts, this is automatically done together with the selection of flash-/carrier mode.

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O

Table 3 : Transmission Mode and Sub-system Adress Selection.

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Adress				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	O						
A	2	0	0	1	X	O					
S	3	0	1	0	X	X	O				
H	4	0	1	1	X	X	X	O			
E	5	1	0	0	X	X	X	X	O		
D	6	1	0	1	X	X	X	X	X	O	
M											
O	0	1	1	1							O
D	1	0	0	0	O						O
U	2	0	0	1	X	O					O
L	3	0	1	0	X	X	O				O
A	4	0	1	1	X	X	X	O			O
T	5	1	0	0	X	X	X	X	O		O
E	6	1	0	1	X	X	X	X	X	O	O
D											

O = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
V_{SS}	SEN1N	0	0	1	1	1	1	8 to 15
V_{SS}	SEN2N	0	1	0	1	1	1	16 to 23
V_{SS}	SEN3N	0	1	1	1	1	1	24 to 31
V_{SS}	SEN4N	1	0	0	1	1	1	32 to 39
V_{SS}	SEN5N	1	0	1	1	1	1	40 to 47
V_{SS}	SEN6N	1	1	0	1	1	1	48 to 55
V_{SS}	SEN5N and SEN6N	1	1	1	1	1	1	56 to 63

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 7	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 150	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C	2		6.5	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz REMO,Output unload, V_{DD} = 3V		0.25	0.5	mA
		V_{DD} = 6V		1.0	2	mA
		• Inactive (stand-by mode) V_{DD} = 6V			2	µA
f_{OSC}	Oscill. Frequency	V_{DD} = 2 to 6.5V (cer resonator)	350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N						
V_{IL}	Input Voltage Low	V_{DD} = 2 to 6.5V			0.3 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 2 to 6.5V	0.7 x V_{DD}			V
- I_I	Input Current	V_{DD} = 2V, V_I = 0V	10		100	µA
		V_{DD} = 6.5V, V_I = 0V	100		600	µA
I_I	Input Leakage Current	V_{DD} = 6.5V, V_I = V_{DD}			1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N						
V_{OL}	Output Voltage "ON"	V_{DD} = 2V, I_O = 0.25mA			0.3	V
		V_{DD} = 6.5V, I_O = 2.5mA			0.6	V
I_O	Output Current "OFF"	V_{DD} = 6.5V, V_O = 11V			10	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.3 x V_{DD}	V
V_{IH}	Input Voltage High		0.7 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond.,V_{IN} = V_{DD} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
DATA OUTPUT REMO						
- I_{OH}	Output Current High	V_{DD} = 2V, V_{OH} = 0.8V V_{DD} = 6.5V, V_{OH} = 5V	60 80			mA mA
I_{OL}	Output Current Low	V_{DD} = 2V, V_{OL} = 0.4V V_{DD} = 6.5V, V_{OL} = 0.4V			0.6 0.6	mA mA
t_{MH}/t_{OSC}	Pulse Duty Cycle	During Carrier Mode	0.4	0.5	0.6	
t_{OH}	Pulse Length	V_{DD} = 6.5V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = 2V V_{DD} = 6.5V, OSC1 at V_{DD}	 5		5 7	µA µA
V_{OH}	Output Voltage high	V_{DD} = 6.5V, - I_{OL} = 0.1mA	V_{DD} - 0.8			V
V_{OL}	Output Voltage Low	V_{DD} = 6.5V, I_{OH} = 0.1mA			0.7	V

Figure 1 : Typical Application.

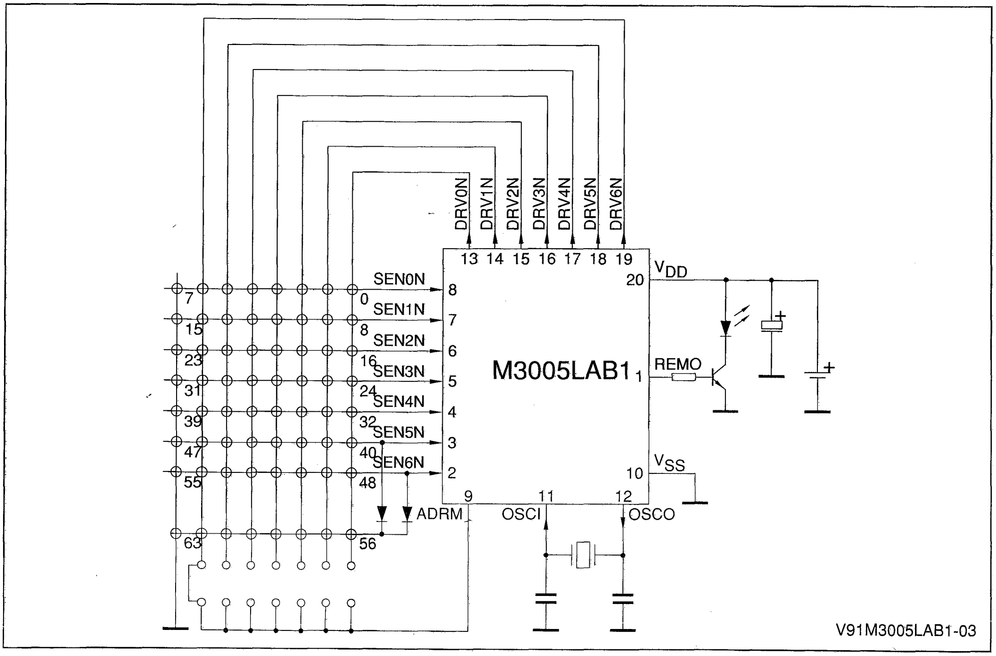


Figure 2 : Data Format of REMO Output

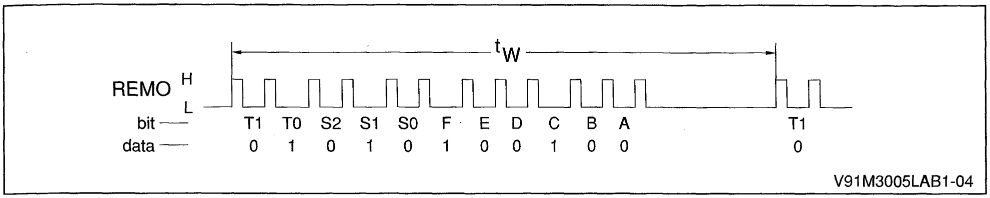


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse

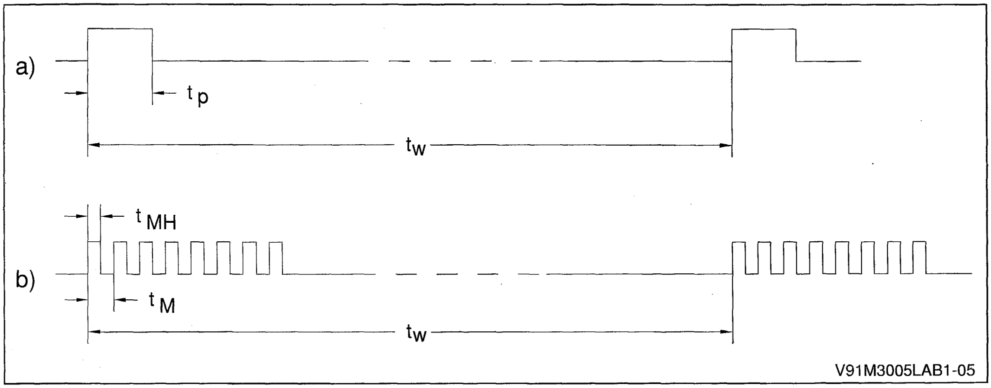


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O.

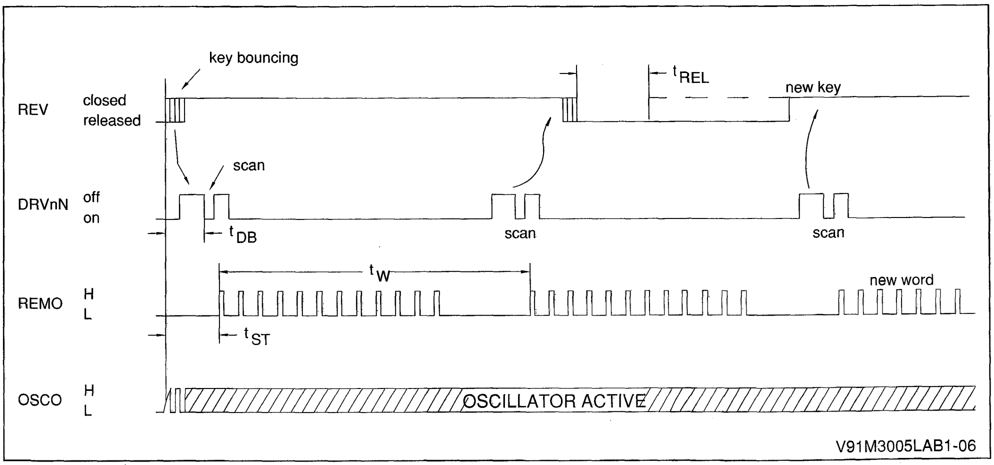
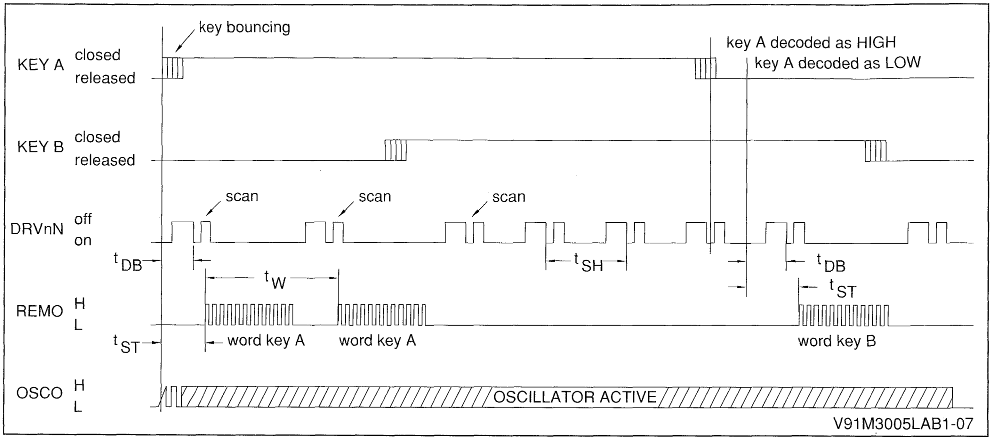


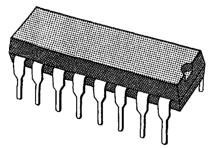
Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O.



REMOTE CONTROL TRANSMITTER

ADVANCE DATA

- FLASHED OR MODULATED TRANSMISSION
- 5 SUB-SYSTEM ADDRESSES
- UP TO 36 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V ($-I_{OH}$ = 120mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2μA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 2 TO 6.5V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)
- ENCAPSULATION : 16-LEAD PLASTIC DIL



DIP16
(Plastic Package)

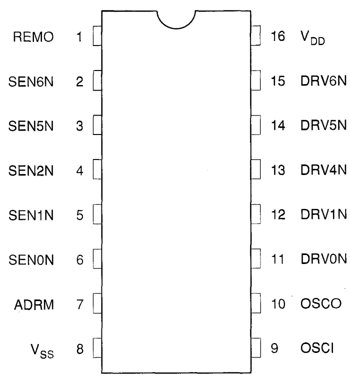
ORDER CODE : M3006LAB1

DESCRIPTION

The M3006LAB1 transmitter IC is designed for infrared remote control systems. It has a total of 180 commands which are divided into 5 sub-system groups with 36 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3006LAB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

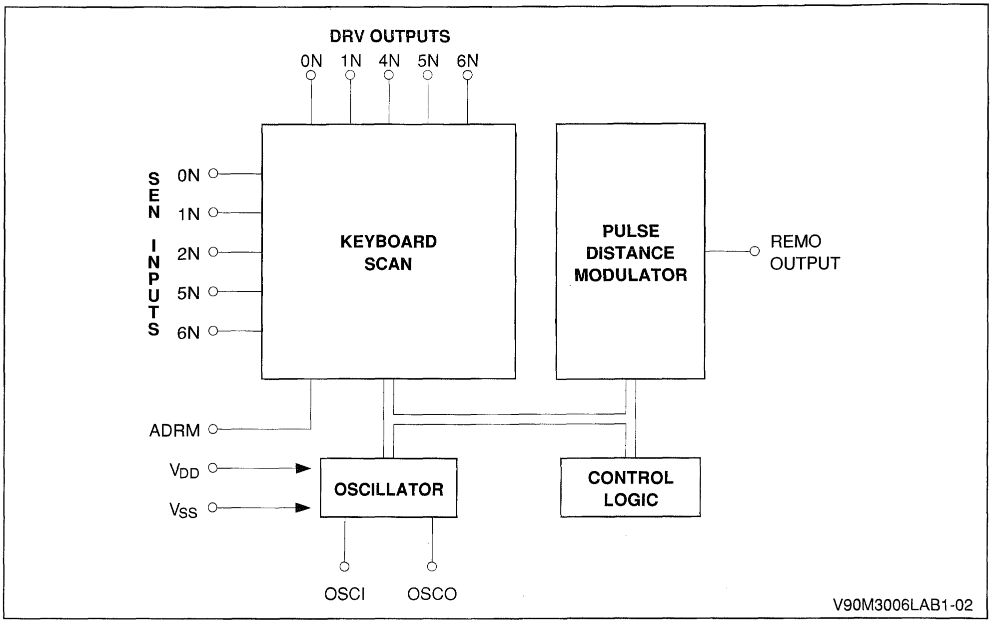
PIN CONNECTIONS



V90M3006LAB1-01

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 5 driver outputs and 5 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 5 sense inputs (SEN0N to SEN6N) enable the generation of 30 command codes. With 2 external diodes all 36 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRVON to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of five sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode, only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if drivers DRV1N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV4N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 5. A change of the sub-system address will not start a transmission.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.

In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.

The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1msec, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT/OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively).

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.

In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 5, 11, 17, 23, 29 and 35) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 30 to 35).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing.

Mode	T_O (ms)	t_P (µs)	t_M (µs)	t_{ML} (µs)	t_{MH} (µs)	t_W (ms)
Flashed	2.53	8.8	-	-	-	121
Modulated	2.53	-	26.4	17.6	8.8	121

f_{OSC}	455kHz	t_{OSC} = 2.2µs
t_P	4 x t_{OSC}	Flashed Pulse Width
t_M	12 x t_{OSC}	Modulation Period
t_{ML}	8 x t_{OSC}	Modulation Period LOW
t_{MH}	4 x t_{OSC}	Modulation Period HIGH
T_O	1152 x t_{OSC}	Basic Unit of Pulse Distance
t_W	55296 x t_{OSC}	Word Distance

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O
Reference Time	3 x T_O

Table 3 : Transmission Mode and Sub-system Adress Selection.

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Adress				Driver DRVnN for n =				
	#	S2	S1	S0	0	1	4	5	6
FLASHED	0	1	1	1					
	1	0	0	0	O				
	2	0	0	1	X	O			
	5	1	0	0	X	X	O		
	6	1	0	1	X	X	X	O	
MODULATED	0	1	1	1					O
	1	0	0	0	O				O
	2	0	0	1	X	O			O
	5	1	0	0	X	X	O		O
	6	1	0	1	X	X	X	O	O

O = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code F	E	D	C	B	A	Matrix Position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV4N	SEN0N	0	0	0	1	0	0	2
DRV5N	SEN0N	0	0	0	1	0	1	3
DRV6N	SEN0N	0	0	0	1	1	0	4
V_{SS}	SEN0N	0	0	0	1	1	1	5
V_{SS}	SEN1N	0	0	1	1	1	1	6 to 11
V_{SS}	SEN2N	0	1	0	1	1	1	12 to 17
V_{SS}	SEN5N	1	0	1	1	1	1	18 to 23
V_{SS}	SEN6N	1	1	0	1	1	1	24 to 29
V_{SS}	SEN5N and SEN6N	1	1	1	1	1	1	30 to 35

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 7	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 125	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C	2		6.5	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz REMO,Output unload V_{DD} = 3V		0.25		mA
		V_{DD} = 6V		1.0		mA
		• Inactive (stand-by mode) V_{DD} = 6V			4	µA
f_{OSC}	Oscill. Frequency	V_{DD} = 2 to 6.5V (cer resonator)	350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N						
V_{IL}	Input Voltage Low	V_{DD} = 2 to 6.5V			0.3 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 2 to 6.5V	0.7 x V_{DD}			V
- I_I	Input Current	V_{DD} = 2V, V_I = 0V	10		100	µA
		V_{DD} = 6.5V, V_I = 0V	100		600	µA
I_I	Input Leakage Current	V_{DD} = 6.5V, V_I = VDD			1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N						
V_{OL}	Output Voltage "ON"	V_{DD} = 2V, I_O = 0.1mA			0.3	V
		V_{DD} = 6.5V, I_O = 1mA			0.6	V
I_O	Output Current "OFF"	V_{DD} = 6.5V, V_O = 6.5V			10	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
KEYBOARD MATRIX - Control Input ADRM						
V_{IL}	Input Voltage Low				0.3 x V_{DD}	V
V_{IH}	Input Voltage High		0.7 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond.,V_{IN} = V_{DD} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
KEYBOARD MATRIX - Data Output REMO						
V_{OH}	Output Voltage High	V_{DD} = 2V, -I_{OH} = 60mA V_{DD} = 6.5V, -I_{OH} = 60mA	0.8 5.0			V V
V_{OL}	Output Voltage Low	V_{DD} = 2V, I_{OL} = 0.3mA V_{DD} = 6.5V, I_{OL} = 0.3mA			0.4 0.4	V V
t_{OH}	Pulse Length	V_{DD} = 6.5V, Oscill. Stopped			1	ms
KEYBOARD MATRIX -Oscillator						
I_I	Input Current	V_{DD} = 2V, OSC1 at V_{DD} V_{DD} = 6.5V, OSC1 at V_{DD}	 5.0		5.0 7.0	µA µA
V_{OH}	Output Voltage high	V_{DD} = 6.5V, - I_{OL} = 0.1mA	V_{DD} - 0.8			V
V_{OL}	Output Voltage Low	V_{DD} = 6.5V, I_{OH} = 0.1mA			0.7	V

Figure 1 : Typical Application.

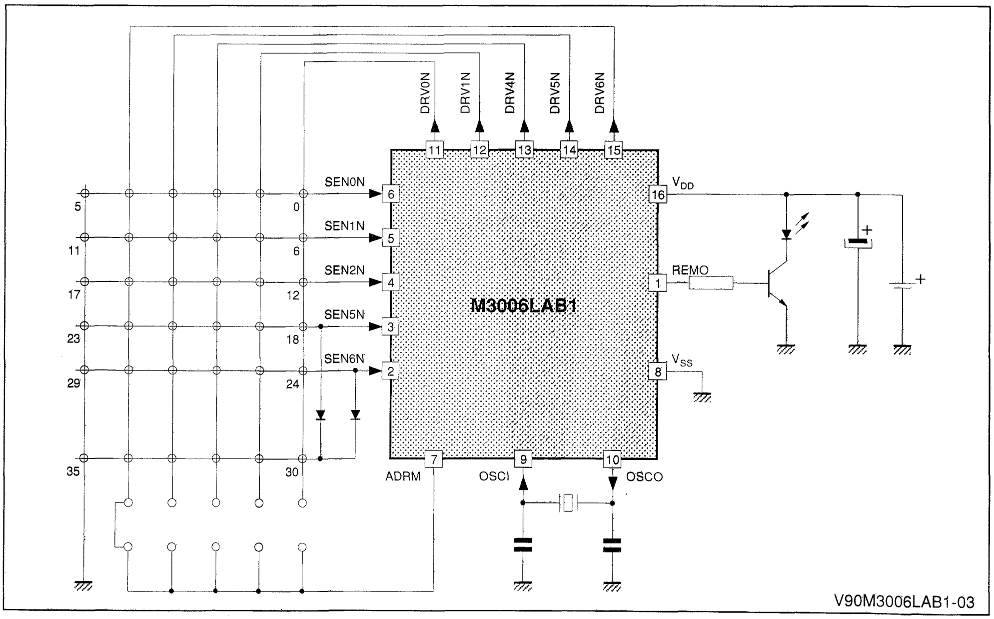


Figure 2 : Data Format of REMO Output; REF = Reference Time; T0 and T1 = Toggle bits; S0, S1 and S2 = System address; A, B, C, D, E and F = Command bits.
(a) flashed mode : transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed)
(b) modulated mode : transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).

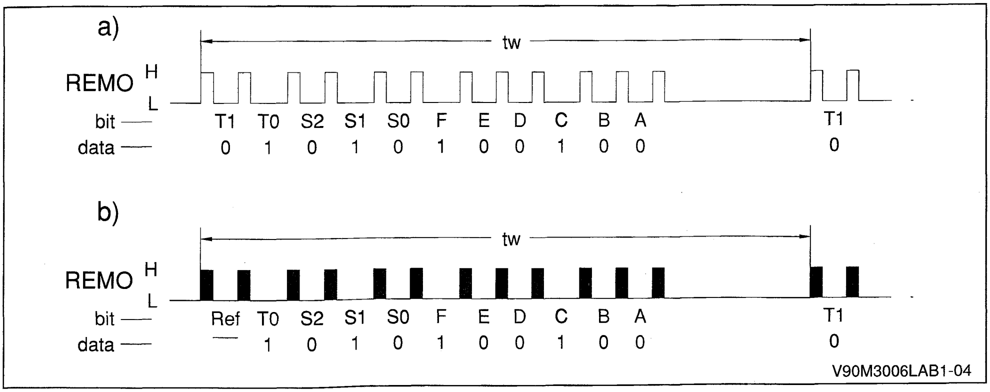


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse { $t_{PW} = (5 \times t_M) + t_{MH}$}.

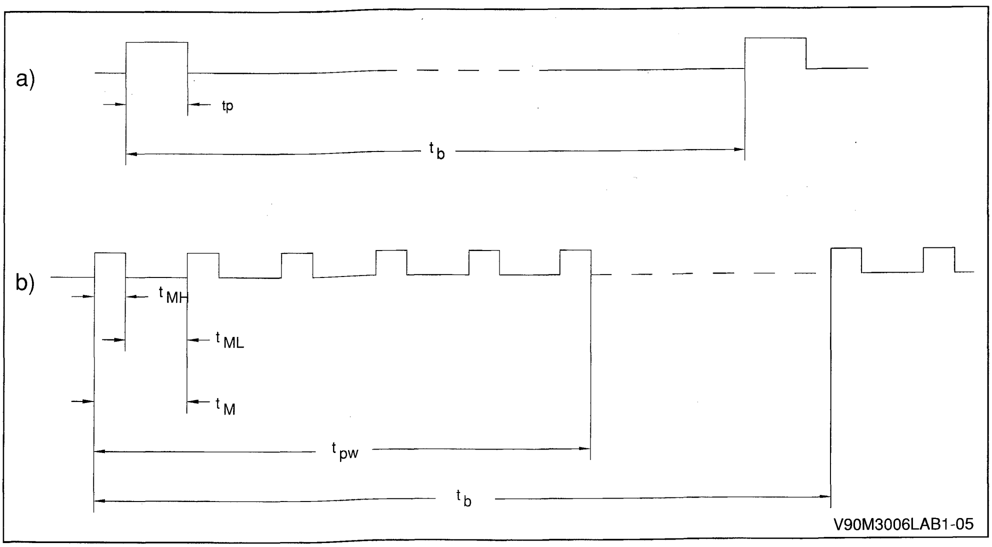


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O.

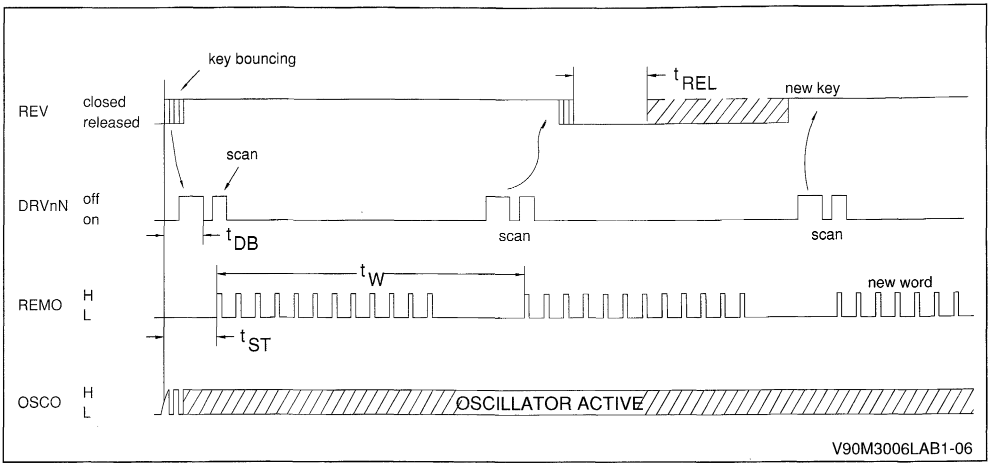
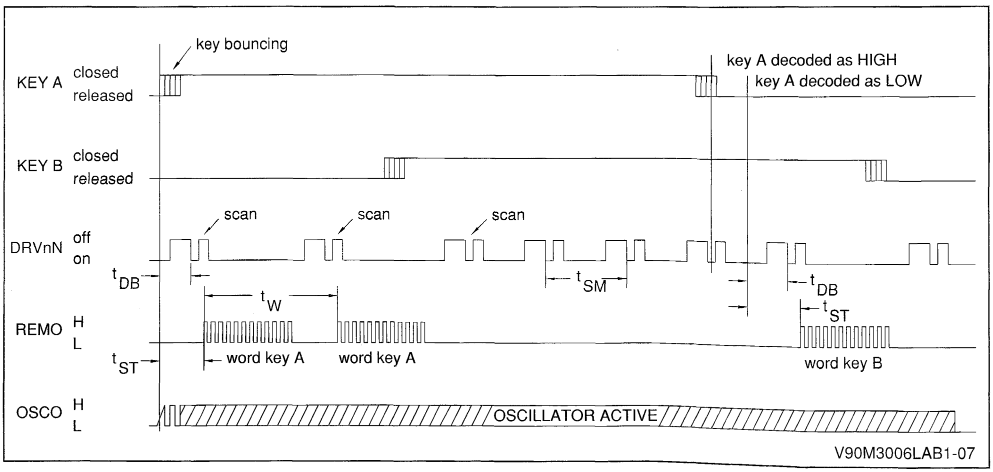
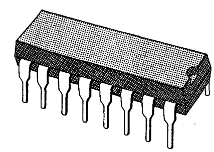


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O.



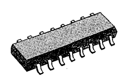
REMOTE CONTROL ENCODER/DECODER CIRCUITS

- M145026 ENCODER
- M145027/M145028 DECODERS
- MAY BE ADDRESSED IN EITHER BINARY OR TRINARY
- TRINARY ADDRESSING MAXIMIZES NUMBER OF CODES
- INTERFACES WITH RF, ULTRASONIC, OR INFRARED TRANSMISSION MEDIAS
- DOUBLE TRANSMISSIONS FOR ERROR CHECKING
- 4.5V TO 18V OPERATION
- ON-CHIP R/C OSCILLATOR, NO CRYSTAL REQUIRED
- HIGH EXTERNAL COMPONENT TOLERANCE, CAN USE 5% COMPONENTS
- STANDARD CMOS B-SERIES INPUT AND OUTPUT CHARACTERISTICS
- APPLICATIONS INCLUDE GARAGE DOOR OPENERS, REMOTE CONTROLLED TOYS, SECURITY MONITORING, ANTITHEFT SYSTEMS, LOW END DATA TRANSMISSIONS WIRE LESS TELEPHONES



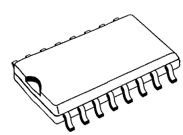
DIP16 (0.25")
(Plastic package)

ORDER CODES :
M145026B1
M145027B1
M145028 B1



SO16 Narrow (0.15")
(Plastic package)

ORDER CODE : M145026D



SO16 Large (0.3")
(Plastic package)

ORDER CODE : M145028D

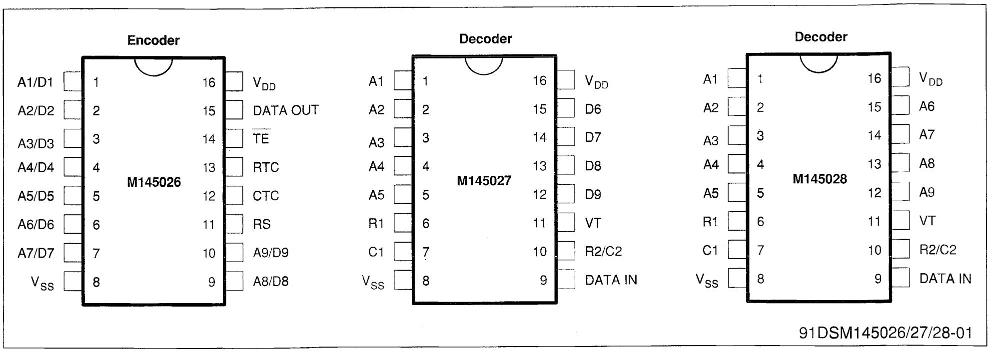
DESCRIPTION

The M145026 encodes nine bits of information and serially transmits this information upon receipt of a transmit enable, $\overline{TE}$, (active low) signal. Nine inputs may be encoded with trinary data (0,1, open) to allow 3^9 (19.683) different codes.

Two decoders are presently available. Both use the same transmitter - the M145026. The decoders will receive the 9-bit word and will interpret some of the bits as address codes and some as data. The M145027 interprets the first five transmitted bits as address and the last four bits as data. The M145028 treats all nine bits as address. If no errors are received, the M145027 outputs the four data bits when the transmitter sends address codes that match that of the receiver. A valid transmission output goes high on both decoders when they recognize an address that matches that of the decoder. Other receivers can be produced with different address/data ratios.

All the devices are available in 16 lead plastic package. The M145026 is available in SO16 plastic package (narrow) and the M145028 is available in SO16 plastic package (large).

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18	V
V_I	Input Voltage, All Inputs	– 0.5 to V_{DD} + 0.5	V
I_I	DC Current Drain Per Pin	10	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_{op}	Operating Temperature Range	– 40 to + 85	°C

TAB-01

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at thses or any other conditions above those indicated in the operational sec-tions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_{amb} = 25 °C)

Symbol	Parameter	V_{DD}	Min.	Typ.	Max.	Unit
t_{TLH} t_{THL}	Output Rise and Fall Time	5 10 15	– – –	100 50 40	200 100 80	ns
t_{TLH} t_{THL}	Data in Rise and Fall Time (M145027, M145028)	5 10 15	– – –	– – –	15 15 15	µs
f_{CL}	Encoder Clock Frequency	5 10 15	0 0 0	– – –	2 5 5	MHz
f_{CL}	Maximum Decoder Frequency (referenced to encoder clock) (see figure 9)	5 10 15	– – –	– – –	240 410 450	kHz
t_{WL}	$\overline{TE}$ Pulse Width	5 10 15	65 30 20	– – –	– – –	ns
	System Propagation Delay ($\overline{TE}$ to valid transmission)	–	–	182	–	Clock Cycles
	Tolerance on Timing Components (ΔRTC + ΔCTC + ΔR1 + ΔC1) (ΔR2 + ΔC2)	 – –	 – –	 – –	 ± 25 ± 25	%

TAB-02

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{DD} V	– 40 °C		25 °C			+ 85 °C		Unit
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OL}	Output Voltage $V_I = V_{DD}$ or 0 "0" Level	5 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	V
V_{OH}	$V_I = 0$ or V_{DD} "1" Level	5 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5 10 15	– – –	4.95 9.95 14.95	– – –	V
V_{IL}	Input Voltage (V_O = 4.5 or 0.5 V) (V_O = 0.9 or 1 V) "0" Level (V_O = 13.5 or 1.5 V)	5 10 15	– – –	1.5 3 4	– – –	2.25 4.50 6.25	1.5 3 4	– – –	1.5 3 4	V
V_{IH}	(V_O = 0.5 or 4.5 V) (V_O = 1.0 or 9 V) "1" Level (V_O = 1.5 or 13.5 V)	5 10 15	3.5 7 11	– – –	3.5 7 11	2.75 5.50 8.25	– – –	3.5 7 11	– – –	V
I_{OH}	Output Drive Current (V_{OH} = 2.5 V) (V_{OH} = 4.6 V) (V_{OH} = 9.5 V) Source (V_{OH} = 13.5 V)	5 5 10 15	– 2.5 – 0.52 – 1.3 – 3.6	– – – –	– 2.1 – 0.44 – 1.1 – 3	– 4.2 – 0.88 – 2.25 – 8.8	– – – –	– 1.7 – 0.36 – 0.9 – 2.4	– – – –	mA
I_{OL}	(V_{OL} = 0.4 V) (V_{OL} = 0.5 V) Sink (V_{OL} = 1.5 V)	5 10 15	0.52 1.3 3.6	– – –	0.44 1.1 3	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	mA
I_I	Input Current TE (M145026, pull up device)	5 10 15	– – –	– – –	3 16 35	4 20 45	7 26 55	– – –	– – –	µA
I_I	Input Current RS (M145026) Data In (M145027, M145028)	15	–	± 0.3	–	± 0.00001	± 0.3	–	± 1.0	µA
I_I	Input Current A1/D1-A9/D9 (M145026) A1-A5 (M145027) A1-A9 (M145028)	5 10 15	– – –	– – –	– – –	± 55 ± 300 ± 650	± 80 ± 340 ± 725	– – –	– – –	µA
C_I	Input Capacitance (V_I = 0)	–	–	–	–	5	7.5	–	–	pF
I_{DD}	Quiescent Current- M145026	5 10 15	– – –	– – –	– – –	0.0050 0.0100 0.0150	0.10 0.20 0.30	– – –	– – –	µA
I_{DD}	Quiescent Current M145027, M145028	5 10 15	– – –	– – –	– – –	30 60 90	50 100 150	– – –	– – –	µA
I_T	Total Supply Current M145026 (f_{CL} = 20 kHz)	5 10 15	– – –	– – –	– – –	100 200 300	200 400 600	– – –	– – –	µA
I_T	Total Supply Current M145027,M145028 (f_{CL} = 20 kHz)	5 10 15	– – –	– – –	– – –	200 400 600	400 800 1200	– – –	– – –	µA

TAB-03

OPERATING CHARACTERISTICS

M145026

The encoder will serially transmit nine bits of trinary data as defined by the state of the A1/D1-A9/D9 input pins. These pins can be in either of three states (0,1, open) allowing 3^9 = 19683 possible codes.The transmit sequence will be initiated by a low level of the $\overline{TE}$ input pin. Each time the $\overline{TE}$ input is forced low the encoder will output two identical data words. This redundant information is used by the receiver to reduce errors. If the $\overline{TE}$ input is kept low, the encoder will continuously transmit the data words. The transmitted words are self-completing (two words will be transmitted for each $\overline{TE}$ pulse).

Each transmitted data bit is encoded into two data pulses. A logic zero will be encoded as two consecutive short pulses, a logic one by two consecutive long pulses, and an open as a long pulse followed by a short pulse. The input state is determined by using a weak output device to try to force each input first low, then high. If only a high state results from the two tests, the input is assumed to be hard wired to V_{DD}. If only a low state is obtained, the input is assumed to be hard wired to V_{SS}. If both a high and a low can be forced at an input, it is assumed to be open and is encoded as such.

The transmit sequence is enabled by a logic zero on the $\overline{TE}$ input. This input has an internal pullup device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high the encoder is completely disabled, the oscillator is inhibited and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started, and an internal reset is generated to initialize the transmit sequence. Each input is then sequentially selected and a determination is made as to input logic state. This information is serially transmitted via the Data Out output pin.

M145027

The decoder will receive the serial data from the encoder, check it for errors and output data if valid. The transmitted data consisting of two identical data words is examined bit by bit as it is received. The first five bits are assumed to be address bits and must be encoded to match the address inputs at the receiver. If the address bits match, the next four (data) bits are stored and compared to the last valid data stored. if this data matches, the VT pin will go high on the 2nd rising edge of the 9th bit of the first word. Between the two data words no signal is sent for three data bit times. As the second encoded word is received, the address must again match, and if it does, the data bits are checked against the previously stored data bits. If the two words of data (four bits each) match, the data is transferred to the output data latches and will remain until new data replaces it. At the same time, the Valid Transmission output pin is brought high and will remain high until an error is received or until no input signal is received for four data bit times.

Although the address information is encoded in trinary fashion, the data information must be either a one or a zero. A trinary (open) will be decoded as a logic one.

M145028

This receiver operates in the same manner as the M145027 except that nine address bits are used and no data output is available. The Valid Transmission output is used to indicate that a valid signal has been received.

Although address information normally is encoded in trinary, the designer should be aware that, for the M145028, the ninth address bit (A9) must be either a one or a zero. This part, therefore, can accept only 2 x 3^8 = 13.122 different codes. A trinary (open) A9 will be interpreted as a logic 1. However if the transmitter sends a trinary (or logic 1) and the receiver address is a logic 1 (or trinary) respectively, the valid transmission output will be shortened to the R1 x C1 time constant.

DOUBLE TRANSMISSION DECODING

Although the encoder sends two words fo error checking, a decoder does not necessarily wait for two transmitted words to be received before issuing a valid transmission output. Refer to the flowcharts in Figure 7 and 8.

Figure 1 : Encoder Block Diagram M145026.

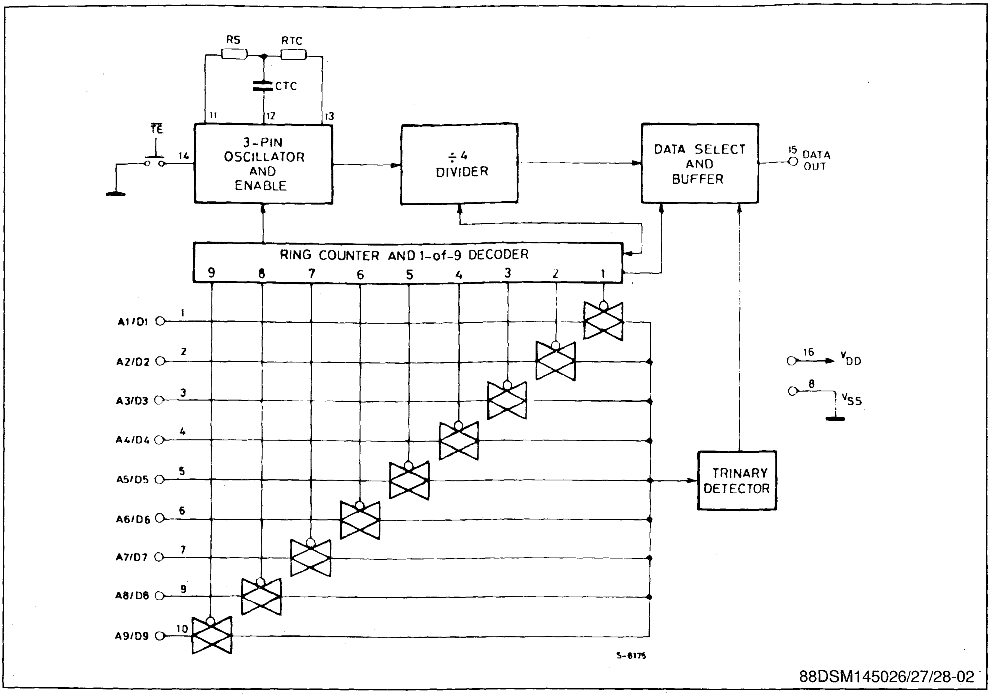


Figure 2 : Decoder Block Diagram M145027.

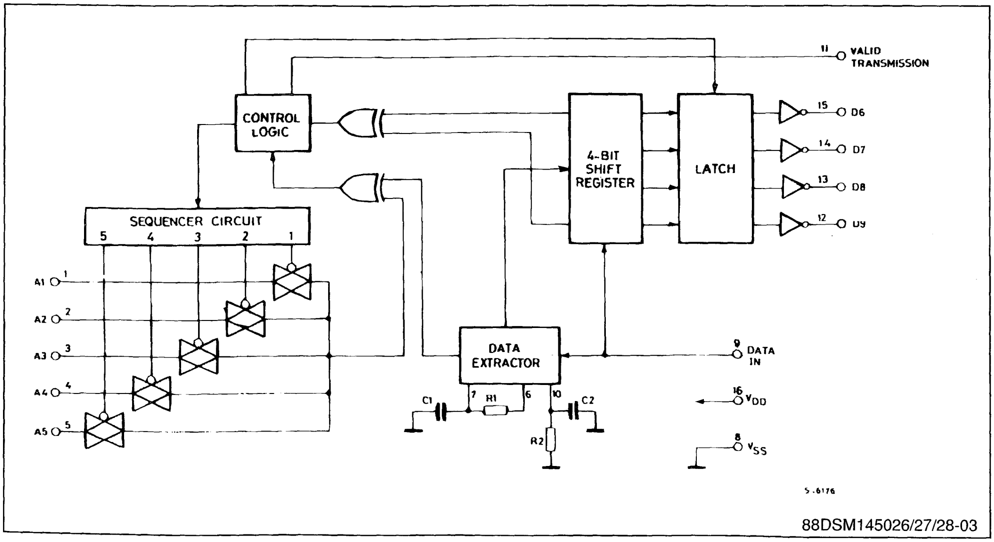
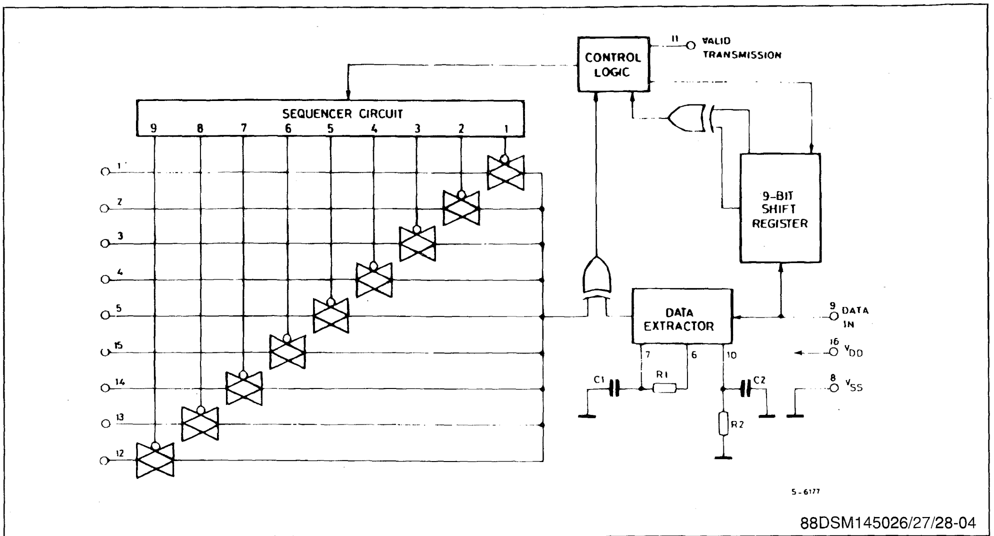


Figure 3 : Decoder Block Diagram M145028.



PIN DESCRIPTION

M145026 ENCODER

A1/D1-A9/D9. These inputs will be encoded and the data serially output form the encoder.

V_{SS}. The most negative supply (usually ground).

RS, CTC, RTC. These pins are part of the oscillator section of the encoder. If an external signal source is used instead of the internal oscillator it should be connected to the RS input and the RTC and CTC pins should be left open.

$\overline{TE}$. This Transmit-Enable (active low) input will initiate transmission when forced low. A pullup device will keep this input high normally.

DATA OUT. This is the output of the encoder that will present the serially encoded signals.

V_{DD}. The most positive supply.

M145027/M145028 DECODERS

A1-A5 (M145027) / A1-A9 (M145028). These are the address inputs that must match the encoder inputs A1/D1-A5/D5 in the case of M145027 or A1/D1-A0/D9 in the case of M145028, in order for the decoder to output data.

D6-D9 (M145027). These outputs will give the information that is presented to the encoder inputs A6/D6-A9/D9.

Note: Only binary data will be acknowledged, a trinary open will be decoded as logic one.

R1, C1. These pins accept a resistor and capacitor that are used to determine whether a narrow pulse or a wide pulse has been encoded. The time constant R1 x C1 should be set to 1.72 transmit clock periods. R1C1 = 3.95 RTC x CTC.

R2/C2. This pin accepts a resistor to V_{SS} and a capacitor to V_{SS} that are used to detect both the end of an encoded word and the end of transmission. The time constant R2 x C2 should be 33.5 transmit clock periods (four data bit periods). This time constant is used to determine that the Data In input has remained low for four data bit times (end of transmission). A separate comparator looks at a voltage equivalent two data bit times (0.4 R2C2) to detect the dead time between transmitted words. R2C2 = 77 x RTC x CTC.

VALID TRANSMISSION, VT. This output will go high when the following conditions are satisfied:

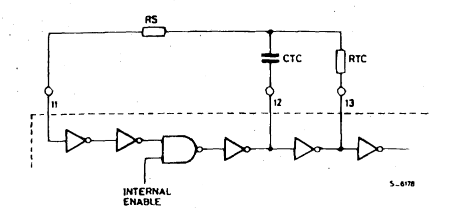
1. the transmitted address matches the receiver address, and
2. the transmitted data matches the last valid data received (M145028 only).

VT will remain high until either a mismatch is received, or no input signal is received for four data data bit times.

V_{DD}. The most positive supply.

V_{SS}. The most negative supply (usually ground).

Figure 4 : Encoder Oscillator Information.



88DSM145026/27/28-05

The value for RS should be chosen to be about 2 times RTC. This range will ensure that current through RS is insignificant compared to current through RTC. The upper limit for RS must ensure that RS x 5 pF (input capacitance) is small compared to RTC x CTC. For frequencies outside the indicated range, the formula will be less accurate. The actual oscillation range of this circuit is from less than 1 Hz to over 1 MHz.

This oscillator will operate at a frequency determined by the external RC network; i.e..

$$f \approx \frac{1}{2.3 \cdot RTC \cdot CTC} \text{ (Hz)}$$

for 1 kHz $\leq f \leq$ 400 kHz

where: CTC = CTC + C layout + 12 pF

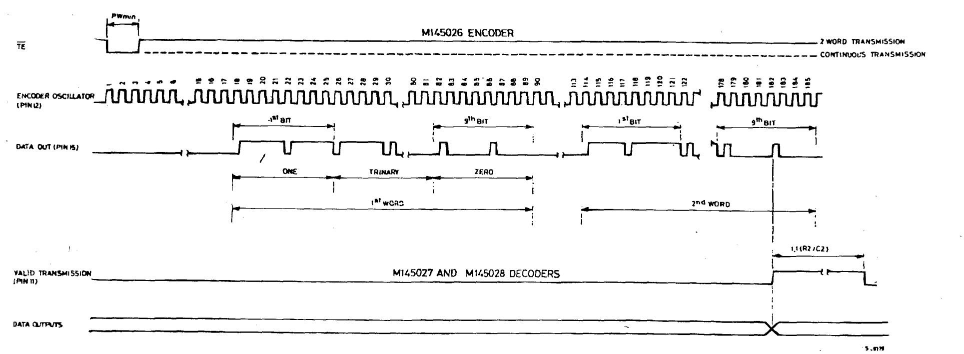
RS $\approx$ 2 RTC

RS $\geq$ 20 k

RTC $\geq$ 10 k

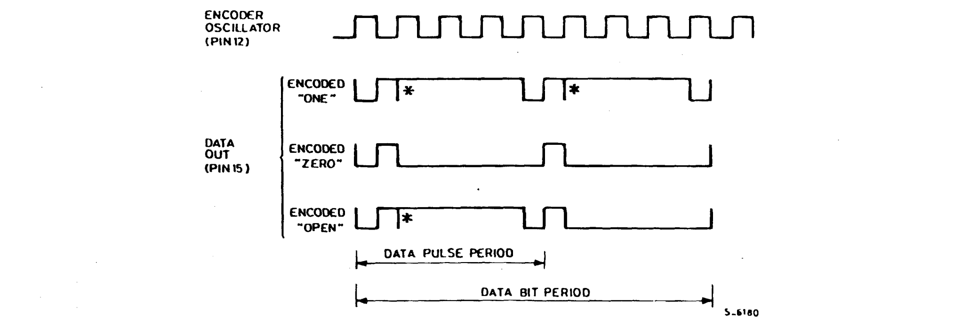
400 pF < CTC < μF

Figure 5 : Encoder/Decoder Timing Diagram.



88DSM145026/27/28-06

Figure 6 : Encoder Data Waveforms (M145026).



* 150 ns Pulse appears at this point (this does not affect the transmitter/receiver operation).

88DSM145026/27/28-07

Figure 7 : M145027 Flowchart.

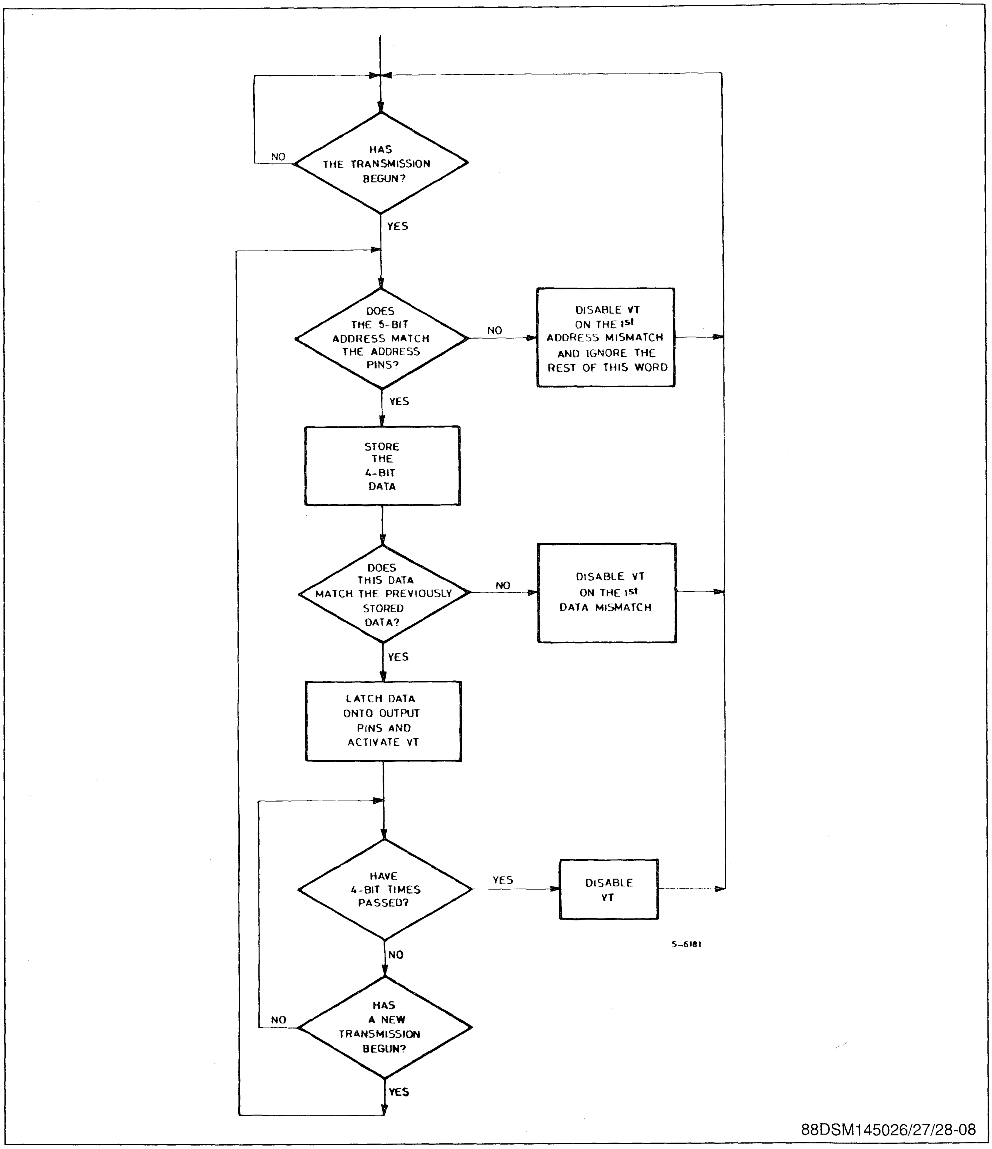
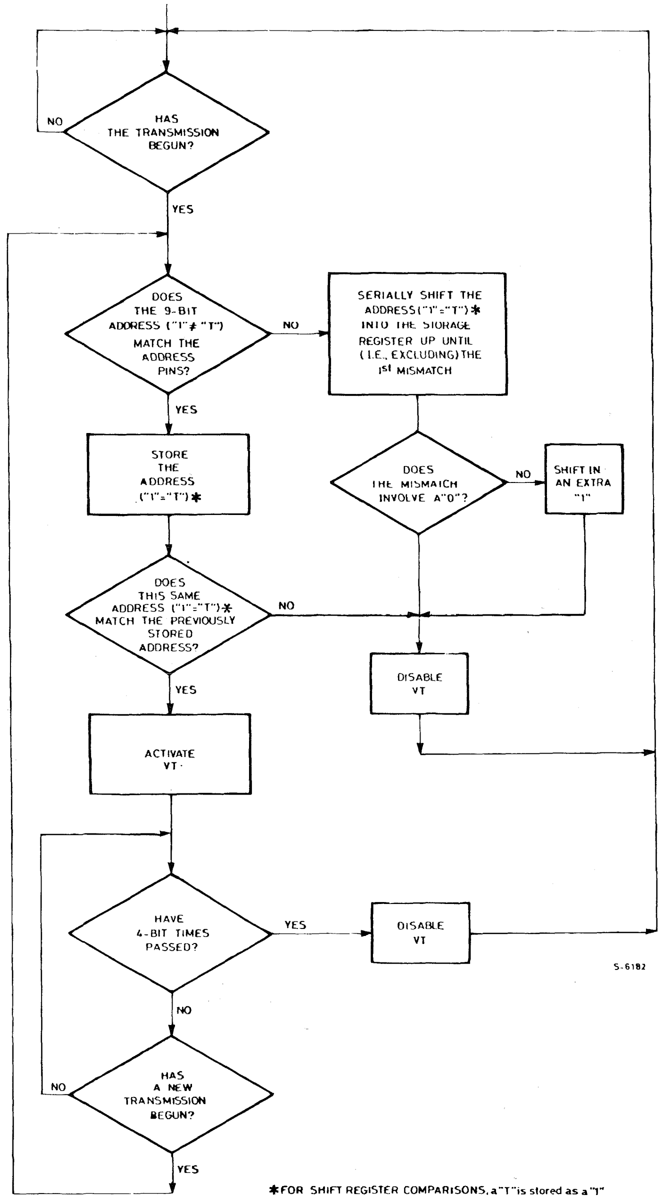
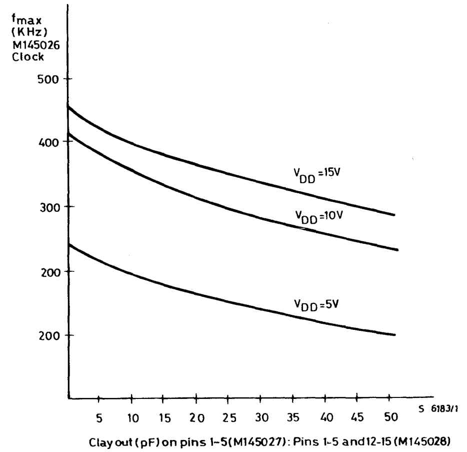


Figure 8 : M145028 Flowchart.



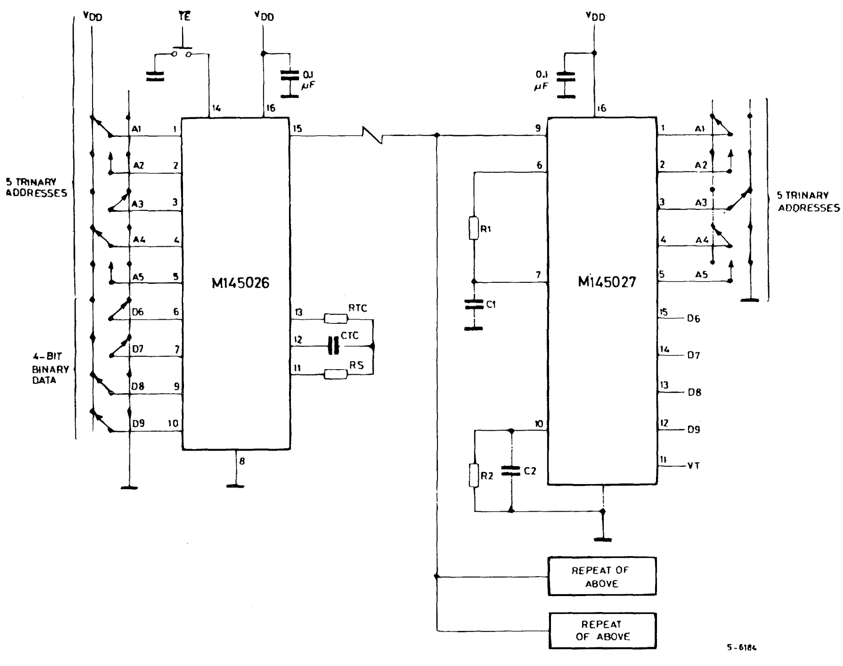
88DSM145026/27/28-09

Figure 9 : M145027/M145028 (f_{max} vs. C_{layout}).



88DSM145026/27/28-010

Figure 10 : Typical Application.



88DSM145026/27/28-11

EXAMPLE R/C VALUES (all resistors and capacitors are ± 5 %)
(CTC' = CTC + 20 pF)

f_{OSC} (kHz)	RTC	CTC'	RS	R1	C1	R2	C2
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 µF
8.53	10 k	5100 pF	20 k	10 k	0.02 µF	200 k	0.02 µF
1.71	50 k	5100 pF	100 k	50 k	0.02 µF	200 k	0.1 µF

7W AUDIO AMPLIFIER

NOT FOR NEW DESIGN

The TBS810P is an improvement of TBA810S.

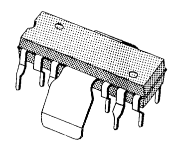
It offers:

- Higher output power (R_L = 4Ω and 2Ω)
- Low noise
- Polarity inversion protection
- Fortuitous open ground protection
- High supply voltage rejection (40dB min.)

The TBA810P is a monolithic integrated circuit in a 12-lead quad in-line plastic package, intended for use as a low frequency class B amplifier.

The TBA810P provides 7W output power at 16V/4Ω; 7W at 14.4/2Ω.

It gives high output current (up to 3A), high efficiency (75% at 60W output) very low harmonic and crossover distortion. The circuit is provided with a thermal limiting circuit and can withstand a short-circuit on the load for supply voltages up to 15V.



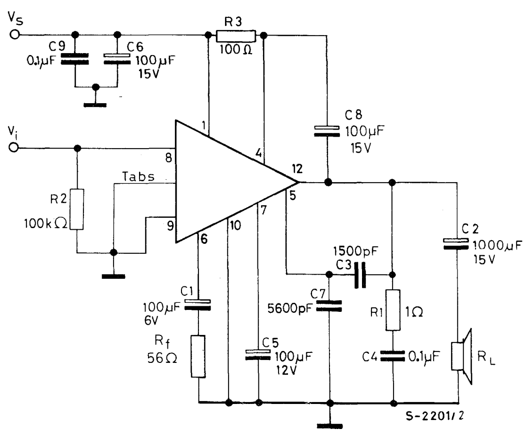
Findip

ORDER CODE: TBA810P

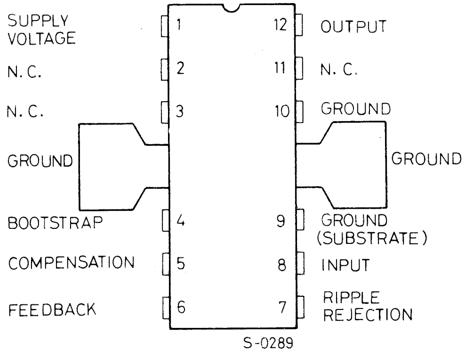
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
I_o	Output peak current (non repetitive)	4	A
I_o	Output peak current (repetitive)	3	A
P_{tot}	Power dissipation at $T_{amb} \leqslant 80°C$	1	W
	$T_{tab} \leqslant 90°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

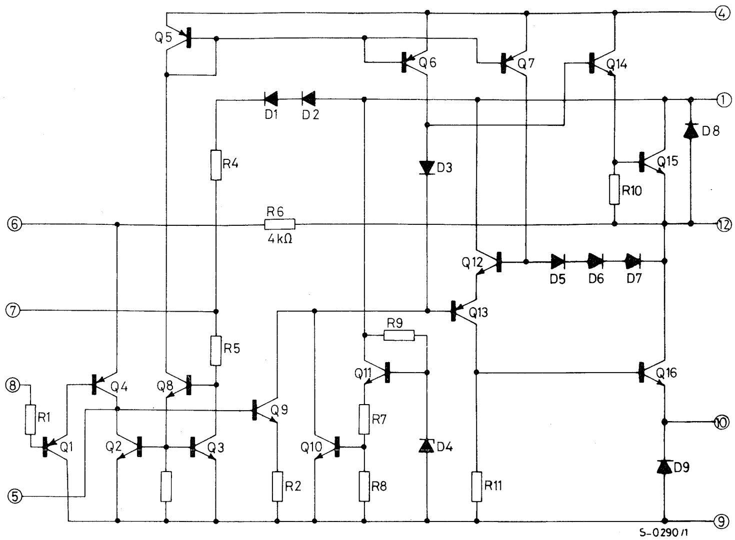
TEST AND APPLICATION CIRCUIT



CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70*	°C/W

* Obtained with tabs soldered to printed circuit with minimized copper area

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; V_s = 14.4V, T_{amb} = 25°C unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 1)		4		20	V
V_o	Quiescent output voltage (pin 2)		6.4	7.2	8	V
I_d	Quiescent drain current			12	20	mA
I_b	Input bias current			0.4		μA
P_o	Output power	d = 10% f = 1KHz R_L = 4Ω R_L = 2Ω	 5.5 5.5	 6 7		 W W
$V_{i\,(rms)}$	Input saturation voltage		220			mV
R_i	Input resistance (pin 8)			5		MΩ
B	Frequency response (-3dB)	R_L = 4Ω/2Ω C_3 = 820pF C_3 = 150pF		 40 to 20,000 40 to 10,000		 Hz Hz
d	Distortion	P_o = 50mW to 2.5W R_L = 4Ω/2Ω f = 1KHz		0.3		%
G_v	Voltage gain (open loop)	R_L = 4Ω f = 1KHz		80		dB
G_v	Voltage gain (closed loop)	R_L = 4Ω/2Ω f = 1KHz	34	37	40	dB
e_N	Input noise voltage	V_s = 16V B (-3dB) = 40 to 15,000Hz		2		μV
i_N	Input noise current			80		pA
η	Efficiency	P_o = 6W R_L = 4Ω f = 1KHz		75		%
SVR	Supply voltage rejection	R_L = 4Ω V_{ripple} = $1V_{rms}$ f_{ripple} = 10Hz	40	48		dB

Fig. 1 - Output power vs. supply voltage

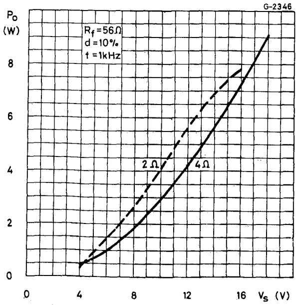


Fig. 2 - Maximum power dissipation vs. supply voltage (sine wave operation)

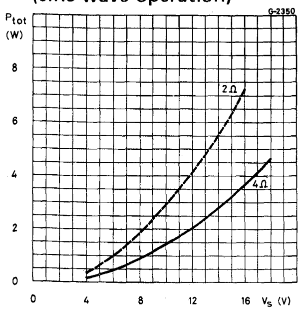
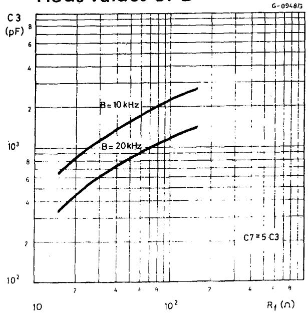


Fig. 3 - Value of C3 vs. feedback resistance for various values of B



SGS-THOMSON MICROELECTRONICS

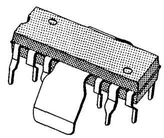
TBA810S

7W AUDIO AMPLIFIER

NOT FOR NEW DESIGN

The TBA810S is a monolithic integrated circuit in a 12-lead quad in-line plastic package, intended for use as a low frequency class B amplifier.

The TBA810A provides 7W power output at 16V/4Ω, 6W at 14.4V/4Ω, 2.5W at 9V/4Ω, 1W at 6V/4Ω and works with a wide range of supply voltage (4 to 20V); it gives high output current (up to 2.5A), high efficiency (75%) at 6W output). very low harmonic and cross-over distortion. In addition, the circuit is provided with a thermal protection circuit.



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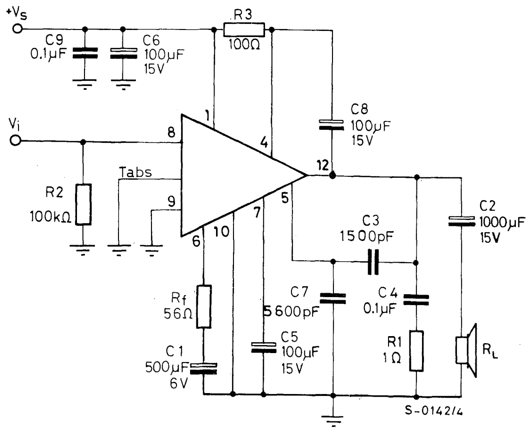
ORDERING NUMBER: TBA810S

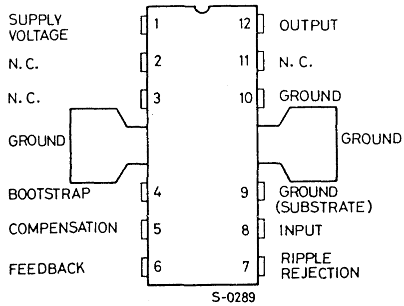
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
I_o	Output peak current (non-repetitive)	3.5	A
I_o	Output current (repetitive)	2.5	A
P_{tot}	Power dissipation: at $T_{amb} \leq 70°C$	1	W
	at $T_{tab} \leq 90°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

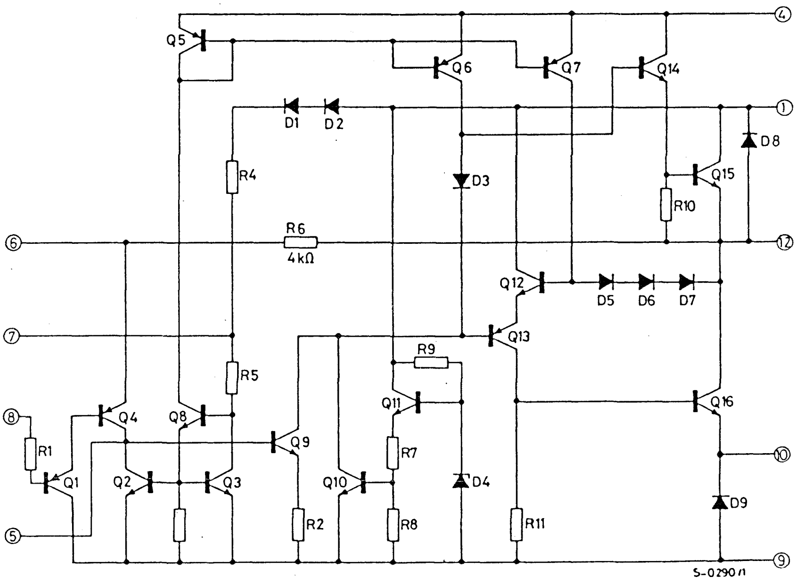
TEST AND APPLICATION CIRCUIT



CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70* °C/W

* Obtained with tabs soldered to printed circuit with minimized copper area.

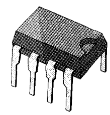
ELECTRICAL CHARACTERISTICS (Refer to the test circuit; $T_{amb} = 25\,°C$)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 1)		4		20	V
V_o	Quiescent output voltage (pin 12)	V_s = 14.4V	6.4	7.2	8	V
I_d	Quiescent drain current	V_s = 14.4V		12	20	mA
I_b	Bias current (pin 8)	V_s = 14.4V		0.4		μA
P_o	Power output	d = 10% R_L = 4Ω f = 1 kHz V_s = 16V V_s = 14.4V V_s = 9V V_s = 6V	 5.5 	 7 6 2.5 1		 W W W W
$V_{i(rms)}$	Input voltage				220	mV
V_i	Input sensitivity	P_o = 6W V_s = 14.4V R_L = 4Ω f = 1kHz R_f = 56Ω R_f = 22Ω		 80 35		 mV mV
R_i	Input resistance (pin 8)			5		MΩ
B	Frequency response (-3 dB)	V_s = 14.4V R_L = 4Ω C3 = 820 pF C3 = 1500 pF		 40 to 20,000 40 to 10,000		 Hz Hz
d	Distorsion	P_o = 50mW to 3W V_s = 14.4V R_L = 4Ω f = 1kHz		0.3		%
G_v	Voltage gain (open loop)	V_s = 14.4V R_L = 4Ω f = 1kHz		80		dB
G_v	Voltage gain (closed loop)	V_s = 14.4V R_L = 4Ω f = 1kHz	34	37	40	dB
e_N	Input noise voltage	V_s = 14.4V R_g = 0 B (-3 dB) = 20Hz to 20,000 Hz		2		μV
i_N	Input noise current	V_s = 14.4V B (-3 dB) = 20 Hz to 20,000 Hz		0.1		nA
η	Efficiency	P_o = 5W V_s = 14.4V R_L = 4Ω f = 1kHz		70		%
SVR	Supply voltage rejection	V_s = 14.4V R_L = 4Ω f_{ripple} = 100 Hz		38		dB

MINIDIP 1.2W AUDIO AMPLIFIER

The TBA820M is a monolithic integrated audio amplifier in a 8 lead dual in-line plastic package. It is intended for use as low frequency class B power amplifier with wide range of supply voltage: 3 to 16V, in portable radios, cassette recorders and players etc. Main features are: minimum working supply voltage of 3V, low quiescent current, low number of external components, good ripple rejection, no cross-over distortion, low power dissipation.

Output power: P_o = 2W at 12V/8Ω, 1.6W at 9V/4Ω and 1.2W at 9V/8Ω.



Minidip Plastic

ORDERING NUMBER: TBA820M

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
I_o	Output peak current	1.5	A
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST AND APPLICATION CIRCUITS

Fig. 1 - Circuit diagram with load connected to the supply voltage

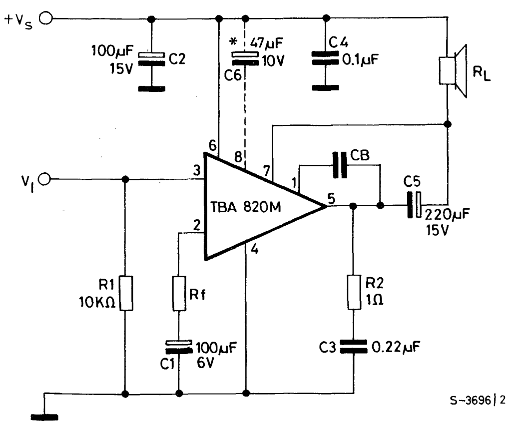
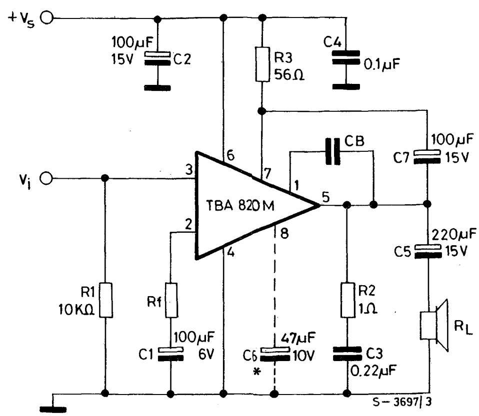


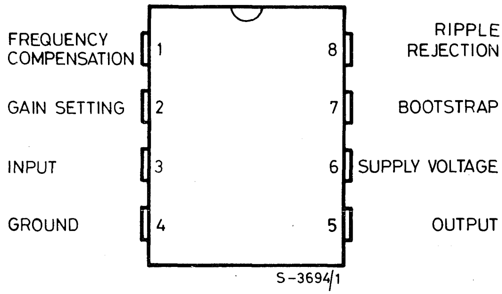
Fig. 2 - Circuit diagram with load connected to ground



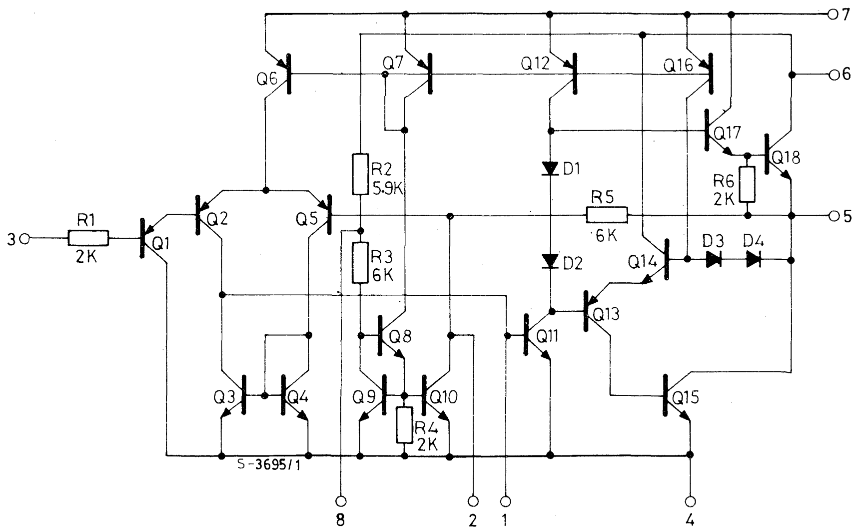
* Capacitor C6 must be used when high ripple rejection is requested.

CONNECTION DIAGRAM

(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits V_s= 9V, T_{amb}= 25°C unless otherwise specified)

	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			3		16	V
V_o	Quiescent output voltage (pin 5)			4	4.5	5	V
I_d	Quiescent drain current				4	12	mA
I_b	Bias current (pin 3)				0.1		μA
P_o	Output power	d = 10% R_f= 120Ω V_s= 12V V_s= 9V V_s= 9V V_s= 6V V_s= 3.5V	f = 1 kHz R_L= 8Ω R_L= 4Ω R_L= 8Ω R_L= 4Ω R_L= 4Ω	 0.9	 2 1.6 1.2 0.75 0.25		 W W W W W
R_i	Input resistance (pin 3)	f = 1 kHz			5		MΩ
B	Frequency response (-3 dB)	R_L= 8Ω C_5 = 1000 μF R_f= 120Ω	C_B= 680 pF	25 to 7,000			Hz
			C_B= 220 pF	25 to 20,000			
d	Distortion	P_o= 500 mW R_L= 8Ω f = 1 kHz	R_f= 33Ω		0.8		%
			R_f= 120Ω		0.4		
G_v	Voltage gain (open loop)	f = 1 kHz	R_L= 8Ω		75		dB
G_v	Voltage gain (closed loop)	R_L= 8Ω	R_f= 33Ω		45		dB
		f = 1 kHz	R_f= 120Ω		34		
e_N	Input noise voltage (∗)				3		μV
i_N	Input noise current (∗)				0.4		nA
$\frac{S+N}{N}$	Signal to noise ratio (∗)	P_o= 1.2W R_L= 8Ω G_v= 34 dB	R1= 10KΩ		80		dB
			R1= 50 kΩ		70		
SVR	Supply voltage rejection (test circuit of fig. 2)	R_L= 8Ω $f_{(ripple)}$ = 100 Hz C6= 47 μF R_f= 120Ω			42		dB

(∗) B = 22 Hz to 22 KHz

Fig. 3 - Output power vs. supply voltage

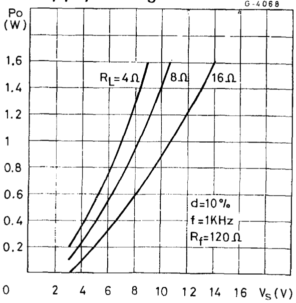


Fig. 4 - Harmonic distortion vs. output power

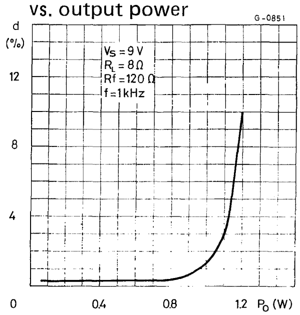


Fig. 5 - Power dissipation and efficiency vs. output power

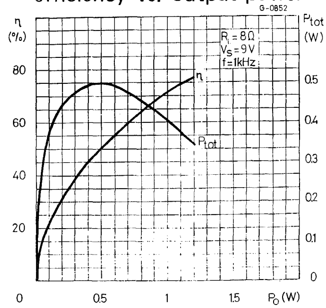


Fig. 6 - Maximum power dissipation (sine wave operation)

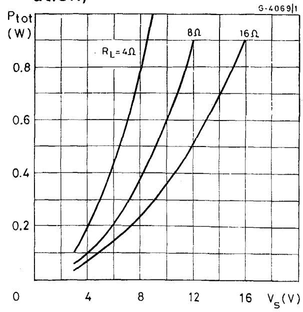


Fig. 7 - Suggested value of C_B vs. R_f

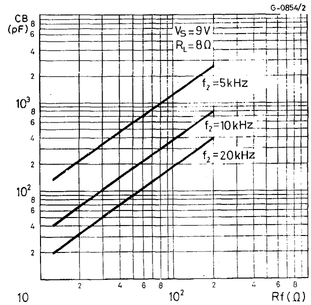


Fig. 8 - Frequency response

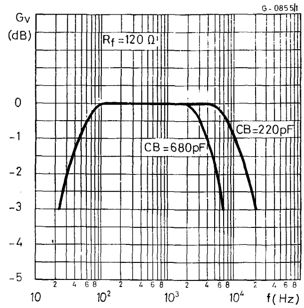


Fig. 9 - Harmonic distortion vs. frequency

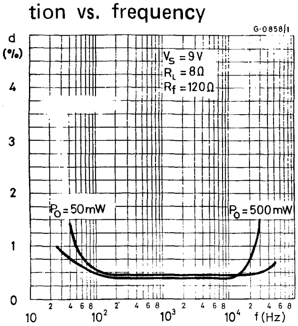


Fig. 10 - Supply voltage rejection (Fig. 2 circuit)

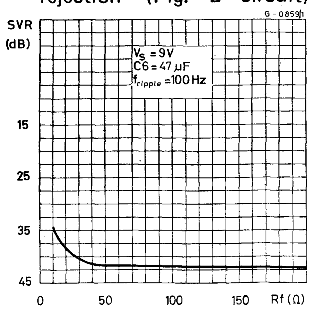
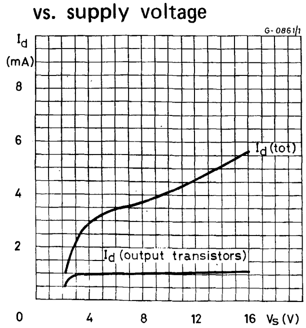


Fig. 11 - Quiescent current vs. supply voltage



SGS-THOMSON MICROELECTRONICS

TCA3189

FM-IF HIGH QUALITY RADIO SYSTEM

- EXCEPTIONAL LIMITING SENSITIVITY
- VERY LOW DISTORTION (0.1% - DOUBLE TUNED DETECTOR COIL)
- IMPROVED S/N RATIO
- EXTERNALLY PROGRAMMABLE AUDIO LEVEL
- ON CHANNEL STEP FOR SEARCH CONTROL
- PROGRAMMABLE AGC VOLTAGE AND AFC FOR TUNER
- INTERCHANNEL MUTING (SQUELCH)
- DEVIATION MUTING
- DIRECT DRIVE OF TUNING METER
- DIRECT DRIVE OF FIELD STRENGTH METER

The TCA3189 is a monolithic integrated circuit in a 16-lead dual in-line plastic package, which provides a **complete subsystem** for amplification of 10.7MHz FM signal in Hi-Fi, car-radios and communications receivers.

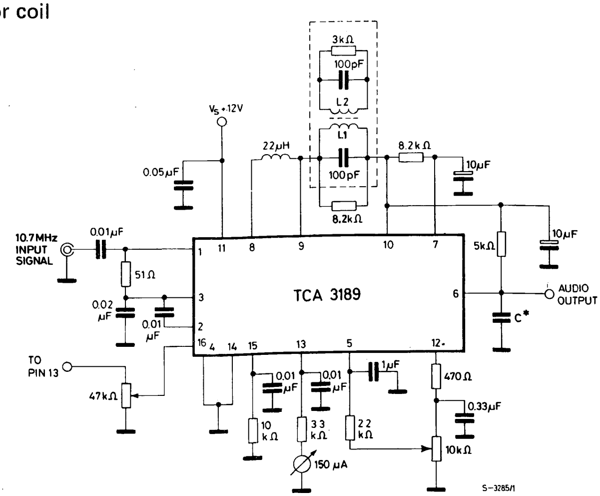
DIP-16 Plastic (0.25)

ORDERING NUMBER: TCA3189

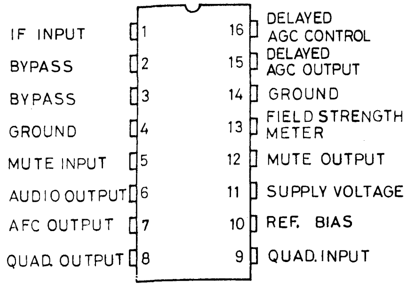
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
I_o	Output current (from pin 15)	2	mA
P_{tot}	Total power dissipation at $T_{amb} \leq 70°C$	800	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating temperature	-25 to 85	°C

Double tuned detector coil

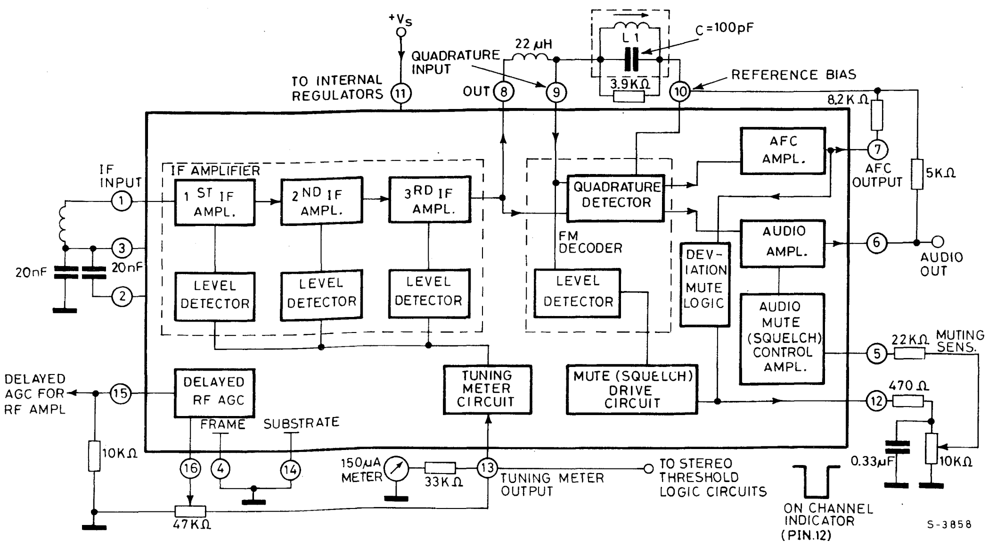


CONNECTION DIAGRAM
(top view)



S-3286

BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max.	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = 12V$, $T_{amb} = 25°C$)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage range	No signal input, non muted		9		16	V
I_s	Supply current			20	31	44	mA
V_1	Voltage at the IF amplifier input			1.2	1.9	2.4	V
V_2, V_3	Voltage at the input bypass			1.2.	1.9	2.4	V
V_{15}	Voltage at the pin 15 (RF AGC)			7.5	9.5	11	V
V_{10}	Reference bias voltage			5	5.6	6	V
V_i	Input limiting voltage (-3 dB) at pin 1	f_o = 10.7 MHz f_m = 1 KHz Δf = ± 75 KHz			12	25	µV
V_o	Recovered audio voltage (pin 6)	$V_i \geq 50\ \mu V$ f_o = 10.7 MHz f_m = 1 KHz Δf = ± 75 KHz		325	500	650	mV
d	Distortion (single tuned)	$V_i \geq 1$ mV f_o = 10.7 MHz f_m = 1 KHz Δf = ± 75 KHz			0.5	1	%
d	Distortion (double tuned)				0.1		%
$\frac{S+N}{N}$	Signal to noise ratio			65	72		dB
AMR	Amplitude modulation rejection	V_i = 100 mV f_o = 10.7 MHz f_m = 1 KHz Δf = ± 75 KHz AM mod. 30%		45	55		dB
V_{16}	RF AGC threshold				1.25		V
$\frac{\Delta I_7}{\Delta f}$	AFC control slope				1.9		$\frac{\mu A}{KHz}$
V_{12}	On channel step (deviation mute)	V_i = 100 mV	$f_{DEV.} <$ ± 40 KHz		0		V
		f_o = 10.7 MHz	$f_{DEV.} >$ ± 40 KHz		5.6		V

TEST CIRCUIT

Fig. 1 – Single tuned detector coil

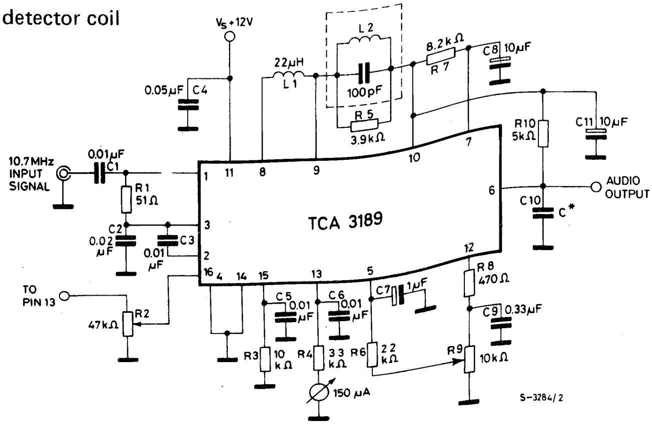


Fig. 2 – Limiting and noise characteristics

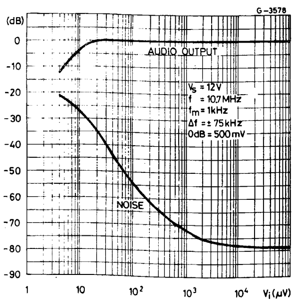


Fig. 3 – Deviation mute threshold vs. R_{7-10}

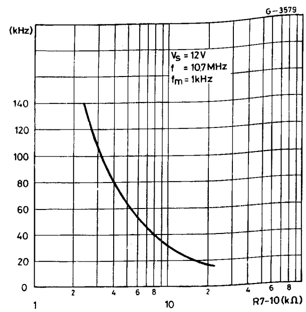


Fig. 4 – Recovered audio and muting action vs. input level

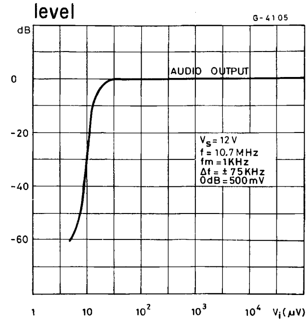


Fig. 5 – AFC characteristics

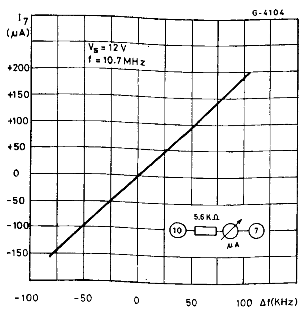


Fig. 6 – AGC voltage for FM tuner vs. input level

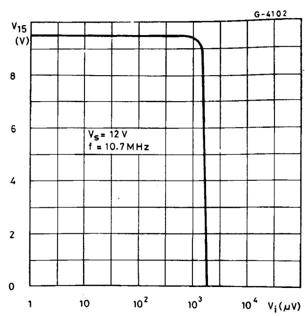
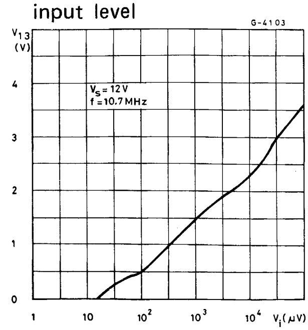


Fig. 7 – Field strength and tuning meter output vs. input level



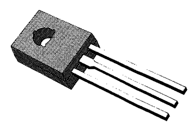
SGS-THOMSON MICROELECTRONICS

TDA1151

MOTOR SPEED REGULATOR

- EXCELLENT VERSATILITY IN USE
- HIGH OUTPUT CURRENT (UP TO 800mA)
- LOW QUIESCENT CURRENT (1.7mA)
- LOW REFERENCE VOLTAGE (1.2V)
- EXCELLENT PARAMETERS STABILITY VERSUS TEMPERATURE

The TDA1151 is a monolithic integrated circuit in SOT-32 plastic package. It is intended for use as speed regulator for DC motors of record players, tape and cassette recorders, movie cameras, toys etc.



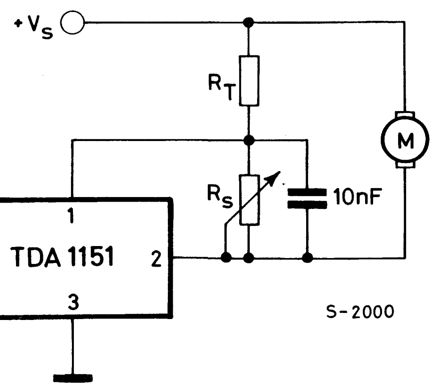
SOT-32

ORDERING NUMBER: TDA1151

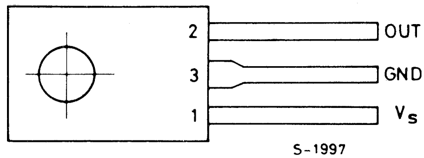
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	0.8	W
	at $T_{case} = 100°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

APPLICATION CIRCUIT

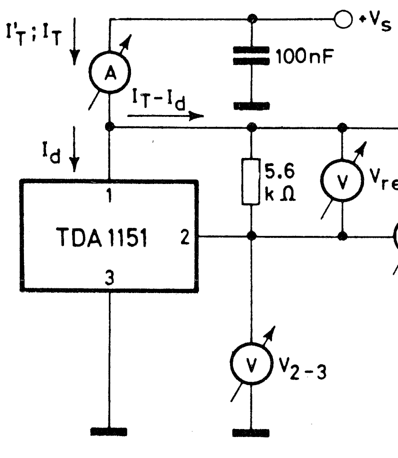


CONNECTION DIAGRAM



tab connected to pin 3

TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction–case	max	10	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_{amb} = 25°C$)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{ref}	Reference voltage (between pins 1 and 2)	$V_s = 6V$ $I_M = 0.1A$	1.1	1.2	1.3	V
I_d	Quiescent drain current	$V_s = 6V$ $I_M = 100\ \mu A$		1.7		mA
I_{MS}	Starting current	$V_s = 5V$ $\Delta V_{ref}/V_{ref} = -50\%$	0.8			A
V_{1-3}	Minimum supply voltage	$I_M = 0.1A$ $\Delta V_{ref}/V_{ref} = -5\%$			2.5	V
$K = I_M/I'_T$	Reflection coefficient	$V_s = 6V$ $I_M = 0.1A$	18	20	22	–
$\frac{\Delta K}{K}/\Delta V_s$		$V_s = 6V$ to $18V$ $I_M = 0.1A$		0.45		%/V
$\frac{\Delta K}{K}/\Delta I_M$		$V_s = 6V$ $I_M = 25$ to $400\ mA$		0.005		%/mA
$\frac{\Delta K}{K}/\Delta T$		$V_s = 6V$ $I_M = 0.1A$ $T_{amb} = -20$ to $70°C$		0.02		%/°C
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta V_s$	Line regulation	$V_s = 6V$ to $18V$ $I_M = 0.1A$		0.02		%/V
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta I_M$	Load regulation	$V_s = 6V$ $I_M = 25$ to $400\ mA$		0.009		%/mA
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta T$	Temperature coefficient	$V_s = 6V$ $I_M = 0.1A$ $T_{amb} = -20$ to $70°C$		0.02		%/°C

Fig. 1 – Quiescent drain current vs. power supply

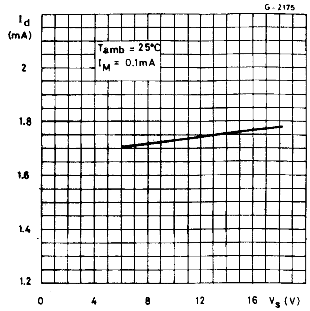


Fig. 2 – Quiescent drain current vs. ambient temperature

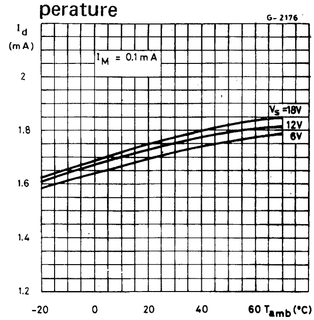


Fig. 3 – Reference voltage vs. supply voltage

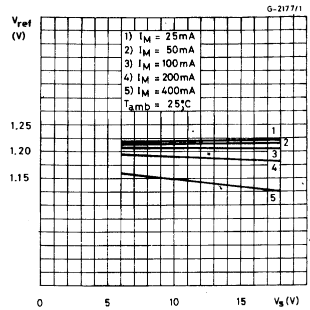


Fig. 4 – Reference voltage vs. motor current

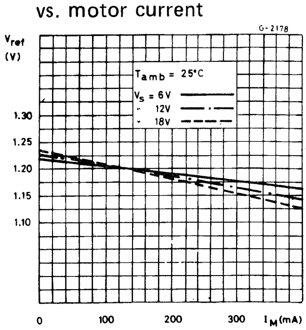


Fig. 5 – Reference voltage vs. ambient temperature

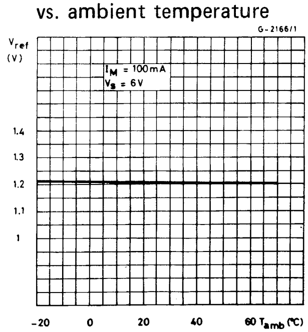


Fig. 6 – Reflection coefficient vs. supply voltage

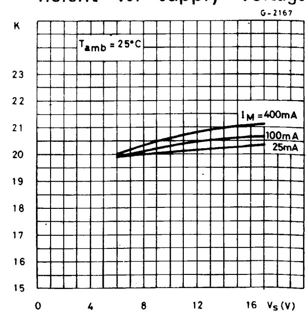


Fig. 7 – Reflection coefficient vs. motor current

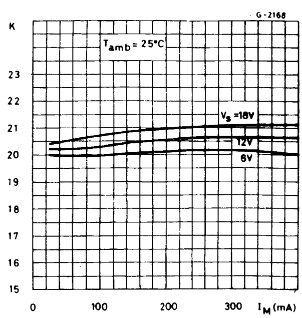


Fig. 8 – Reflection coefficient vs. ambient temperature

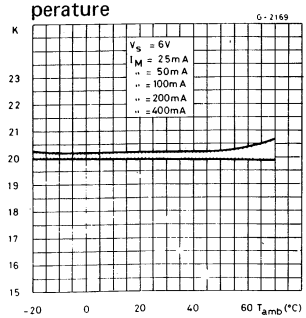
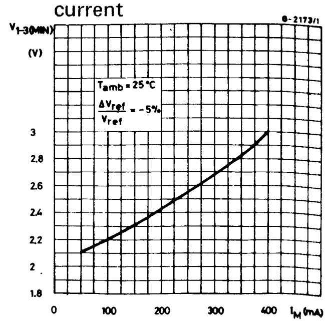
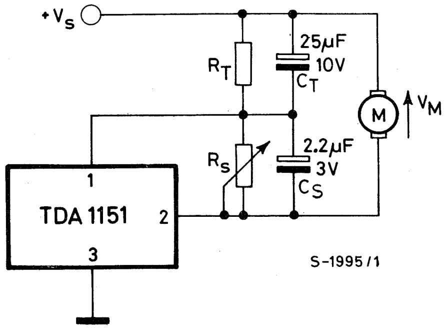


Fig. 9 – Typical minimum supply voltage vs. motor current



SGS-THOMSON MICROELECTRONICS

Fig. 10 – Application circuit



$V_s = +9V$
$R_M = 14.2\Omega$
$R_T = 280\Omega$
$R_S = 1\ k\Omega$
$E_g = 2.9V$
$I_M = 150\ mA$
$V_M = R_M \cdot I_M + E_g = 5.03V$

Note: A ceramic capacitor of 10 nF between pins, 1 and 2 improves stability in some applications.

Fig. 11 – P.C. board and component layout of the circuit of Fig. 10 (1 : 1 scale)

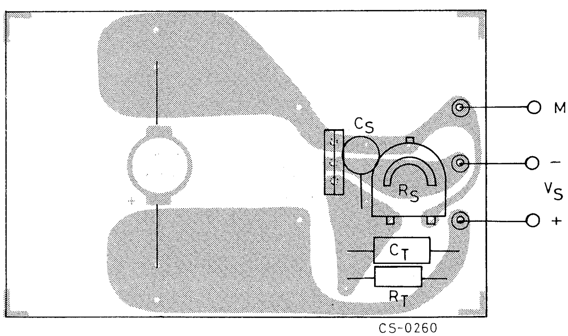


Fig. 12 - Speed variation vs. supply voltage

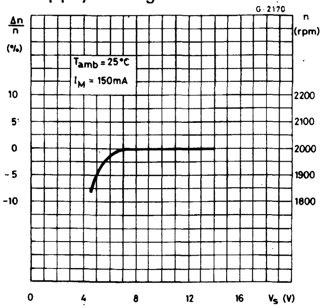


Fig. 13 - Speed variation vs. motor current

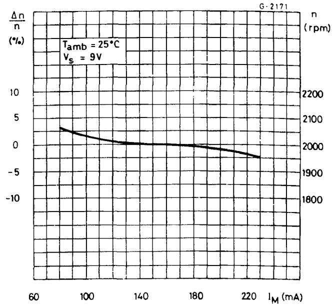


Fig. 14 - Speed variation vs. ambient temperature

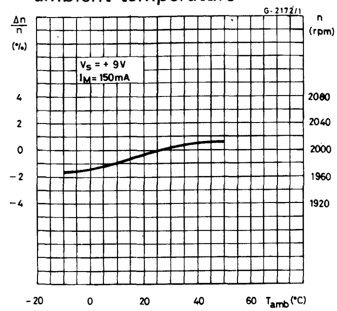
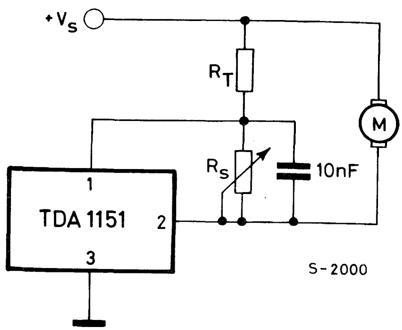


Fig. 15 - Low cost application circuit



V_S = +12V
R_M = 14.7Ω
R_T = 290Ω
R_S = 1 kΩ
E_g = 2.65V
I_M = 110 mA

Fig. 16 - Speed variation vs. supply voltage

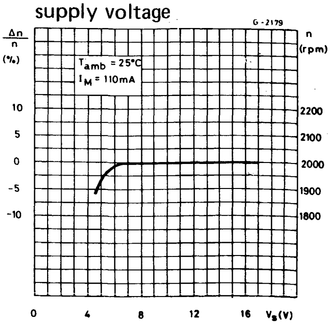


Fig. 17 - Speed variation vs. motor current

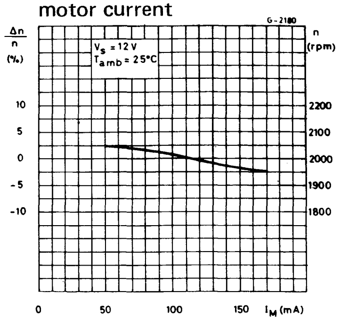
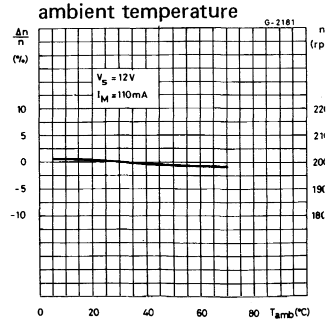


Fig. 18 - Speed variation vs. ambient temperature



SGS-THOMSON MICROELECTRONICS

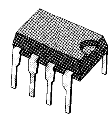
TDA1154

SPEED REGULATOR FOR DC MOTORS

- MATCHING FLEXIBILITY TO MOTORS WITH VARIOUS CHARACTERISTICS
- BUILT-IN CURRENT LIMIT
- ON-CHIP 1.2V REFERENCE VOLTAGE
- STARTING CURRENT: 0.5A @2.5V
- REFLECTION COEFFICIENT K = 20

The TDA1154 is a monolithic integrated circuit intended for speed regulation of permanent magnet dc motors used in record players, tape recorders, cassette recorders and toys.

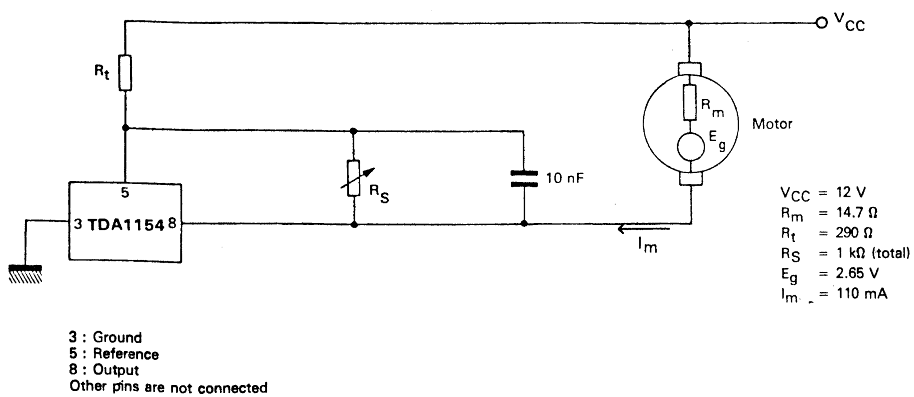
The circuit offers an excellent speed regulation with much higher power supply, temperature and load variations than conventional circuits built around discrete components.



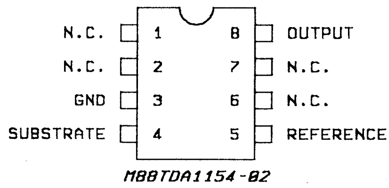
Minidip

ORDER CODE: TDA1154

Fig. 1 - Application circuit



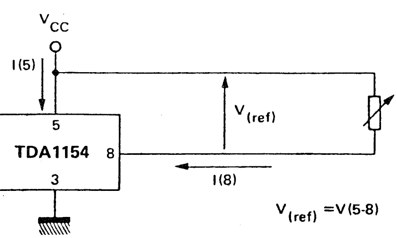
PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	20	V
I_O	Output current	1.2	A
P_{tot}	Power dissipation	(see curve)	W
T_j	Junction temperature	+150	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Fig. 2 - Test circuit



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	100	°C/W
$R_{th\ j-amb}$	Thermal resistance junction-pin 4	max	70	°C/W

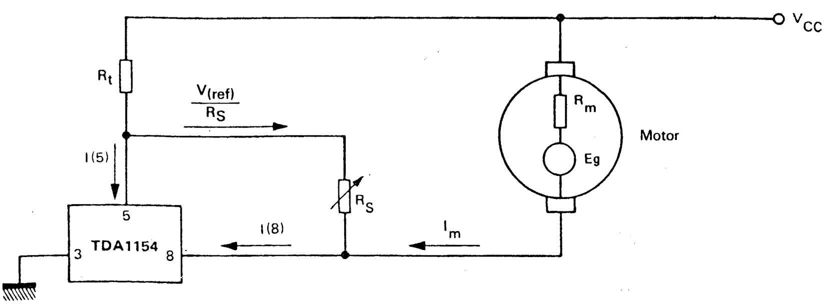
ELECTRICAL CHARACTERISTICS T_{amb} = +25°C (Unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(ref)}$	Reference voltage	V_{CC} = +6V I(8) = 0.1A	1.15	1.25	1.35	V
$\frac{\Delta V_{(ref)}}{V_{(ref)}} / \Delta T$	Reference voltage temperature coefficient	V_{CC} = +6V I(8) = 0.1A T_{amb} = -20°C to +70°C	–	0.02	–	%/°C
$\frac{\Delta V_{(ref)}}{V_{(ref)}} / \Delta V_{CC}$	Line regulator	V_{CC} = +4V to +18V I(8) = 0.1A	–	0.02	–	% /V
$\frac{\Delta V_{(ref)}}{V_{(ref)}} / \Delta I(8)$	Load regulator	V_{CC} = +6V I(8) = 25 to 400 mA	–	0.009	–	% /mA
V (5 - 3)	Minimum supply voltage	I(8) = 0.1A $\frac{\Delta V_{(ref)}}{V_{(ref)}}$ = -5%	2.5	–	–	V
I(8)	Starting current(*)	$\frac{\Delta V_{(ref)}}{V_{(ref)}}$ = -50% V_{CC} = +5V	1.2	–	–	A
		V_{CC} = +2.5V	0.5	0.8	–	A
I_O (5)	Quiescent current on pin 5	V_{CC} = +6V I(8) = 100 μA	–	1.7	–	mA
K	$K = \frac{\Delta I(8)}{\Delta I(5)}$ reflection coefficient	V_{CC} = +6V I(8) = 0.1A	18	20	22	
$\frac{\Delta K}{K} / \Delta V_{CC}$	K spread versus V_{CC}	V_{CC} = +6V to +18V I(8) = 0.1A	–	0.45	–	%/V
$\frac{\Delta K}{K} / \Delta I(8)$	K spread versus I(8)	V_{CC} = +6V I(8) = 25 to 400 mA	–	0.005	–	%/mA
$\frac{\Delta K}{K} / \Delta T$	K spread versus temperature	V_{CC} = +6V I(8) = 0.1A T_{amb} = +20°C to +70°C	–	0.02	–	%/°C

(*) An internal protection circuit reduces the current if the temperature of the junction increase: I(8) = 0.75A at T_j = +140°C.

OPERATING MODE

Fig. 3



The circuit maintains a 1.2V constant reference voltage between pins 5 and 8:

$$V(5 - 8) = V_{(ref)} = 1.2V$$

The current (I(5)) drawn by the circuit at pin 5 is sum of two currents.
One is constant: $I_O(5)$ = 1.7 mA and the other is proportional to pin 8 current (I(8)):

$$I(5) = I_O(5) + I(8)\,K\,(a) \quad (I_O(5) = 1.7\,mA,\ K = 20)$$

If E_g and R_m are motor back electromotive force and motor internal resistance respectively, then:

$$E_g + R_m I_m = R_t \left[I(5) + \frac{V_{(ref)}}{R_S} \right] + V_{(ref)} \quad \text{(b)}$$

From figure 2 it is seen that:

$$I(8) = I_m + \frac{V_{(ref)}}{R_S} \quad \text{(c)}$$

Substituting equations (a) and (c) into (b) yields:

$$E_g = \underbrace{I_m \left[\frac{R_t}{K} - R_m \right]}_{(1)} + \underbrace{V_{(ref)} \left[\frac{R_t}{R_s} \left(1 + \frac{1}{K}\right) + 1 \right] + R_t I_O(5)}_{(2)} \quad \text{(d)}$$

The motor speed will be independent of the resisting torque if E_g is also independent of I_m. Therefore, in order to determine the value of R_t term(1) in (d) must be zero:

$$R_t = K \; R_m \quad (K = 20)$$

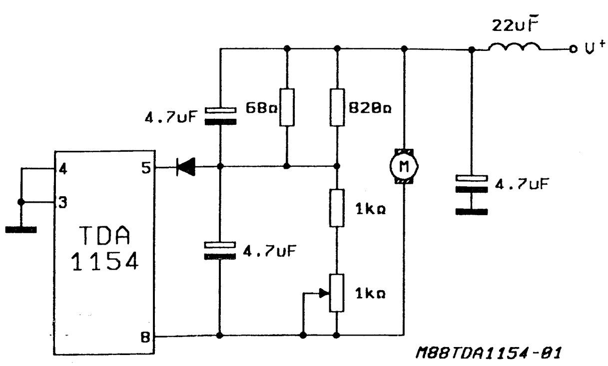
If $R_t > KR_m$, an instability may occur as a result of overcompensation.
The value of R_S is determined by term (2) in (d) so as to obtain the back electromotive force (E_g) corresponding to required motor speed:

$$R_S = R_t \frac{V_{(ref)} \, (1 + 1/K)}{E_g - V_{(ref)} - R_t I_O(5)} \cong$$

$$\cong R_t \frac{V_{(ref)}}{E_g - V_{(ref)} - R_t I_O(5)}$$

Where $V_{(ref)} = 1.2V$ and $I_O(5) = 1.7$ mA

Fig. 4 - Application circuit



AM-FM QUALITY RADIO

The TDA1220B is a monolithic integrated circuit in a 16-lead dual in-line package.

It is intended for quality receivers produced in large quantities.

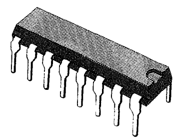
The functions incorporated are:

AM SECTION
- Preamplifier and double balanced mixer
- One pin local oscillator
- IF amplifier with internal AGC
- Detector and audio preamplifier

FM SECTION
- IF amplifier and limiter
- Quadrature detector
- Audio preamplifier

The TDA1220B is suitable up to 30MHz AM and for FM bands (including 450KHz narrow band) and features:
- Very constant characteristics (3V to 16V)
- High sensitivity and low noise
- Very low tweet
- Very high signal handling (1V)
- Sensitivity regulation facility (*)
- High recovered audio signal suited for stereo decoders and radio recorders
- Very simple DC switching of AM-FM
- Low current drain
- AFC facility

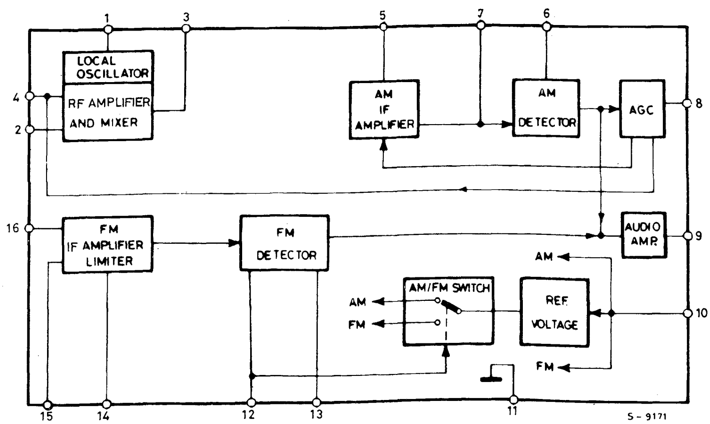
(*) Maximum AM sensitivity can be reduced by means of a resistor (5 to 12KΩ) between pin 4 and ground.



DIP-16 Plastic
(0.25)

ORDERING NUMBER: TDA1220BK

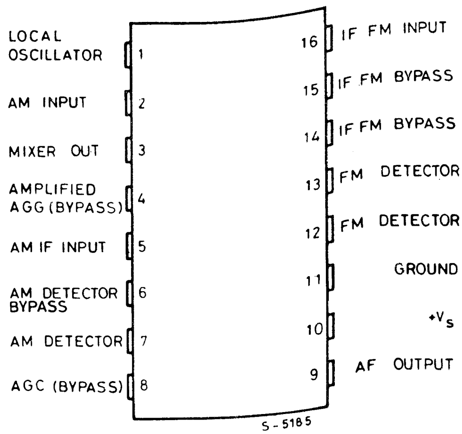
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
P_{tot}	Total power dissipation at $T_{amb} < 110°C$	400	mW
T_{op}	Operating temperature	-20 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 9V unless otherwise specified, refer to test circuit)

Parameter		Test conditions		Min.	Typ	Max	Unit
V_s	Supply voltage			3		16	V
I_d	Drain current	FM			10	15	mA
		AM			14	20	mA

AM SECTION (f_o = 1 MHz; f_m = KHz)

V_i	Input sensitivity	S/N = 26 dB	m = 0.3		12	25	μV
S/N		V_i = 10 mV	m = 0.3	45	52		dB
V_i	AGC range	ΔV_{out} = 10 dB	m = 0.8	94	100		dB
V_o	Recovered audio signal (pin 9)	V_i = 1 mV	m = 0.3	80	130	200	mV
d	Distortion	V_i = 1 mV	m = 0.3		0.4	1	%
			m = 0.8		1.2		%
V_H	Max input signal handling capability	m = 0.8	d < 10%	1			V
R_i	Input resistance between pins 2 and 4	m = 0			7.5		KΩ
C_i	Input capacitance between pins 2 and 4	m = 0			18		pF
R_o	Output resistance (pin 9)			4.5	7	9.5	KΩ
	Tweet 2 IF	m = 0.3	V_i = 1 mV		40		dB
	Tweet 3 IF				55		dB

FM SECTION (f_o = 10.7 MHz; f_m = 1 KHz)

V_i	Input limiting voltage	-3 dB limiting point			22	36	μV
AMR	Amplitude modulation rejection	Δf = ± 22.5 KHz, V_i = 3 mV	m = 0.3	40	50		dB
S/N	Ultimate quieting	Δf = ± 22.5 KHz	V_i = 1 mV	55	65		dB
d	Distortion	Δf = ± 75 KHz	V_i = 1 mV		0.7	1.5	%
d	Distortion	Δf = ± 22.5 KHz	V_i = 1 mV		0.25	0.5	%
d	Distortion (double tuned)				0.1		%
V_o	Recovered audio signal (pin 9)	Δf = ± 22.5 KHz	V_i = 1 mV	80	110	140	mV
R_i	Input resistance between pin 16 and ground				6.5		KΩ
C_i	Input capacitance between pin 16 and ground				14		pF
R_o	Output resistance (pin 9)			4.5	7	9.5	KΩ

Fig. 1 - Test circuit

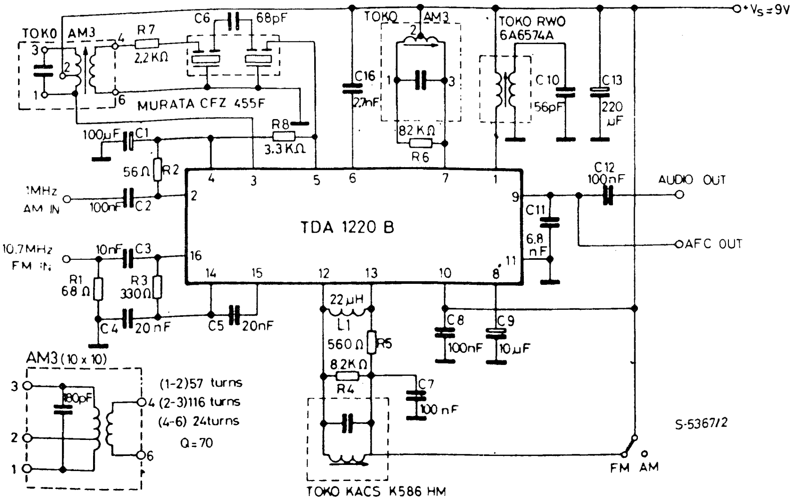


Fig. 2 - PC board and component layout (1:1 scale) of the test circuit.

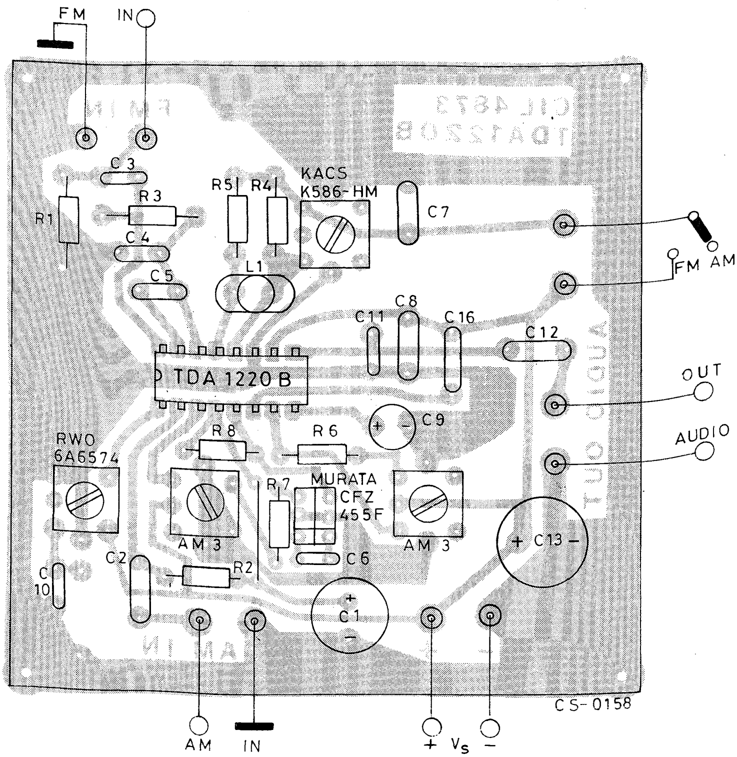


Fig. 3 - Audio output, noise and tweet levels vs. input signal (AM section)

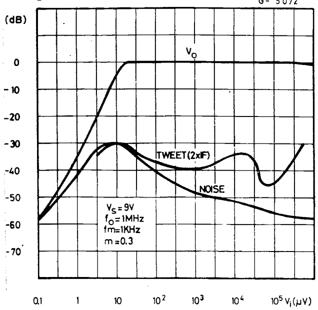


Fig. 4 - Distortion vs input signal and modulation index (AM section)

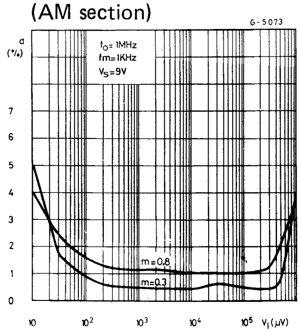


Fig. 5 - Audio output vs. supply voltage (AM section)

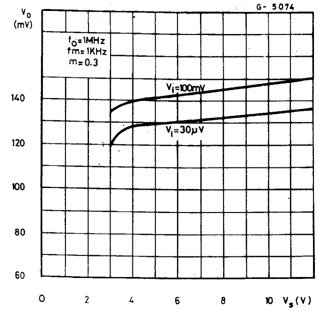


Fig. 6 - Audio output and noise level vs. input signal (FM section)

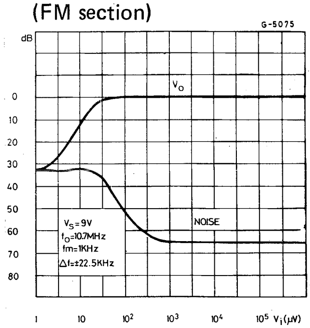


Fig. 7 - Distortion vs. input signal (FM section)

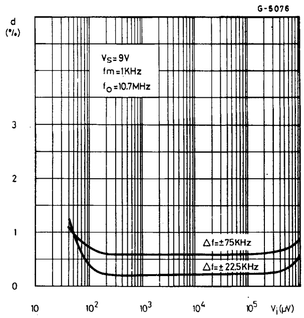


Fig. 8 - Audio output vs. supply voltage (FM section)

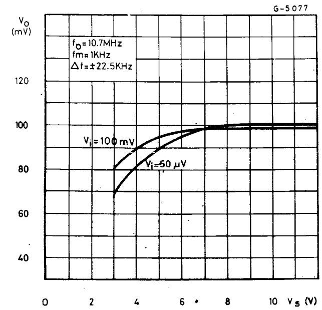


Fig. 9 - Amplitude modulation rejection vs. input signal (FM section)

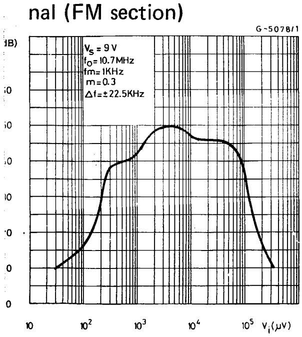


Fig. 10 - ΔDC output voltage (pin. 9) vs. frequency shift (FM section)

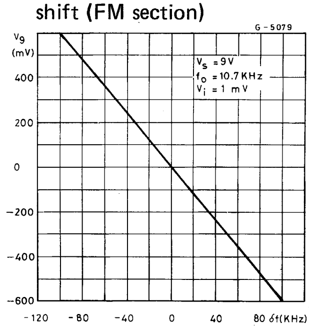
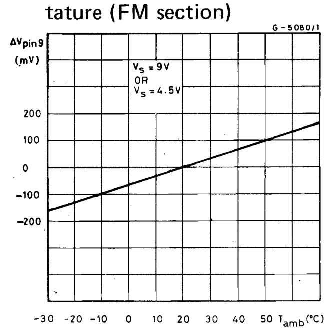


Fig. 11 - ΔDC output voltage (pin 9) vs. ambient tempetature (FM section)



APPLICATION INFORMATION

AM Section

RF Amplifier and mixer stages

The RF amplifier stage (pin 2) is connected directly to the secondary winding of the ferrite rod antenna or input tuned circuit. Bias is provided at pin 4 which must be adequately decoupled. The RF amplifier provides stable performance extending beyond 30 MHz.
The Mixer employed is a double - balanced multiplier and the IF output at pin 3 is connected directly to the IF filter coil.

Local oscillator

The local oscillator is a cross coupled differential stage which oscillates at the frequency determined by the load on pin 1.
The oscillator resonant circuit is transformer coupled to pin 1 to improve the Q factor and frequency stability.
The oscillator level at pin 1 is about 100 mV rms and the performance extends beyond 30 MHz, however to enhance the stability and reduce to a minimum pulling effects of the AGC operation or supply voltage variations, a high C/L ratio should be used above 10 MHz.
An external oscillator can be injected at pin 1. The level should be 50 mV rms and pin 1 should be connected to the supply via a 100Ω resistor.

IF Amplifier Detector

The IF amplifier is a wide band amplifier with a tuned output stage.
The IF filters can be either LC or mixed LC/ceramic.
AM detection occurs at pin 7. A detection capacitor is connected to pin 6 to reduce the radiation of spurious detector products.
The Audio output is at pin 9 (for either AM or FM); the IF frequency is filtered by an external capacitor which is also used as the FM mono de-enphasis network. The audio output impedance is about 7KΩ and a high impedance load (~ 50KΩ) must be used.

AGC

Automatic gain control operates in two ways.
With weak signals it acts on the IF gain, maintaining the maximum S/N. For strong signals a second circuit intervenes which controls the entire chain and allows signal handling in excess of one volt (m = 0.8).
At pin 8 there is a carrier envelope signal which is filtered by an external capacitor to remove the Audio and RF content and obtain a mean DC signal to drive the AGC circuit.

APPLICATION INFORMATION (continued)

FM Section

IF Amplifier and limiter

The 10.7 MHz IF signal from the ceramic filter is amplified and limited by a chain of four differential stages.
Pin 16 is the amplifier input and has a typical input impedance of 6.5 KΩ in parallel with 14 pF at 10.7 MHz.
Bias for the first stage is available at pin 14 and provides 100% DC feedback for stable operating conditions. Pin 15 is the second input to the amplifier and is decoupled to pin 14, which is grounded by a 20 nF capacitor.
An RLC network is connected to the amplifier output and gives a 90° phase shift (at the IF centre frequency) between pins 13 and 12. The signal level at pin 13 is about 150 mV rms.

FM Detector

The circuit uses a quadrature detector and the choise of component values is determined by the acceptable level of distortion at a given recovered audio level.
With a double tuned network the linearity improves (distortion is reduced) and the phase shift can be optimized; however this leads to a reduction in the level of the recovered audio. A satisfactory compromise for most FM receiver applications is shown in the test circuit.

Care should be taken with the physical layout.
The main recommandations are:

- Locate the phase shift coil as near as possible to pin 13.
- Shunt pins 14 and 16 with a low value resistor (between 56Ω and 330Ω).
- Ground the decoupling capacitor of pin 14 and the 10.7 MHz input filter at the same point.

AM-FM Switching

AM-FM switching is achieved by applying a DC voltage at pin 13, to switch the internal reference.

Typical DC voltages (refer to the test circuit)

Pins	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Unit
AM	9	1.4	9	1.4	1.4	8.4	9	0.7	1.9	9	0	0.1	0.1	8.5	8.5	8.5	V
FM	9	0.02	9	0.02	0.02	8.5	9	0	1.7	9	0	9	9	8	8	8	V

APPLICATION SUGGESTION

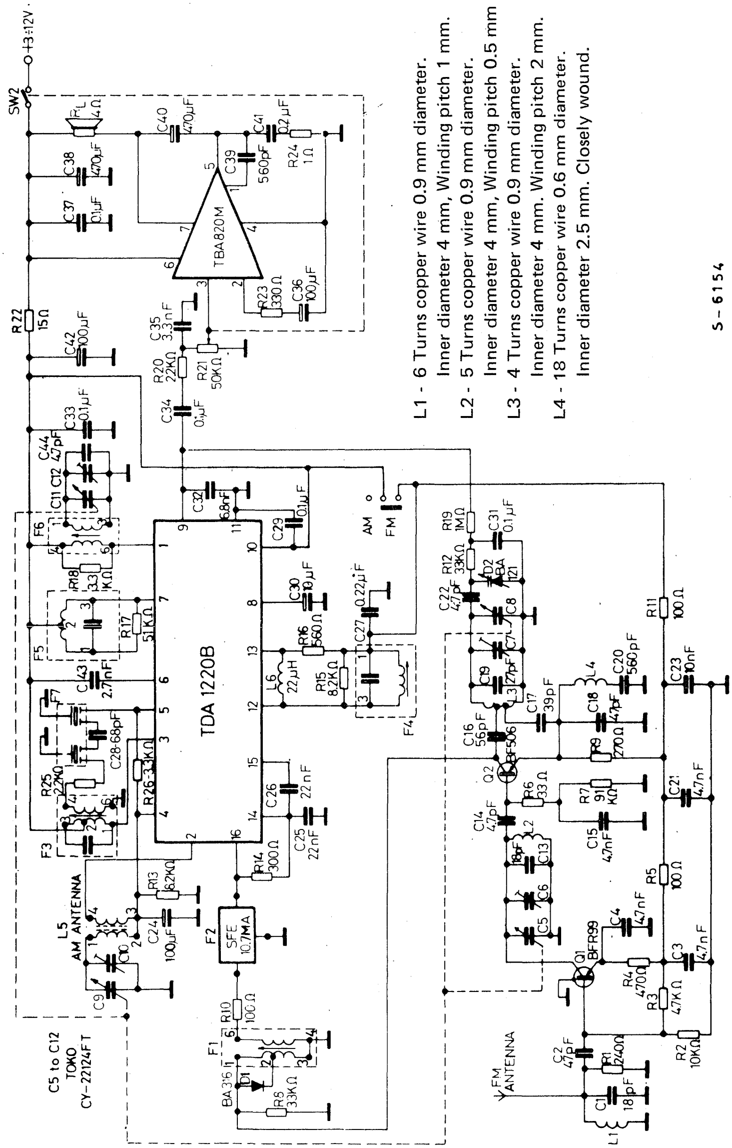
Reccomended values are referred to the test circuit of Fig. 2

Part number	Recommended value	Purpose	Smaller than recommended value	Larger than recommended value
C1	100 μF	AGC bypass	Increase of the distortion at low audio frequency	Increase of the AGC time constant
C2 (*)	100 nF	AM input DC cut		
C3 (*)	10 nF	FM input DC cut		
C4 C5	20 nF 20 nF	FM amplifier bypass	Reduction of sensitivity	– Bandwidth increase – Higher noise
C6	68 pF	Ceramic filter coupling	IF bandwidth reduction	IF bandwidth increase
C7	100 nF	FM detector decoupling	Danger of RF irradiation	
C8	100 nF	Power supply bypass	Noise increase of the audio output	
C9	10 μF	AGC bypass	Increase of the distortion at low audio frequency	Increase of the AGC time constant
C10 (*)	56 pF	Tuning of the AM oscillator at 1455 KHz		
C11	6.8 nF	50 μs FM de-enphasis		
C12	100 nF	Output DC decoupling	Low audio frequency cut	
C13	220 μF	Power supply decoupling	Increase of the distortion at low frequency	
C16	2.7 nF	AM detector capacitor	Low suppression of the IF frequency and harmonics	Increase of the audio distortion
R1 (*)	68 ohm	FM input matching		
R2 (*)	56 ohm	AM input matching		
R3	330 ohm	Ceramic filter matching		
R4	8.2 Kohm	FM detector coil Q setting	Audio output decrease and lower distortion	Audio output increase and higher distortion
R5	560 ohm	FM detector load resistor	Audio output decrease and higher AMR	
R6	82 Kohm	AM detector coil Q setting	Lower IF gain and Lower AGC range	Higher IF gain and lower AGC range
R7	2.2 Kohm	455 KHz IF filter matching		
R8	3.3 Kohm	455 KHz IF filter matching		

(*) Only for test circuit

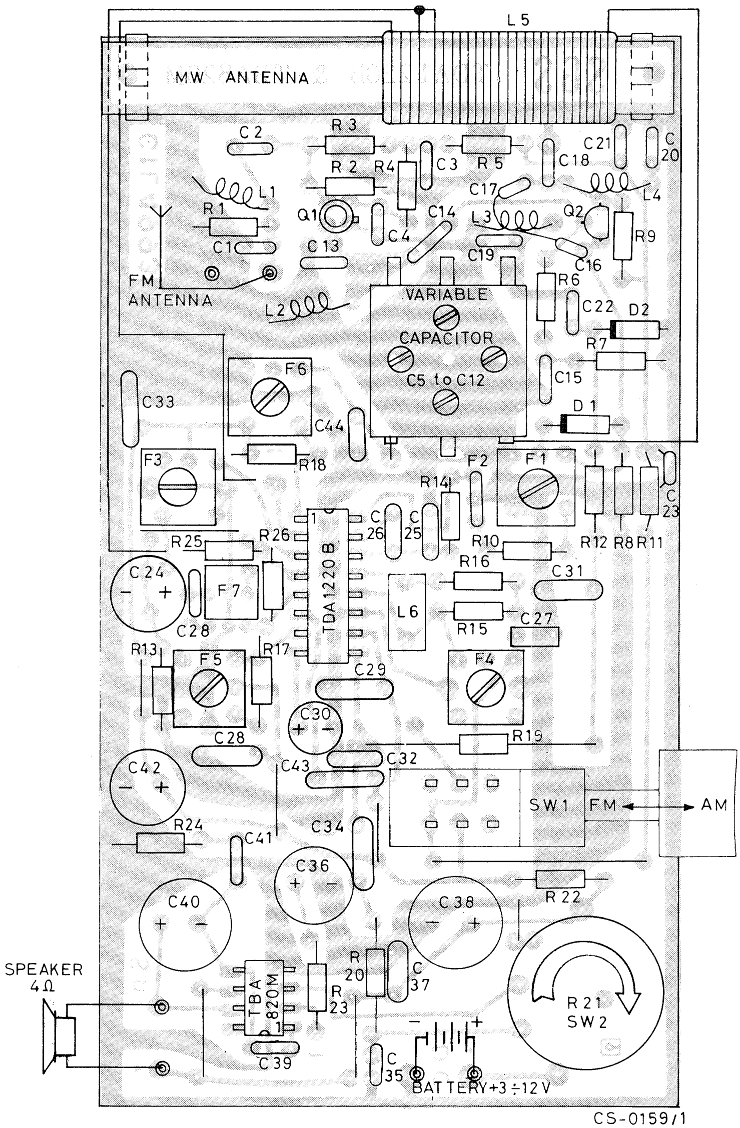
APPLICATION INFORMATION (continued)

Fig. 12 - Portable AM/FM radio



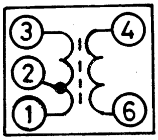
APPLICATION INFORMATION (continued)

Fig. 13 - PC board and component layout of the fig. 12 1:1 scale



APPLICATION INFORMATION (continued)

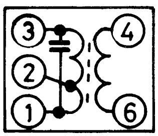
F1 – 10.7 MHz IF Coil



C_O (pF)	f (MHz)	Q_O	TURNS		
–		1-3	1-2	2-3	4-6
–	10.7	110	6	8	2

TOKO - FM1 - 10x10 mm.
154 AN - 7A5965R

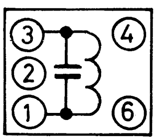
F3 and F5 - 455 KHz IF Coil



C_O (pF)	f (kHz)	Q_O	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	70	57	116	24

TOKO - AM3 - 10x10 mm.
RLC - 4A7525N

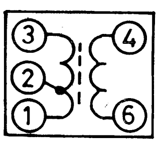
F4 – FM Detector Coil



C_O (pF)	f (MHz)	Q_O	TURNS		
1-3		1-3	1-3	–	–
82	10.7	100	12	–	–

TOKO - 10x10 mm.
KACS - K586 HM

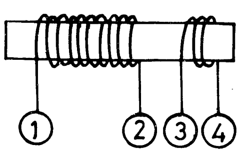
F6 – AM Oscillator Coil



f (kHz)	L (μH)	Q_O	TURNS		
	1-3	1-3	1-2	2-3	4-6
796	220	80	2	75	8

TOKO -10x10 mm
RWO + 6A6574N

L5 – Antenna Coil



S-6161

f (KHz)	L (μH)	Q_O	TURNS	
	1-2	1-2	1-2	3-4
796			105	7

WIRE: LITZ - 15x0.05 mm.
CORE: 10x80 mm.

APPLICATION INFORMATION (continued)

Typical performance of the radio receiver of fig.12 (V_s = 9V)

Parameter		Test Conditions		Value
WAVEBANDS	FM			87.5 to 108 MHz
	AM			510 to 1620 KHz
SENSITIVITY	FM	S/N = 26dB	Δf = 22.5KHz	1 μV
	AM	S/N = 6dB	m = 0.3	1 μV
	AM	S/N = 26dB	m = 0.3	10 μV
DISTORTION (fm = 1KHz)	FM	P_o = 0.5W	Δf = 22.5KHz	0.25%
			Δf = 75KHz	0,7%
	AM	V_i = 100 μV	m = 0.3	0.4%
			m = 0,8	0,8%
SIGNAL TO NOISE (fm = 1KHz)	FM	P_o = 0.5W V_i = 100 μV	Δf = 22.5KHz	64 dB
	AM	P_o = 0.5W V_i = 1 mV	m = 0.3	50dB
AMPLITUDE MODULATION REJECTION	FM	V_i = 100 μV	Δf = 22.5KHz m = 0.3	50dB
TWEET	2nd H.	f = 911 KHz		0.3%
	3rd H.	f = 1370 KHz		0.07%
QUIESCENT CURRENT				20mA
SUPPLY VOLTAGE RANGE				3 to 12V

APPLICATION INFORMATION (continued)

Fig. 14 - Low cost 27 MHz receiver

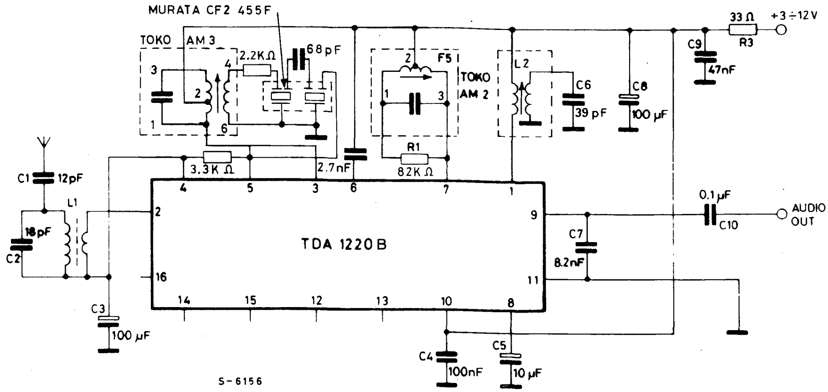
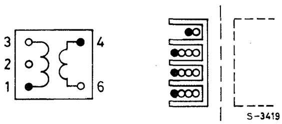
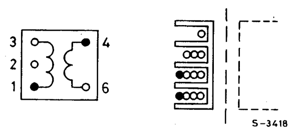


Fig. 15 - L2 Oscillator coil



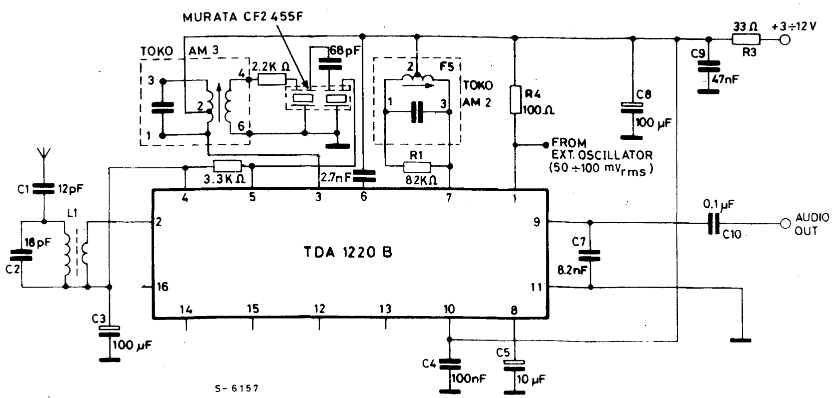
Coil support: Toko 10K
Primary winding: 10 Turns of enamelled copper wire 0.16 mm diameter (pins 3-1).
Secondary winding: 4 Turns copper wire 0.16 mm diameter (pins 6-4)

Fig. 16 - L1 Antenna Coil



Coil support: Toko 10K.
Primary winding: as L2 (pins 3-1)
Secondary winding: 2 Turns copper wire 0.16 mm diameter (pins 6-4)

Fig. 17 - Low cost 27 MHz receiver with external xtal oscillator



APPLICATION INFORMATION (continued)

Fig. 18 - 455 KHz FM narrow band IF

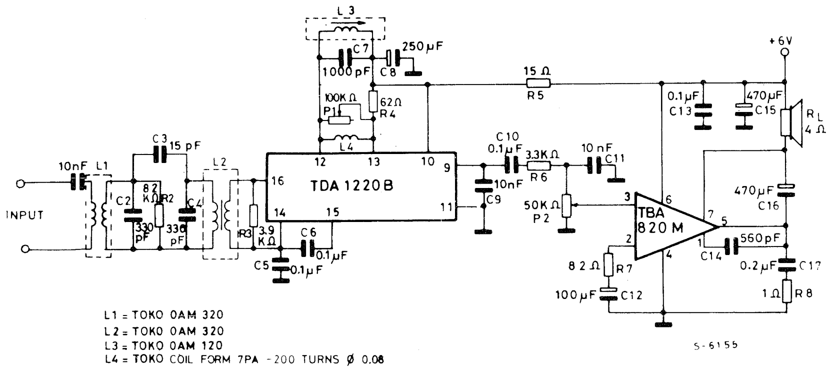
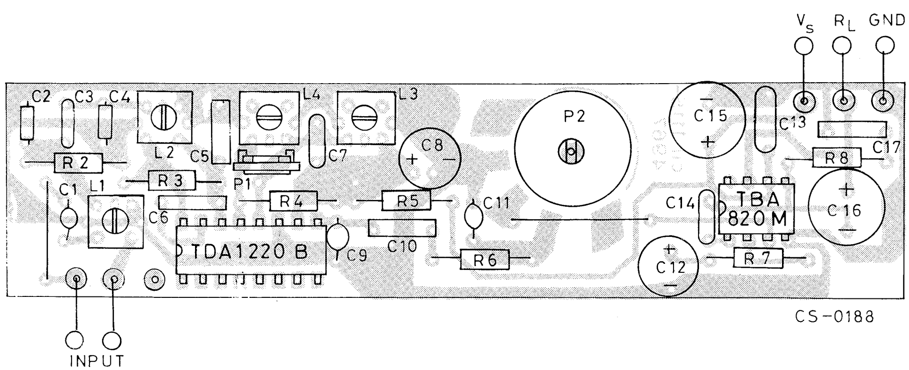


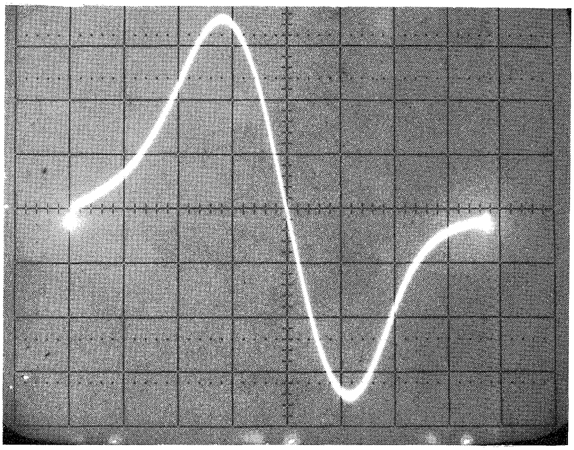
Fig. 19 - P.C. board and component layout of the circuit of fig. 18



APPLICATION INFORMATION (continued)

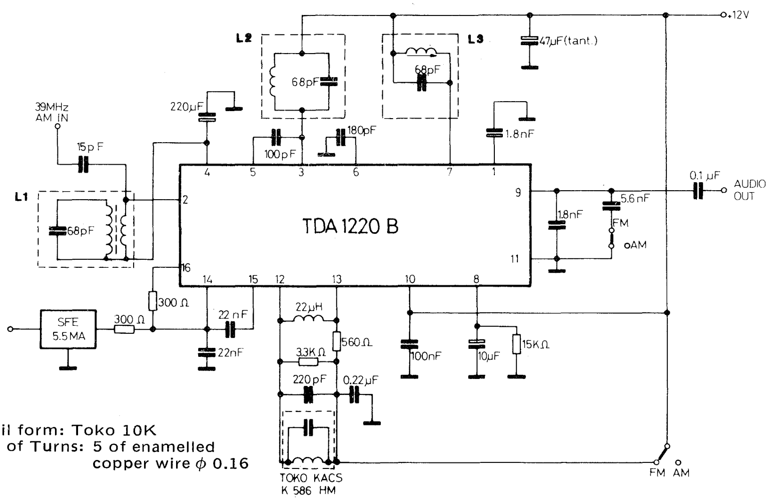
Fig. 20 - Discriminator "S" curve response (circuit of fig. 18)

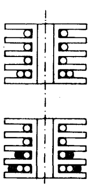
20 mV/div



8 KHz/div

Fig. 21 - Application in sound channel of multistandard TV or in parallel AM modulated sound channel (AM section only).





L2, L3 — Coil form: Toko 10K
N° of Turns: 5 of enamelled copper wire φ 0.16

L1 — Coil form: Toko 10K
N° of Turns: 5+2 of enamelled copper wire φ 0.16

ELECTRICAL CHARACTERISTICS (V_s = 12V)

AM Section (f_o = 39MHz; f_m = 15KHz)

Parameter	Typ	Unit
Audio out (m = 0.3)	60	mV
S/N (V_i = 100 μV; m = 0.3)	37	dB
S/N (V_i = 1mV; m = 0.3)	55	dB
S/N (V_i = 10mV; m = 0.3)	56	dB
AGC range (m = 0.8, ΔVout = 3dB)	65	dB
Max input signal handling (m = 0.8; d = 5%)	150	mV
–3dB bandwidth	600	KHz
Distortion (V_i = 100 μV; m = 0.3)	2	%
(V_i = 1mV; m = 0.3)	1	%
(V_i = 10mV; m = 0.3)	0.8	%
(V_i = 100 μV; m = 0.8)	7	%
(V_i = 1mV; m = 0.8)	5	%
(V_i = 10mV; m = 0.8)	3	%

FM Section (f_o = 5.5MHz; f_m = 1KHz)

Parameter	Typ	Unit
–3dB input limiting voltage (Δf = 25KHz)	3	μV
AMR (Δf = +25KHz; m = 0.3; V_i = 100 μV)	40	dB
(Δf = +25KHz; m = 0.3; V_i = 1mV)	58	dB
(Δf = +25KHz; m = 0.3; V_i = 10mV)	54	dB
S/N (Δf = ±25KHz; V_i = 100 μV)	51	dB
S/N (Δf = ±25KHz; V_i = 1mV)	70	dB
S/N (Δf = ±25KHz; V_i = 10mV)	70	dB
Distortion (Δf = ±25KHz; V_i = 100 μV)	0.5	%
(Δf = ±25KHz; V_i = 1mV)	0.6	%
(Δf = ±25KHz; V_i = 10mV)	0.6	%
(Δf = ±50KHz; V_i = 100 μV)	1	%
(Δf = ±50KHz V_i = 1mV)	1	%
(Δf = ±50KHz; V_i = 10mV)	1	%
Recovered audio (Δf = ±15KHz; V_i = 1mV) (Recovered audio can be varied by variation of 3.3K ohm resistor in parallel with the discriminator coil)	70	mV
Max input signal handling	1	V

Note: AM performance at 39MHz can be improved by mean of a selective preamplifier stage.

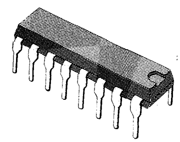
SGS-THOMSON MICROELECTRONICS

TDA1904

4W AUDIO AMPLIFIER

- HIGH OUTPUT CURRENT CAPABILITY (UP TO 2A)
- PROTECTION AGAINST CHIP OVERTEMPERATURE
- LOW NOISE
- HIGH SUPPLY VOLTAGE REJECTION
- SUPPLY VOLTAGE RANGE: 4V TO 20V

The TDA 1904 is a monolithic integrated circuit in POWERDIP package intended for use as low-frequency power amplifier in wide range of applications in portable radio and TV sets.



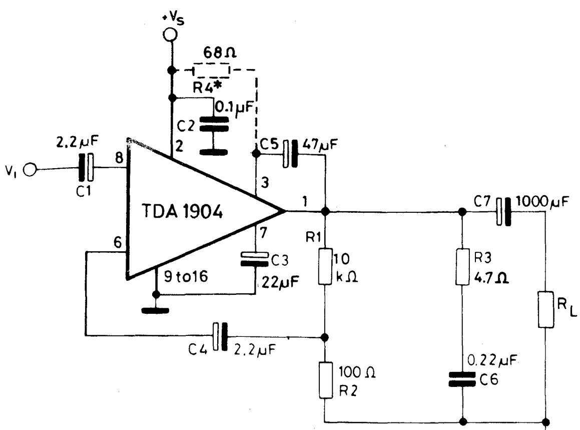
Powerdip
(8 + 8)

ORDERING NUMBER: TDA 1904

ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	20	V
I_O	Peak output current (non repetitive)	2.5	A
I_O	Peak output current (repetitive	2	A
P_{tot}	Total power dissipation at $T_{amb} = 80°C$	1	W
	at $T_{pins} = 60°C$	6	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

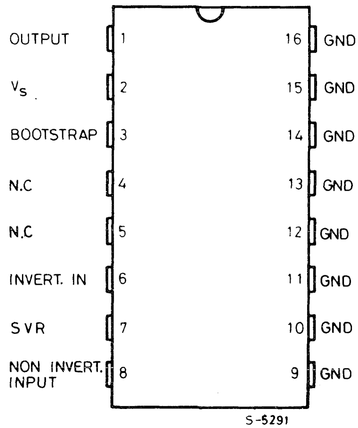
TEST AND APPLICATION CIRCUIT



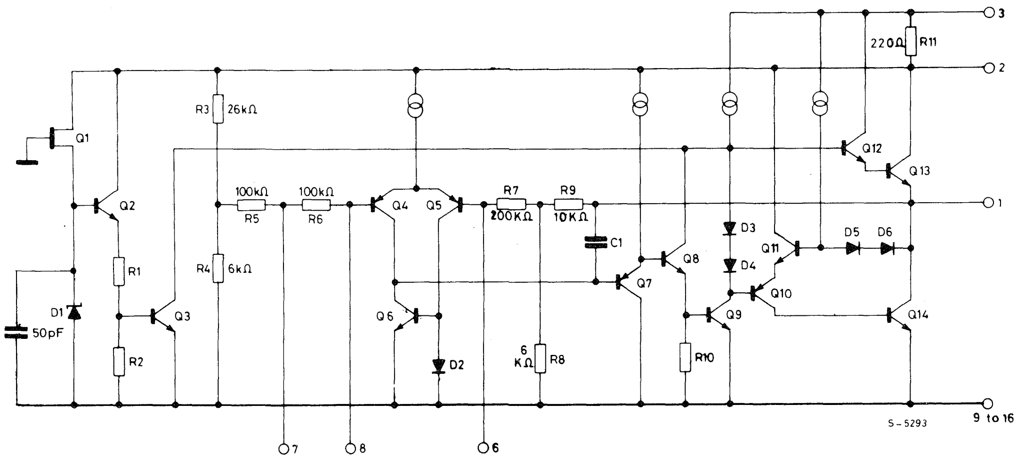
(*) R4 is necessary only for $V_S < 6V$.

S-5292/2

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

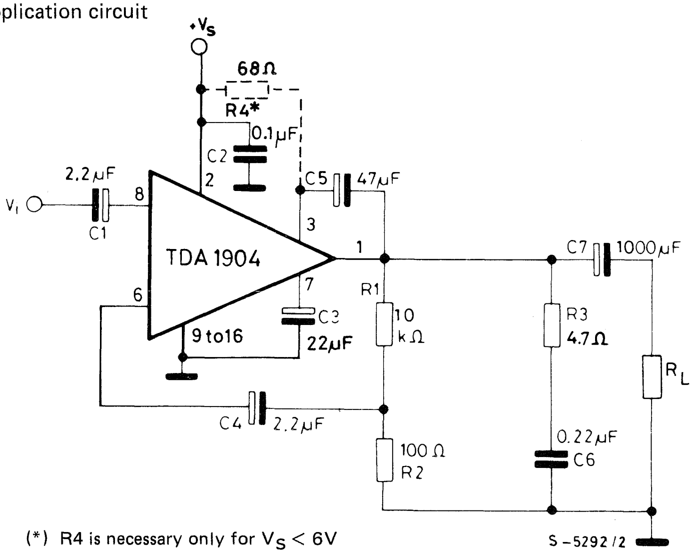
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb} = 25°C, R_{th} (heatsink) = 20°C/W, unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		20	V
V_o	Quiescent output voltage	V_s = 4V V_s = 14V		2.1 7.2		V
I_d	Quiescent drain current	V_s = 9V V_s = 14V		8 10	15 18	mA
P_o	Output power	d = 10% f = 1 KHz V_s = 9V R_L = 4Ω V_s = 14V V_s = 12V V_s = 6V	 1.8 4 3.1 0.7	 2 4.5		W
d	Harmonic distortion	f = 1 KHz V_s = 9V R_L = 4Ω P_o = 50 mW to 1.2W		0.1	0.3	%
V_i	Input saturation voltage (rms)	V_s = 9V V_s = 14V	0.8 1.3			V
R_i	Input resistance (pin 8)	f = 1 KHz	55	150		KΩ
η	Efficiency	f = 1 KHz V_s = 9V R_L = 4Ω P_o = 2W V_s = 14V R_L = 4Ω P_o = 4.5W		 70 65		%
BW	Small signal bandwidth (-3 dB)	V_s = 14V R_L = 4Ω	40 to 40,000			Hz
G_v	Voltage gain (open loop)	V_s = 14V f = 1 KHz		75		dB
G_v	Voltage gain (closed loop)	V_s = 14V R_L = 4Ω f = 1 KHz P_o = 1W	39.5	40	40.5	dB
e_N	Total input noise	R_g = 50Ω R_g = 10 KΩ (°)		1.2 2	 4	µV
		R_g = 50Ω R_g = 10 KΩ (°°)		2 3		µV
SVR	Supply voltage rejection	V_s = 12V f_{ripple} = 100 Hz R_g = 10 KΩ V_{ripple} = 0.5Vrms	40	50		dB
T_{sd}	Thermal shut-down case temperature	P_{tot} = 2W		120		°C

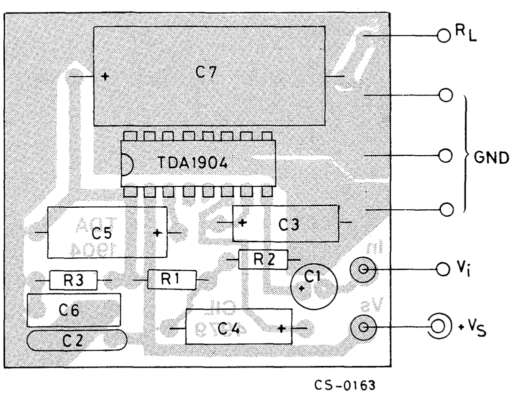
Note: (°) Weighting filter = curve A.
(°°) Filter with noise bendwidth: 22 Hz to 22 KHz.

Fig. 1 – Test and application circuit



(*) R4 is necessary only for $V_S < 6V$

Fig. 2 - P.C. board and components layout of fig. 1 (1 : 1 scale)



APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 1.
When the supply voltage V_S is less than 6V, a 68Ω resistor must be connected between pin 2 and pin 3 in order to obtain the maximum output power.
Different values can be used. The following table can help the designer.

Components	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value	Allowed range	
					Min.	Max.
R1	10 KΩ	Feedback resistors	Increase of gain.	Decrease of gain. Increase quiescent current.	9 R3	
R2	100 Ω	Feedback resistors	Decrease of gain.	Increase of gain.		1 KΩ
R3	4.7 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads.			
R4	68 Ω	Increase of the output swing with low supply voltage.			39 Ω	220 Ω
C1	2.2 μF	Input DC decoupling.	Higher cost lower noise.	Higher low frequency cutoff. Higher noise.		
C2	0.1 μF	Supply voltage bypass.		Danger of oscillations.		
C3	22 μF	Ripple rejection	Increase of SVR increase of the switch-on time.	Degradation of SVR.	2.2 μF	100μF
C4	2.2 μF	Inverting input DC decoupling.	Increase of the switch-on noise	Higher low frequency cutoff.	0.1 μF	
C5	47 μF	Bootstrap.		Increase of the distortion at low frequency.	10 μF	100μF
C6	0.22 μF	Frequency stability.		Danger of oscillation.		
C7	1000 μF	Output DC decoupling.		Higher low frequency cutoff.		

Fig. 3 – Quiescent output voltage vs. supply voltage

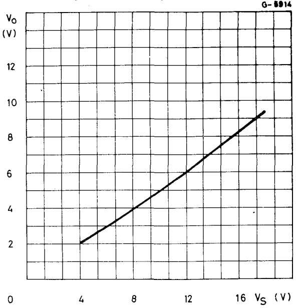


Fig. 4 – Quiescent drain current vs. supply voltage

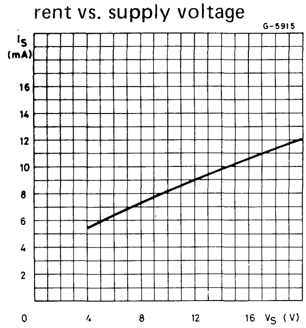


Fig. 5 – Output power vs. supply voltage

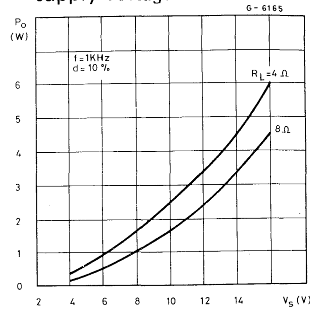


Fig. 6 – Distortion vs. output power

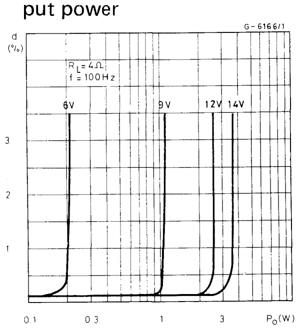


Fig. 7 – Distortion vs. output power

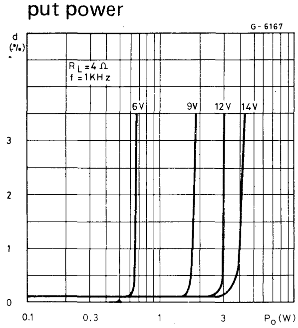


Fig. 8 – Distortion vs. output power

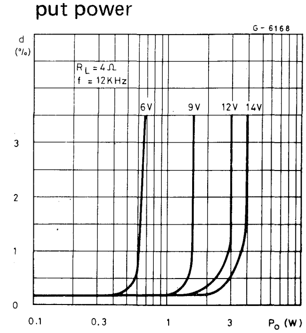


Fig. 9 – Distortion vs. output power

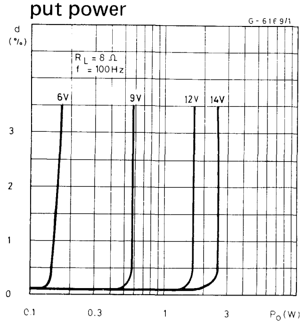


Fig. 10 – Distortion vs. output power

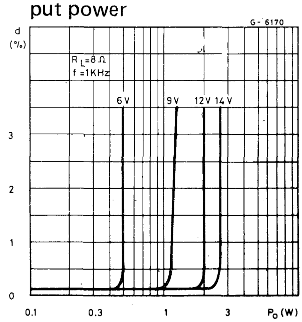


Fig. 11 – Distortion vs. output power

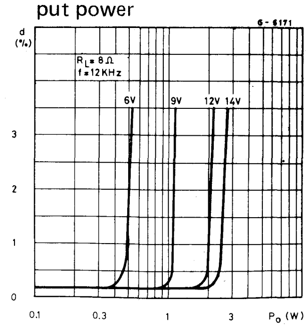


Fig. 12 - Distortion vs. frequency

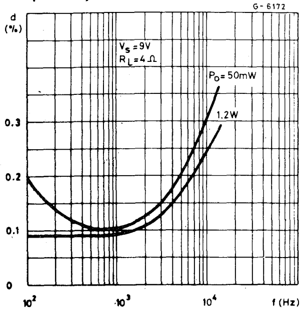


Fig. 13 - Distortion vs. frequency

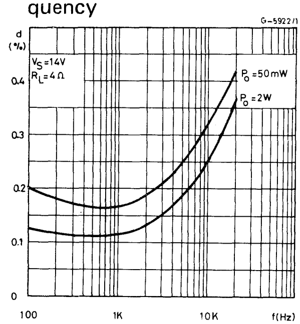


Fig. 14 - Distortion vs. frequency

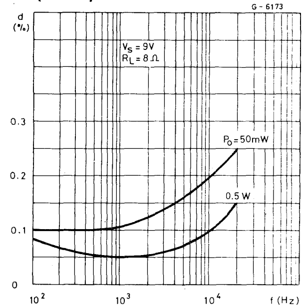


Fig. 15 - Distortion vs. frequency

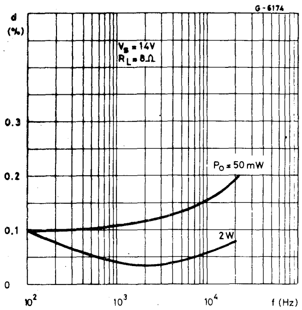


Fig. 16 - Supply voltage rejection vs. frequency

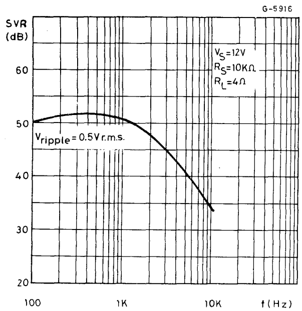


Fig. 17 - Total power dissipation and efficiency vs. output power

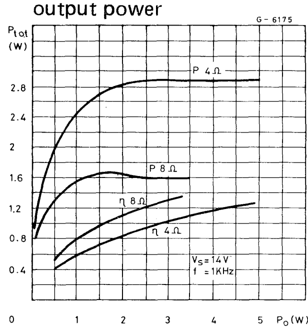


Fig. 18 - Total power dissipation vs. output power

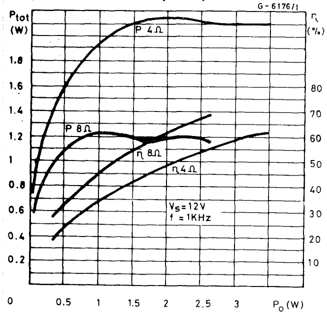


Fig. 19 - Total power dissipation vs. output power

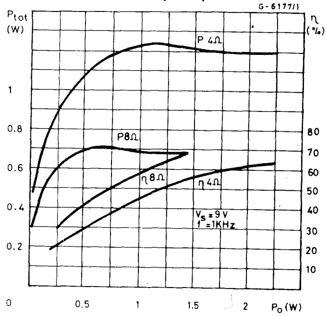
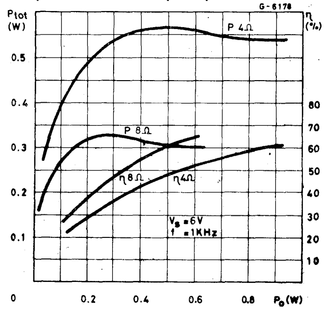


Fig. 20 - Total power dissipation vs. output power



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily tolerated since the T_j cannot be higher than 150°C.

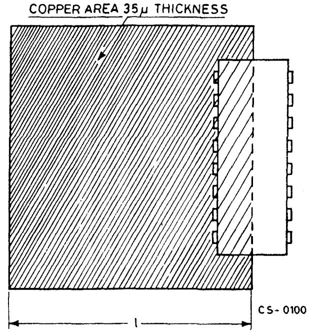
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
If for any reason, the junction temperature increase up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

MOUNTING INSCTRUCTION

The TDA 1904 is assembled in the Powerdip, in which 8 pins (from 9 to 16) are attached to the frame and remove the heat produced by the chip.

Figure 21 shows a PC board copper area used as a heatsink (l = 65 mm).
The thermal resistance junction-ambient is 35°C.

Fig. 21 - Example of heatsink using PC board copper (l = 65 mm)



SGS-THOMSON MICROELECTRONICS

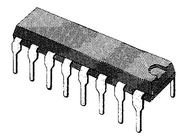
TDA1905

5W AUDIO AMPLIFIER WITH MUTING

The TDA1905 is a monolithic integrated circuit in POWERDIP package, intended for use as low frequency power amplifier in a wide range of applications in radio and TV sets:

- muting facility
- protection against chip over temperature
- very low noise
- high supply voltage rejection
- low "switch-on" noise
- voltage range 4V to 30V

The TDA 1905 is assembled in a new plastic package, the POWERDIP, that offers the same assembly ease, space and cost saving of a normal dual in-line package but with a power dissipation of up to 6W and a thermal resistance of 15°C/W (junction to pins).



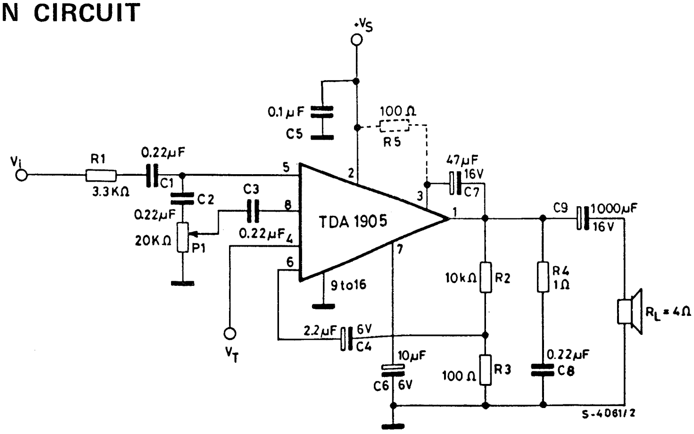
Powerdip
(8 + 8)

ORDERING NUMBER: TDA1905

ABSOLUTE MAXIMUM RATINGS

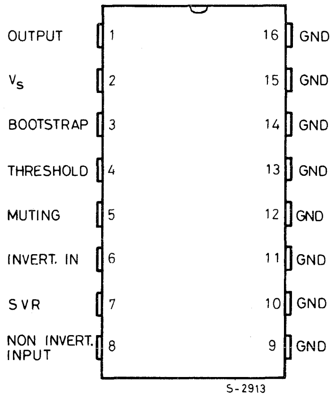
V_s	Supply voltage	30	V
I_o	Output peak current (non repetitive)	3	A
I_o	Output peak current (repetitive)	2.5	A
V_i	Input voltage	0 to $+V_s$	V
V_i	Differential input voltage	±7	V
V_{11}	Muting thresold voltage	V_s	V
P_{tot}	Power dissipation at $T_{amb} = 80°C$	1	W
	$T_{case} = 60°C$	6	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

APPLICATION CIRCUIT

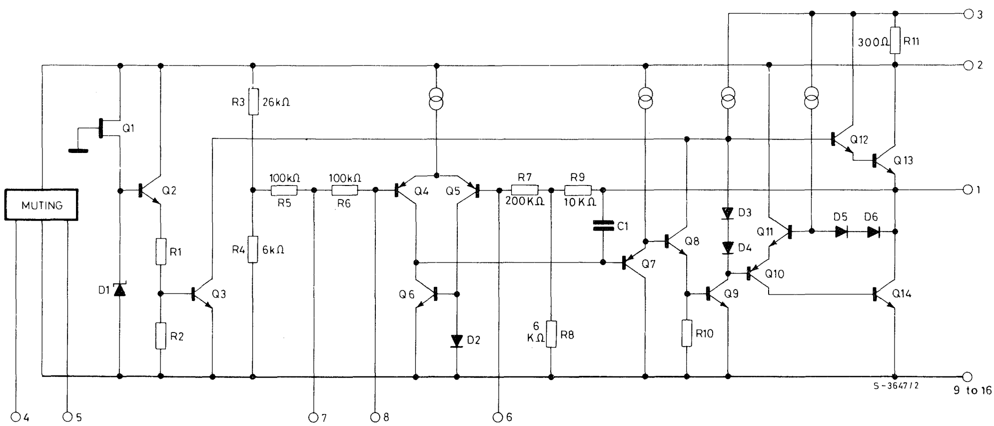


CONNECTION DIAGRAM

(Top view)



SCHEMATIC DIAGRAM

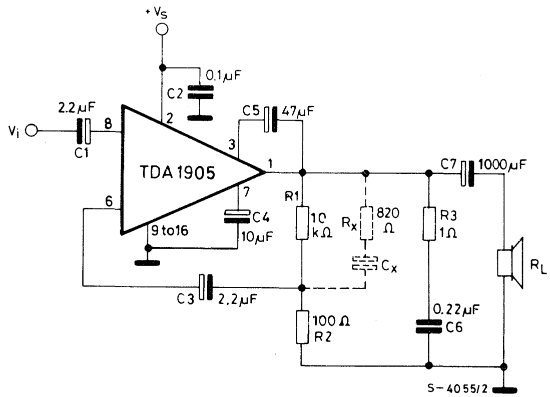


THERMAL DATA

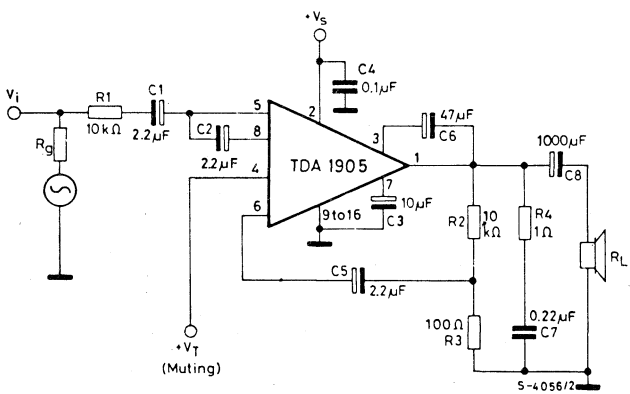
$R_{th\,j\text{-}case}$	Thermal resistance junction-pins	max	15	°C/W
$R_{th\,j\text{-}amb}$	Thermal resistance junction-amb	max	70	°C/W

TEST CIRCUITS:

WITHOUT MUTING



WITH MUTING FUNCTION



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb} = 25°C, R_{th} (heatsink) = 20°C/W, unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		30	V
V_o	Quiescent output voltage	V_s = 4V V_s = 14V V_s = 30V	1.6 6.7 14.4	2.1 7.2 15.5	2.5 7.8 16.8	V
I_d	Quiescent drain current	V_s = 4V V_s = 14V V_s = 30V		15 17 21	 35	mA
$V_{CE\ sat}$	Output stage saturation voltage	I_C = 1A I_C = 2A		0.5 1		V
P_o	Output power	d = 10% f = 1KHz V_s = 9V R_L = 4Ω (*) V_s = 14V R_L = 4Ω V_s = 18V R_L = 8Ω V_s = 24V R_L = 16Ω	 2.2 5 5 4.5	 2.5 5.5 5.5 5.3		W
d	Harmonic distortion	f = 1KHz V_s = 9V R_L = 4Ω P_o = 50 mW to 1.5W V_s = 14V R_L = 4Ω P_o = 50 mW to 3W V_s = 18V R_L = 8Ω P_o = 50 mW to 3W V_s = 24V R_L = 16Ω P_o = 50 mW to 3W		 0.1 0.1 0.1 0.1		%
V_i	Input sensitivity	f = 1KHz V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 8Ω P_o = 5.5W V_s = 24V R_L = 16Ω P_o = 5.3W		 37 49 73 100		mV
V_i	Input saturation voltage (rms)	V_s = 9V V_s = 14V V_s = 18V V_s = 24V	0.8 1.3 1.8 2.4			V
R_i	Input resistance (pin 8)	f = 1KHz	60	100		KΩ
I_d	Drain current	f = 1KHz V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 8Ω P_o = 5.5W V_s = 24V R_L = 16Ω P_o = 5.3W		 380 550 410 295		mA
η	Efficiency	f = 1KHz V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 8Ω P_o = 5.5W V_s = 24V R_L = 16Ω P_o = 5.3W		 73 71 74 75		%

(*) With an external resistor of 100Ω between pin 3 and $+V_s$.

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BW	Small signal bandwidth (-3dB)	V_s = 14V R_L = 4Ω P_o = 1W	40 to 40,000			Hz
G_v	Voltage gain (open loop)	V_s = 14V f = 1KHz		75		dB
G_v	Voltage gain (closed loop)	V_s = 14V R_L = 4Ω f = 1KHz P_o = 1W	39.5	40	40.5	dB
e_N	Total input noise	R_g = 50Ω R_g = 1KΩ (°) R_g = 10KΩ		1.2 1.3 1.5	4.0	μV
		R_g = 50Ω R_g = 1KΩ (°°) R_g = 10KΩ		2.0 2.0 2.2	6.0	μV
S/N	Signal to noise ratio	V_s = 14V P_o = 5.5W R_L = 4Ω; R_g = 10KΩ R_g = 0 (°)		90 92		dB
		R_g = 10KΩ R_g = 0 (°°)		87 87		dB
SVR	Supply voltage rejection	V_s = 18V R_L = 8Ω f_{ripple} = 100 Hz R_g = 10KΩ V_{ripple} = 0.5Vrms	40	50		dB
T_{sd}	Thermal shut-down case temperature (*)	P_{tot} = 2.5W		115		°C

MUTING FUNCTION

V_{TOFF}	Muting-off threshold voltage (pin 4)		1.9		4.7	V
V_{TON}	Muting-on threshold voltage (pin 4)		0		1.3	V
			6.2		V_s	V
R_5	Input resistance (pin 5)	Muting off	80	200		KΩ
		Muting on		10	30	Ω
R_4	Input resistance (pin 4)		150			KΩ
A_T	Muting attenuation	$R_g + R_1$ = 10KΩ	50	60		dB

Note:
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.
(*) See fig. 30 and fig. 31

Fig. 1 - Quiescent output voltage vs. supply voltage

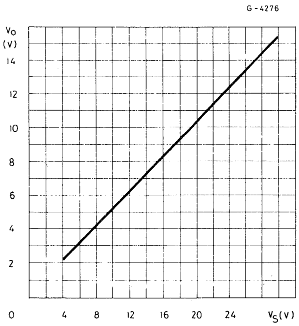


Fig. 2 - Quiescent drain current vs. supply voltage

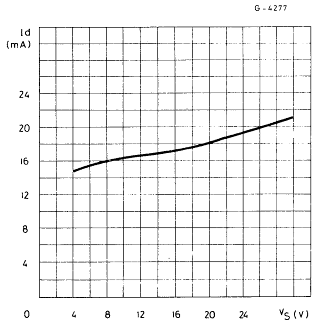


Fig. 3 - Output power vs. supply voltage

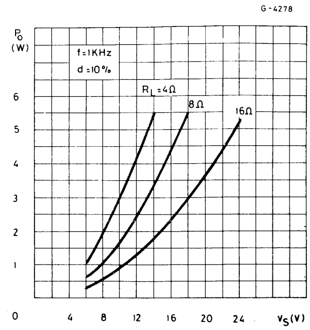


Fig. 4 - Distortion vs. output power (R_L = 16Ω)

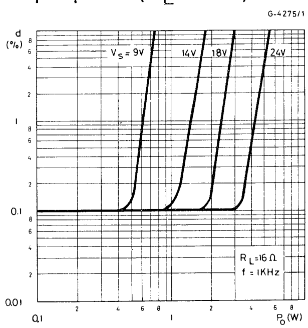


Fig. 5 - Distortion vs. output power (R_L = 8Ω)

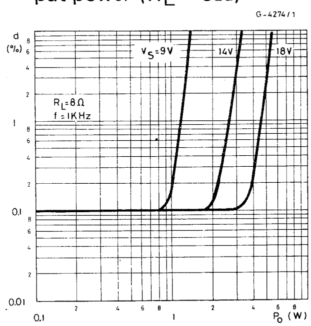


Fig. 6 - Distortion vs. output power (R_L = 4Ω)

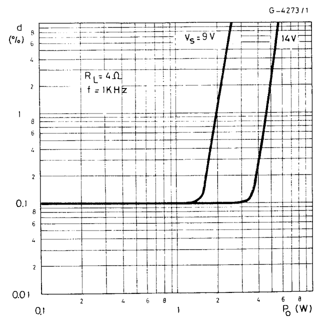


Fig. 7 - Distortion vs. frequency (R_L = 16Ω)

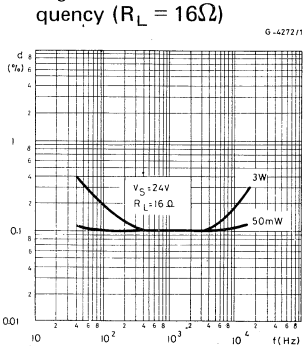


Fig. 8 - Distortion vs. frequency (R_L = 8Ω)

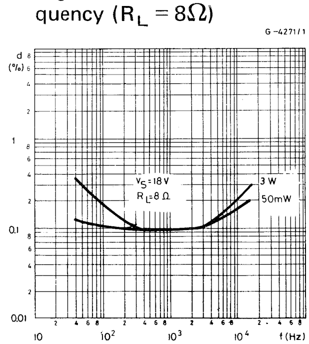


Fig. 9 - Distortion vs. frequency (R_L = 4Ω)

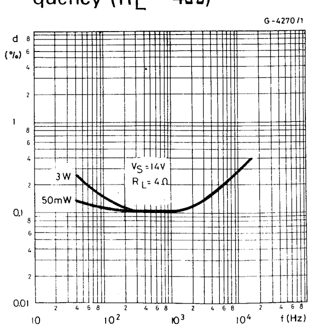


Fig. 10 - Open loop frequency response

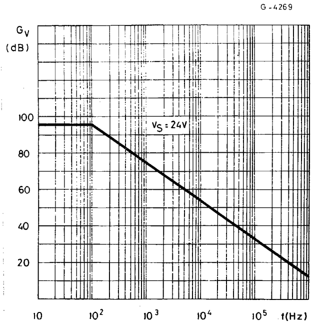


Fig. 11 - Output power vs. input voltage

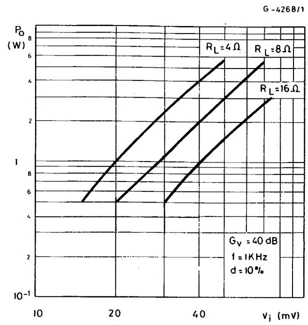


Fig. 12 - Value of capacitor Cx vs. bandwidth (BW) and gain (Gv)

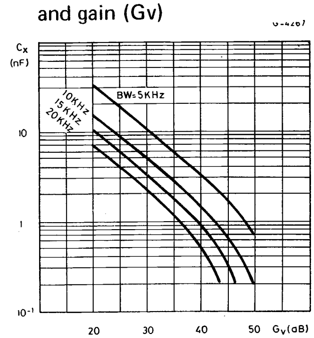


Fig. 13 - Supply voltage rejection vs. voltage gain (ref. to the Muting circuit)

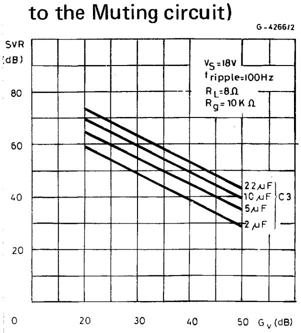


Fig. 14 - Supply voltage rejection vs. source resistance

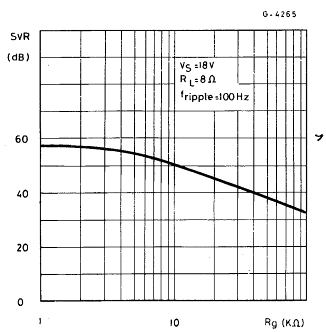


Fig. 15 - Max power dissipation vs. supply voltage (sine wave operation)

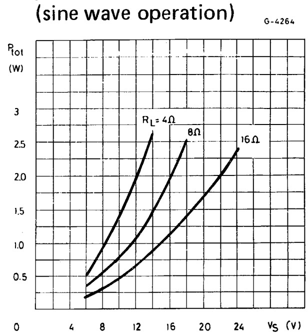


Fig. 16 - Power dissipation and efficiency vs. output power

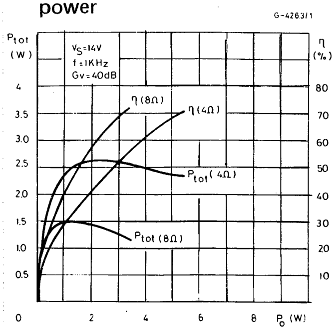


Fig. 17 - Power dissipation and efficiency vs. output power

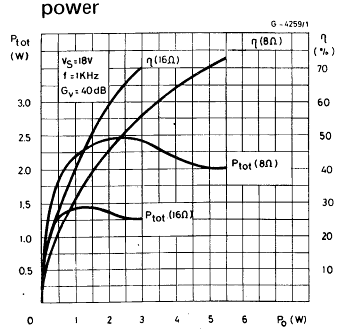
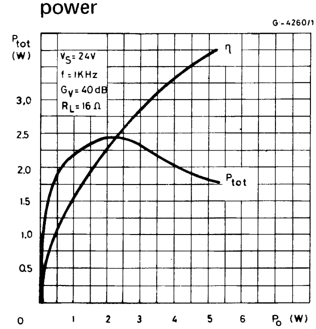
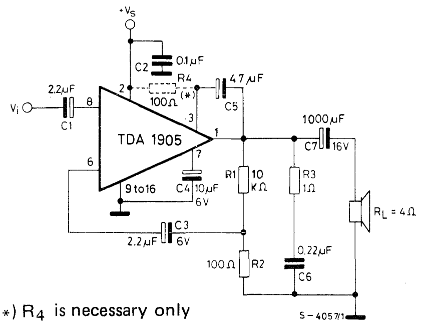


Fig. 18 - Power dissipation and efficiency vs. output power



APPLICATION INFORMATION

Fig. 19 - Application circuit without muting



(*) R_4 is necessary only for $V_s < 10V$.

$P_o = 5.5W$ (d = 10%)
$V_s = 14V$
$I_d = 0.55A$
$G_v = 40$ dB

Fig. 20 - PC board and components lay-out of the circuit of fig. 19 (1:1 scale)

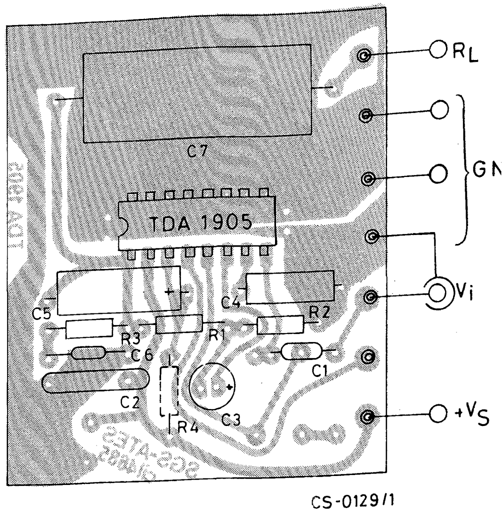


Fig. 21 - Application circuit with muting

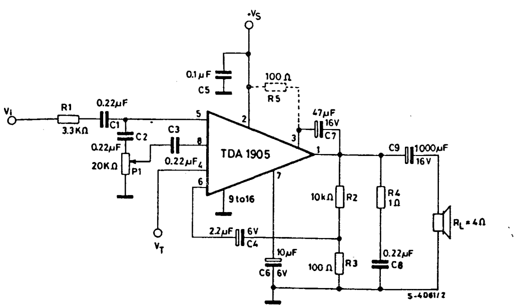
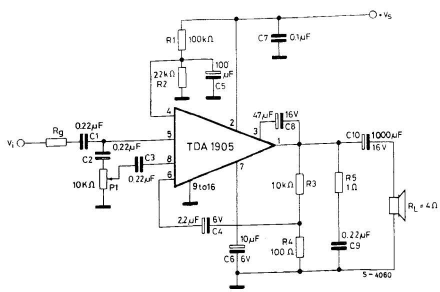


Fig. 22 - Delayed muting circuit



APPLICATION INFORMATION (continued)

Fig. 23 - Low-cost application circuit without bootstrap.

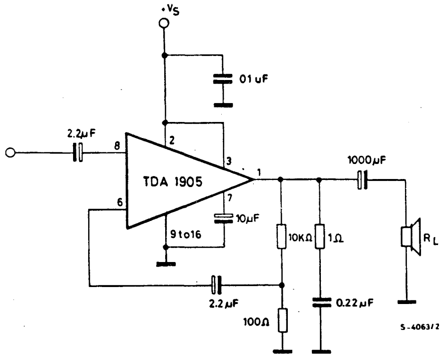


Fig. 24 - Output power vs. supply voltage (circuit of fig. 23)

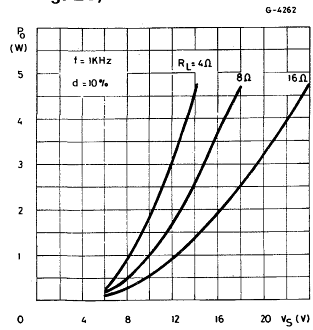


Fig. 25 - Two position DC tone control using change of pin 5 resistance (muting function)

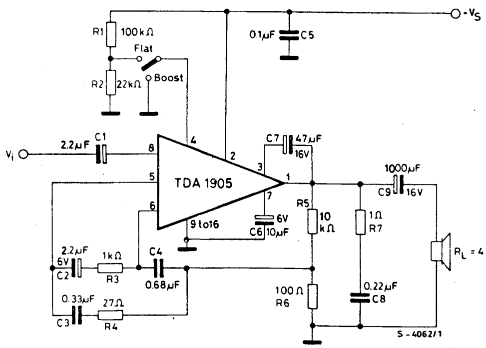


Fig. 26 - Frequency response of the circuit of fig. 25

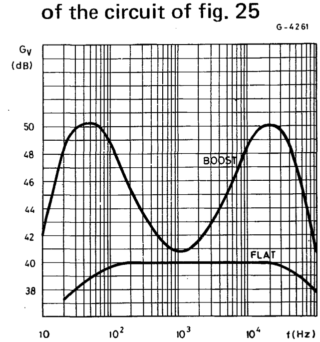


Fig. 27 - Bass Bomb tone control using change of pin 5 resistance (muting function)

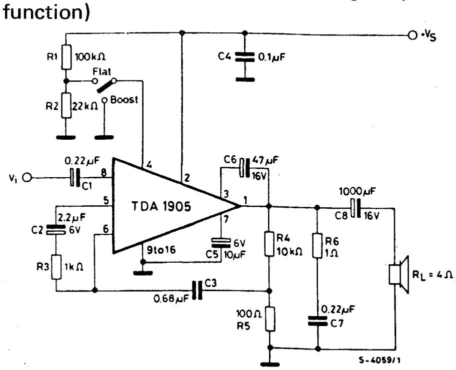
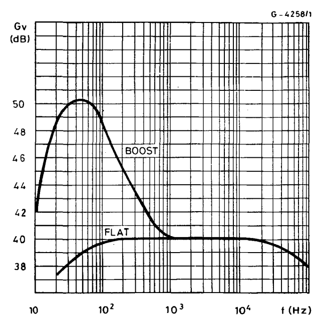


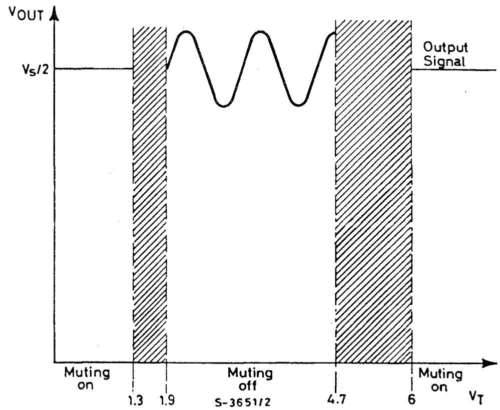
Fig. 28 - Frequency response of the circuit of fig. 27



MUTING FUNCTION

The output signal can be inhibited applying a DC voltage V_T to pin 4, as shown in fig. 29

Fig. 29

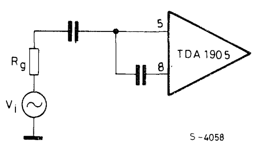


The input resistance at pin 5 depends on the threshold voltage V_T at pin 4 and is typically:

$R_5 = 200\ K\Omega$ @ $1.9V \leqslant V_T \leqslant 4.7V$ muting-off

$R_5 = 10\Omega$ @ $0V \leqslant V_T \leqslant 1.3V$, $6V \leqslant V_T \leqslant V_s$ muting-on

Referring to the following input stage, the possible attenuation of the input signal and therefore of the output signal can be found using the following expression:



$$A_T = \frac{V_i}{V_8} = \frac{R_g + \left(\frac{R_8 \cdot R_5}{R_8 + 5}\right)}{\left(\frac{R_8 \cdot R_5}{R_8 + R_5}\right)}$$

where $R_8 \cong 100\ K\Omega$

Considering $R_g = 10\ K\Omega$ the attenuation in the muting-on condition is typically $A_T = 60$ dB. In the muting-off condition, the attenuation is very low, tipically 1.2 dB.
A very low current is necessary to drive the threshold voltage V_T because the input resistance at pin 4 is greater than 150 KΩ· The muting function can be used in many cases, when a temporary inhibition of the output signal is requested, for example:

- in switch-on condition, to avoid preamplifier power-on transients (see fig. 22)
- during switching at the input stages.
- during the receiver tuning.

The variable impedance capability at pin 5 can be useful in many application and two examples are shown in fig. 25 and 27, where it has been used to change the feedback network, obtaining 2 different frequency response.

APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 21. When the supply voltage V_s is less than 10V, a 100Ω resistor must be connected between pin 2 and pin 3 in order to obtain the maximum output power.
Different values can be used. The following table can help the designer.

Component	Raccom. value	Purpose	Larger than recommended value	Smaller than recommended value	Allowed range Min.	Max.
$R_g + R_1$	10KΩ	Input signal imped. for muting operation	Increase of the attenuation in muting-on condition. Decrease of the input sensitivity.	Decrease of the attenuation in muting on condition.		
R_2	10KΩ	Feedback resistors	Increase of gain.	Decrease of gain. Increase quiescent current.	9 R_3	
R_3	100Ω	Feedback resistors	Decrease of gain.	Increase of gain.		1KΩ
R_4	1Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads.			
R_5	100Ω	Increase of the output swing with low supply voltage.			47	330
P_1	20KΩ	Volume potentiometer	Increase of the switch-on noise.	Decrease of the input impedance and of the input level.	10KΩ	100KΩ
C_1 C_2 C_3	0.22 μF	Input DC decoupling.	Higher cost lower noise.	Higher low frequency cutoff. Higher noise		
C_4	2.2μF	Inverting input DC decoupling.	Increase of the switch-on noise.	Higher low frequency cutoff.	0.1μF	
C_5	0.1μF	Supply voltage bypass.		Danger of oscillations.		
C_6	10 μF	Ripple rejection	Increase of SVR increase of the switch-on time	Degradation of SVR	2.2 μF	100 μF
C_7	47μF	Bootstrap.		Increase of the distortion at low frequency.	10μF	100μF
C_8	0.22μF	Frequency stability.		Danger of oscillation.		
C_9	1000 μF	Output DC decoupling.		Higher low frequency cutoff.		

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily tolerated since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
   If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 32 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 30 - Output power and drain current vs. case temperature.

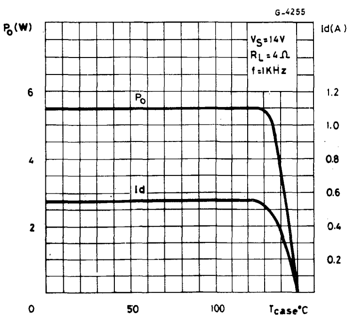


Fig. 31 - Output power and drain current vs. case temperature

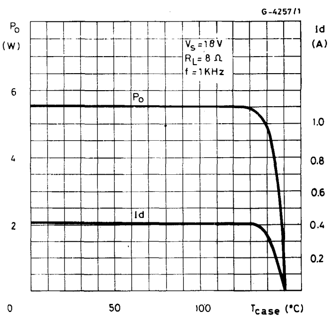
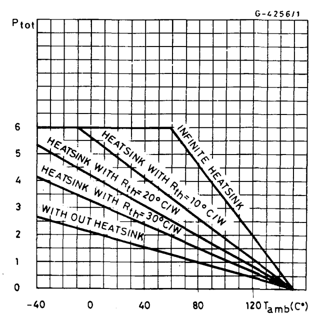


Fig. 32 - Maximum allowable power dissipation vs. ambient temperature.

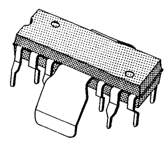


MOUNTING INSTRUCTION: See TDA1904

8W AUDIO AMPLIFIER

The TDA1908 is a monolithic integrated circuit in 12 lead quad in-line plastic package intended for low frequency power applications. The mounting is compatible with the old types TBA800, TBA810S, TCA830S and TCA940N. Its main features are:

- flexibility in use with a max output curent of 3A and an operating supply voltage range of 4V to 30V;
- protection against chip overtemperature;
- soft limiting in saturation conditions;
- low "switch-on" noise;
- low number of external components;
- high supply voltage rejection;
- very low noise.



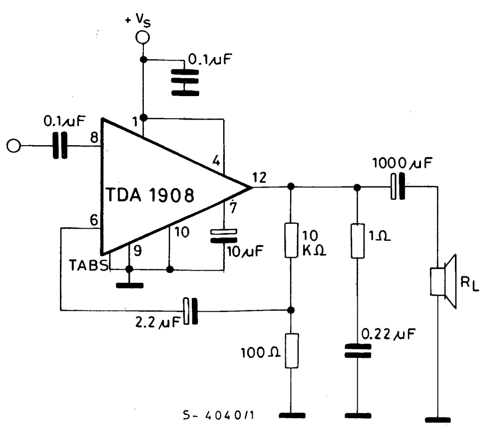
Findip

ORDER CODE: TDA1908

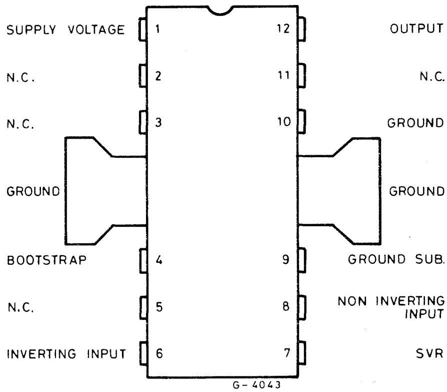
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	30	V
I_o	Output peak current (non repetitive)	3.5	A
I_o	Output peak current (repetitive)	3	A
P_{tot}	Power dissipation: at $T_{amb} = 80°C$	1	W
	at $T_{amb} = 90°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

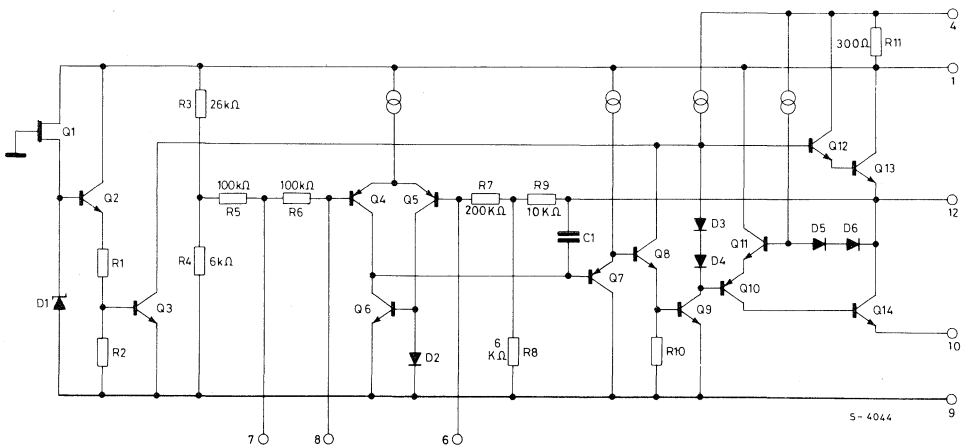
APPLICATION CIRCUIT



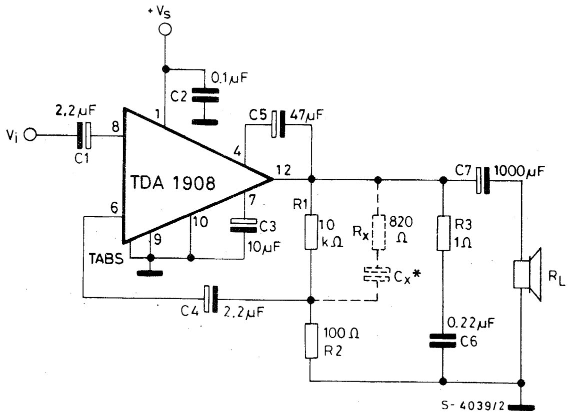
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



TEST CIRCUIT



* See fig. 12.

THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	(°) 70	°C/W

(°) Obtained with tabs soldered to printed circuit board with min copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb} = 25°C, R_{th} (heatsink)= 8 °C/W, unless otherwise specified)

	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		30	V
V_o	Quiescent output voltage	V_s = 4V V_s = 18V V_s = 30V	1.6 8.2 14.4	2.1 9.2 15.5	2.5 10.2 16.8	V
I_d	Quiescent drain current	V_s = 4V V_s = 18V V_s = 30V		15 17.5 21	 35	mA
V_{CEsat}	Output stage saturation voltage (each output transistor)	I_C= 1A I_C= 2.5A		0.5 1.3		V
P_o	Output power	d = 10% f = 1 KHz V_s = 9V R_L= 4Ω V_s = 14V R_L= 4Ω V_s = 18V R_L= 4Ω V_s = 22V R_L= 8Ω V_s = 24V R_L= 16Ω	 7 6.5 4.5	 2.5 5.5 9 8 5.3		W

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test condition	Min.	Typ.	Max	Unit
d	Harmonic distortion	f = 1KHz V_s = 9V R_L = 4Ω P_o = 50 mW to 1.5W V_s = 18V R_L = 4Ω P_o = 50 mW to 4W V_s = 24V R_L = 16Ω P_o = 50 mW to 3W		0.1 0.1 0.1		%
V_i	Input sensitivity	V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 4Ω P_o = 9W V_s = 22V R_L = 8Ω P_o = 8W V_s = 24V R_L = 16Ω P_o = 5.3W		37 52 64 90 110		mV
V_i	Input saturation voltage (rms)	V_s = 9V V_s = 14V V_s = 18V V_s = 24V	0.8 1.3 1.8 2.4			V
R_i	Input resistance (pin 8)	f = 1 KHz	60	100		KΩ
I_s	Drain current	f = 1 KHz V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 4Ω P_o = 9W V_s = 22V R_L = 8Ω P_o = 8W V_s = 24V R_L = 16Ω P_o = 5.3W		570 730 500 310		mA
η	Efficiency	V_s = 18V f = 1 KHz R_L = 4Ω P_o = 9W		72		%
BW	Small signal bandwidth (-3 dB)	V_s = 18V R_L = 4Ω P_o = 1W		40 to 40 000		Hz
G_v	Voltage gain (open loop)	f = 1 KHz		75		dB
G_v	Voltage gain (closed loop)	V_s = 18V R_L = 4Ω f = 1 KHz P_o = 1W	39.5	40	40.5	dB
e_N	Total input noise	(°) R_g = 50Ω R_g = 1KΩ R_g = 10 KΩ		1.2 1.3 1.5	4.0	μV
		(°°) R_g = 50Ω R_g = 1KΩ R_g = 10KΩ		2.0 2.0 2.2	6.0	μV
S/N	Signal to noise ratio	V_s = 18V P_o = 9W R_L = 4Ω — R_g = 10KΩ, R_g = 0 (°)		92 94		dB
		R_g = 10KΩ, R_g = 0 (°°)		88 90		dB
SVR	Supply voltage rejection	V_s = 18V R_L = 4Ω f_{ripple} = 100 Hz R_g = 10KΩ	40	50		dB
T_{sd}	Thermal shut-down junction temperature (*)			145		°C

Note:
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.

Fig. 1 - Quiescent output voltage vs. supply voltage

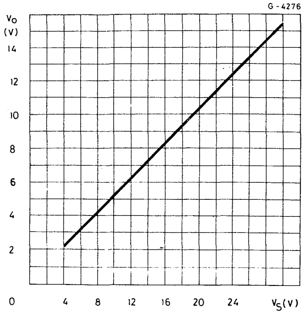


Fig. 2 - Quiescent drain current vs. supply voltage

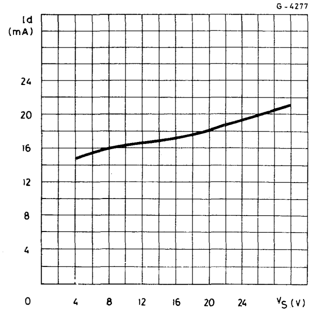


Fig. 3 - Output power vs. supply voltage

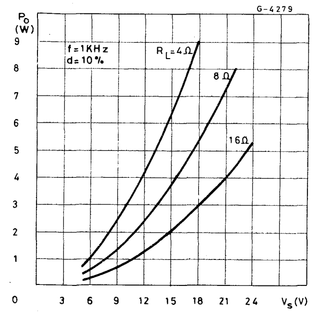


Fig. 4 - Distortion vs. output power (R_L = 16Ω)

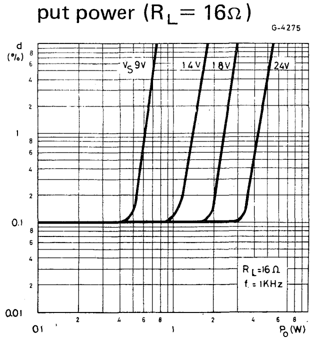


Fig. 5 - Distortion vs. output power (R_L = 8Ω)

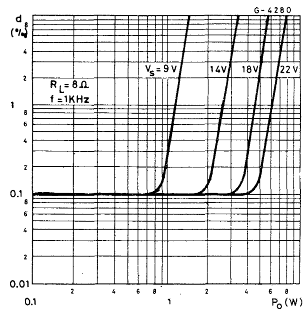


Fig. 6 - Distortion vs. output power (R_L = 4Ω)

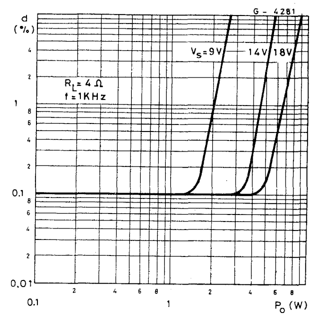


Fig. 7 - Distortion vs. frequency (R_L = 16Ω)

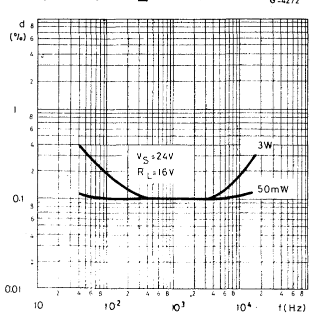


Fig. 8 - Distortion vs. frequency (R_L = 8Ω)

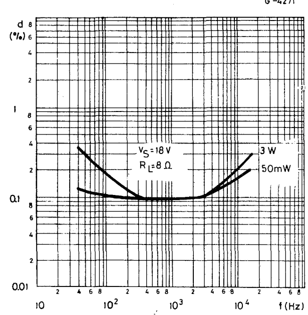


Fig. 9 - Distortion vs. frequency (R_L = 4Ω)

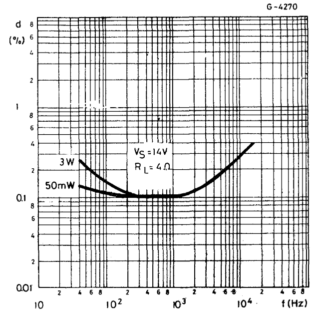


Fig. 10 - Open loop frequency response

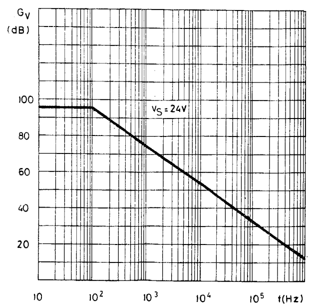


Fig. 11 - Output power vs. input voltage

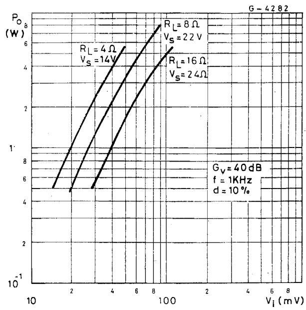


Fig. 12 - Values of capacitor C_X versus gain and B_W

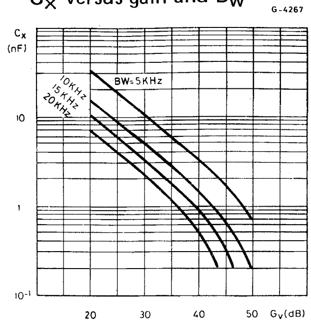


Fig. 13 - Supply voltage rejection vs. voltage gain

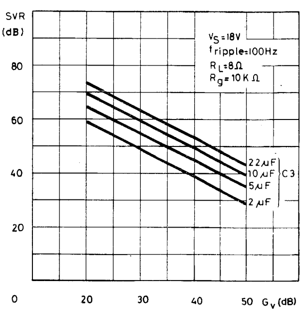


Fig. 14 - Supply voltage rejection vs. source resistance

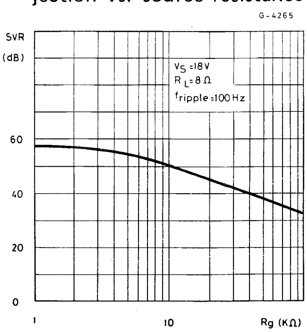


Fig. 15 - Max power dissipation vs. supply voltage

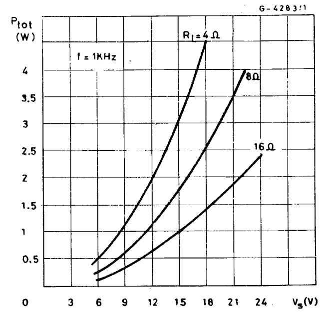


Fig. 16 - Power dissipation and efficiency vs. output power (V_s = 14V)

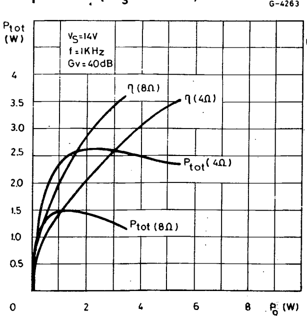


Fig. 17 - Power dissipation and efficiency vs. output power (V_s = 18V)

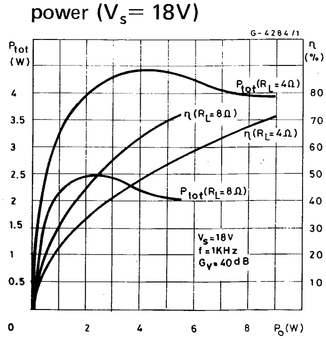
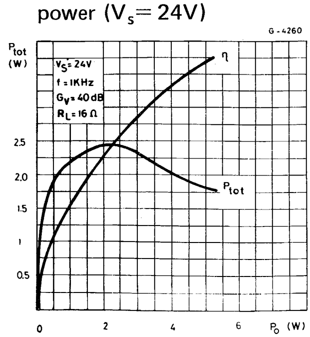
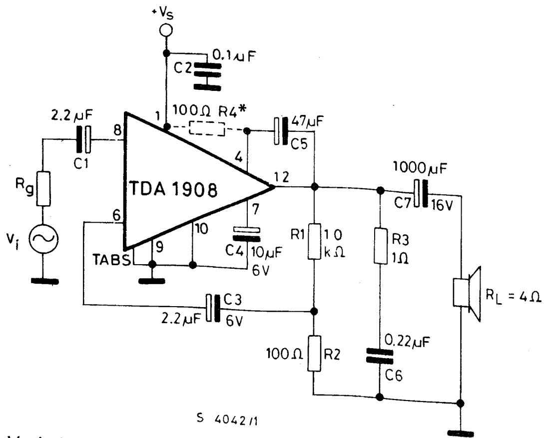


Fig. 18 - Power dissipation and efficiency vs. output power (V_s = 24V)



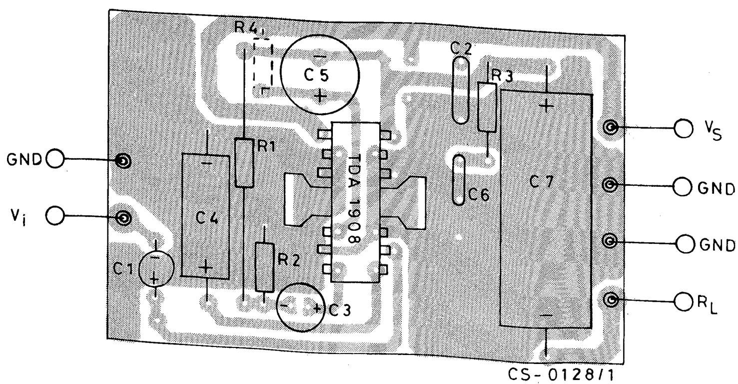
APPLICATION INFORMATION

Fig. 19 - Application circuit with bootstrap



* R4 is necessary when V_s is less than 10V.

Fig. 20 - P.C. board and component lay-out of the circuit of fig. 19 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 21 - Application circuit without bootstrap

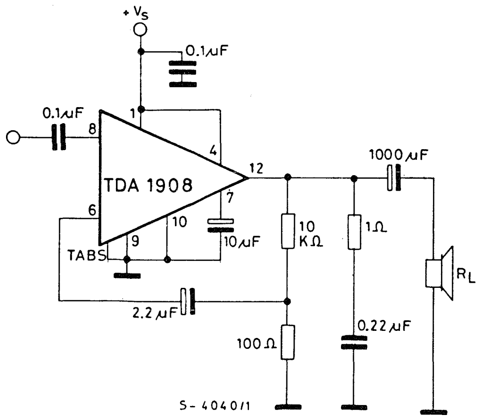


Fig. 22 - Output power vs. supply voltage (circuit of fig. 21)

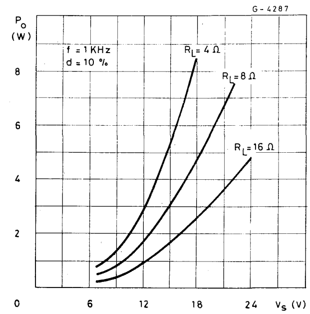
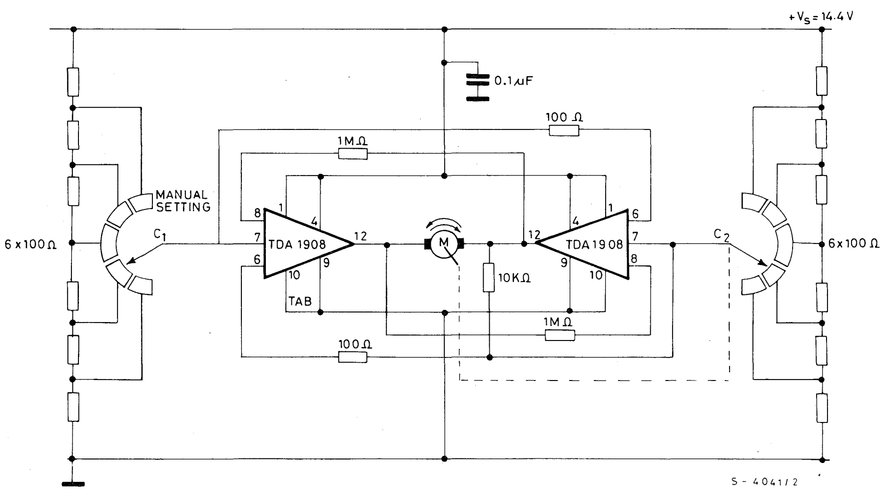


Fig. 23 - Position control for car headlights



APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 19.
When the supply voltage V_s is less than 10V, a 100Ω resistor must be connected between pin 1 and pin 4 in order to obtain the maximum output power.
Different values can be used. The following table can help the designer.

Component	Raccom. value	Purpose	Larger than raccomanded value	Smaller than raccomanded value	Allowed range	
					Min.	Max.
R_1	10 KΩ	Close loop gain setting.	Increase of gain.	Decrease of gain. Increase quiescent current.	9 R_2	
R_2	100 Ω	Close loop gain setting.	Decrease of gain.	Increase of gain.		$R_1/9$
R_3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads.			
R_4	100 Ω	Increasing of output swing with low V_s.			47Ω	330Ω
C_1	2.2 μF	Input DC decoupling.	Lower noise	Higher low frequency cutoff. Higher noise.	0.1 μF	
C_2	0.1 μF	Supply voltage bypass.		Danger of oscillations.		
C_3	2.2 μF	Inverting input DC decoupling.	Increase of the switch-on noise	Higher low frequency cutoff.	0.1 μF	
C_4	10 μF	Ripple Rejection.	Increase of SVR. Increase of the switch-on time.	Degradation of SVR.	2.2 μF	100 μF
C_5	47 μF	Bootstrap		Increase of the distortion at low frequency	10 μF	100 μF
C_6	0.22 μF	Frequency stability.		Danger of oscillation.		
C_7	1000 μF	Output DC decoupling.		Higher low frequency cutoff.		

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If, for any reason, the junction temperature increase up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 26 shows the dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 24 - Output power and drain current vs. case temperature

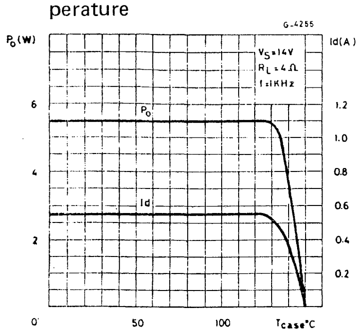


Fig. 25 - Output power and drain current vs. case temperature

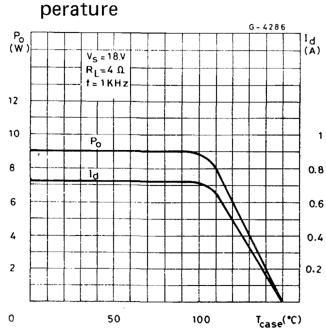
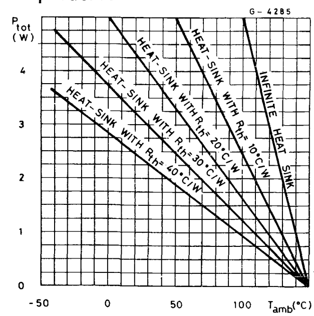


Fig. 26 - Maximum power dissipation vs. ambient temperature



MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by soldering the tabs to a copper area on the PC board (see Fig. 27).

During soldering, tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

Fig. 27 - Mounding example

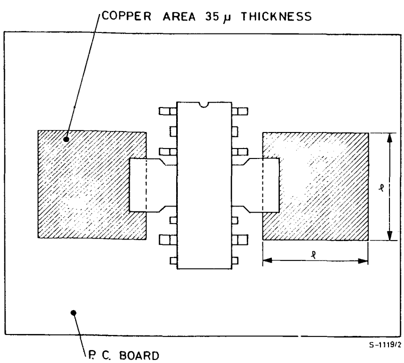
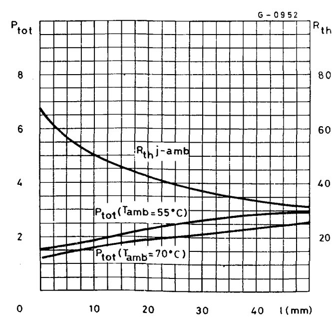


Fig. 28 - Maximum power dissipation and thermal resistance vs. side "ℓ"

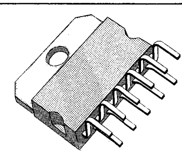


10W AUDIO AMPLIFIER WITH MUTING

The TDA 1910 is a monolithic integrated circuit in MULTIWATT® package, intended for use in Hi-Fi audio power applications, **as high quality TV sets.**

The TDA 1910 meets the DIN 45500 (d = 0.5%) guaranteed output power of 10W when used at 24V/4Ω. At 24V/8Ω the output power is 7W min. Features:
- muting facility
- protection against chip over temperature
- very low noise
- high supply voltage rejection
- low "switch-on" noise.

The TDA 1910 is assembled in MULTIWATT® package that offers:
- easy assembly
- simple heatsink
- space and cost saving
- high reliability.



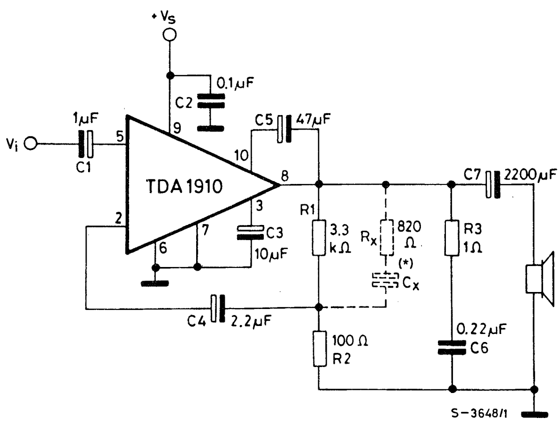
Multiwatt 11

ORDERING NUMBER: TDA 1910

ABSOLUTE MAXIMUM RATINGS

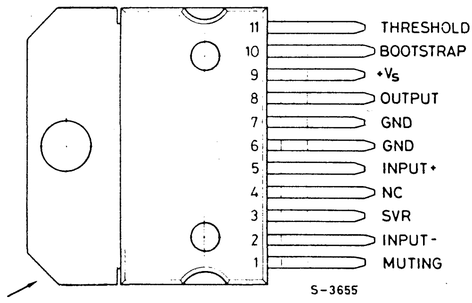
V_s	Supply voltage	30	V
I_o	Output peak current (non repetitive)	3.5	A
I_o	Output peak current (repetitive)	3.0	A
V_i	Input voltage	0 to + V_s	V
V_i	Differential input voltage	± 7	V
V_{11}	Muting thresold voltage	V_s	V
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST CIRCUIT



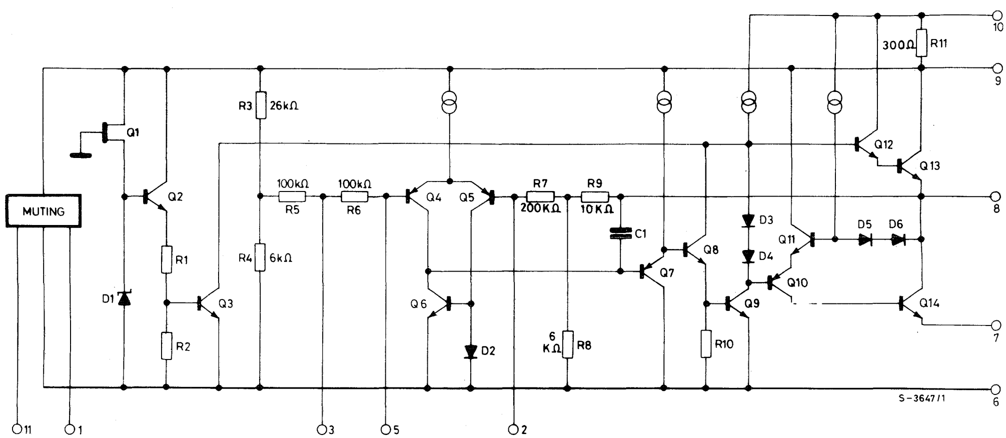
(*) See fig. 13.

CONNECTION DIAGRAM (Top view)

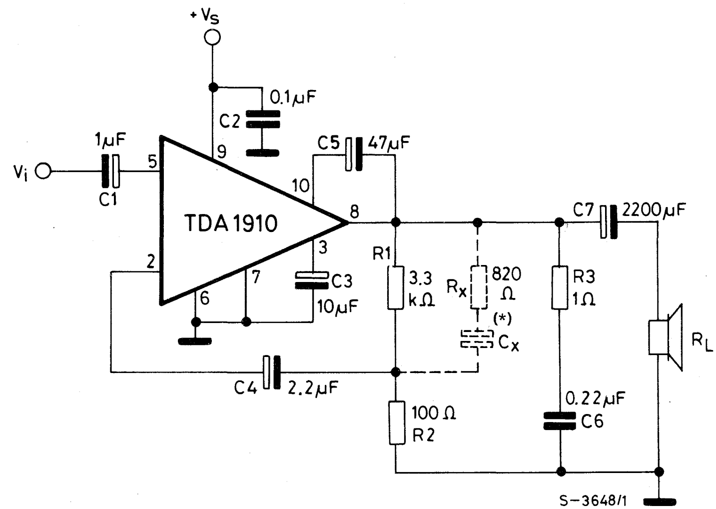


tab connected to pin 6

SCHEMATIC DIAGRAM

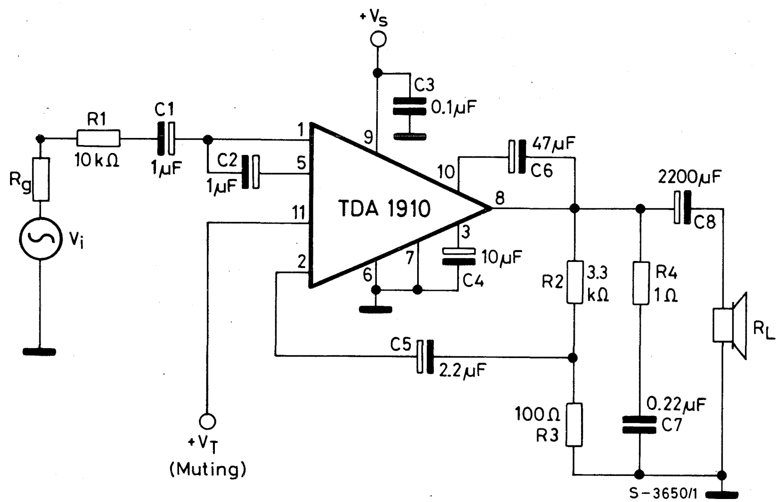


TEST CIRCUIT



(∗) See fig. 13.

MUTING CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}c}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb} = 25°C, R_{th} (heatsink) = 4°C/W, unless otherwise specified)

Parameter		Test condition	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		30	V
V_o	Quiescent output voltage	V_s = 18V V_s = 24V	8.3 11.5	9.2 12.4	10 13.4	V
I_d	Quiescent drain current	V_s = 18V V_s = 24V		19 21	32 35	mA
$V_{CE\ sat}$	Output stage saturation voltage	I_C= 2A		1		V
		I_C= 3A		1.6		V
P_o	Output power	d = 0.5% f = 40 to 15,000Hz V_s = 18V R_L= 4Ω V_s = 24V R_L= 4Ω V_s = 24V R_L= 8Ω	 6.5 10 7	 7 12 7.5		W
		d = 10% f = 1 KHz V_s = 18V R_L= 4Ω V_s = 24V R_L= 4Ω V_s = 24V R_L= 8Ω	 8.5 15 9	 9.5 17 10		W
d	Harmonic distortion	f = 40 to 15,000 Hz V_s = 18V R_L= 4Ω P_o= 50 mW to 6.5W V_s= 24V R_L= 4Ω P_o= 50 mW to 10W V_s = 24V R_L= 8Ω P_o= 50 mW to 7W		 0.2 0.2 0.2	 0.5 0.5 0.5	%
d	Intermodulation distortion	V_s = 24V R_L= 4Ω P_o= 10W f_1= 250 Hz f_2= 8 KHz (DIN 45500)		0.2		%
V_i	Input sensitivity	f = 1 KHz V_s = 18V R_L= 4Ω P_o= 7W V_s = 24V R_L= 4Ω P_o= 12W V_s = 24V R_L= 8Ω P_o= 7.5W		 170 220 245		mV
V_i	Input saturation voltage (rms)	V_s = 18V V_s = 24V	1.8 2.4			V
R_i	Input resistance (pin 5)	f = 1 KHz	60	100		KΩ
I_d	Drain current	V_s = 24V f = 1 KHz R_L= 4Ω P_o= 12W R_L= 8Ω P_o= 7.5W		 820 475		mA

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test condition	Min.	Typ.	Max.	Unit
η	Efficiency	V_s = 24V f = 1 KHz R_L = 4Ω P_o = 12W R_L = 8Ω P_o = 7.5W		 62 65		%
BW	Small signal bandwidth	V_s = 24V R_L = 4Ω P_o = 1W	10 to 120,000			Hz
BW	Power bandwidth	V_s = 24V R_L = 4Ω P_o = 12W d ≤ 0.5%	40 to 15,000			Hz
G_v	Voltage gain (open loop)	f = 1 KHz		75		dB
G_v	Voltage gain (closed loop)	V_s = 24V R_L = 4Ω f = 1 KHz P_o = 1W	29.5	30	30.5	dB
e_N	Total input noise	R_g = 50Ω R_g = 1KΩ (°) R_g = 10KΩ		1.2 1.3 1.5	3.0 3.2 4.0	μV
		R_g = 50Ω R_g = 1KΩ (°°) R_g = 10KΩ		2.0 2.0 2.2	5.0 5.2 6.0	μV
S/N	Signal to noise ratio	V_s = 24V P_o = 12W R_L = 4Ω — R_g = 10KΩ, R_g = 0 (°)	97	103 105		dB
		V_s = 24V P_o = 12W R_L = 4Ω — R_g = 10KΩ, R_g = 0 (°°)	93	100 100		dB
SVR	Supply voltage rejection	V_s = 24V R_L = 4Ω f_{ripple} = 100 Hz R_g = 10KΩ	50	60		dB
T_{sd}	Thermal shut-down case temperature (*)	P_{tot} = 8W	110	125		°C

MUTING FUNCTION (Refer to Muting circuit)

	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_T	Muting-off threshold voltage (pin 11)		1.9		4.7	V
V_T	Muting-on threshold voltage (pin 11)		0		1.3	V
			6		V_s	V
R_1	Input resistance (pin 1)	Muting off	80	200		KΩ
		Muting on		10	30	Ω
R_{11}	Input resistance (pin 11)		150			KΩ
A_T	Muting attenuation	$R_g + R_1$ = 10 KΩ	50	60		dB

Note:
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.
(*) See fig. 29 and fig. 30.

Fig. 1 - Quiescent output voltage vs. supply voltage

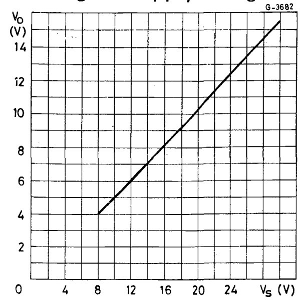


Fig. 2 - Quiescent drain current vs. supply voltage

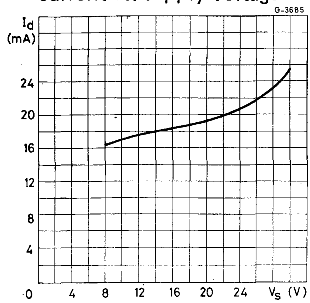


Fig. 3 - Open loop frequency response

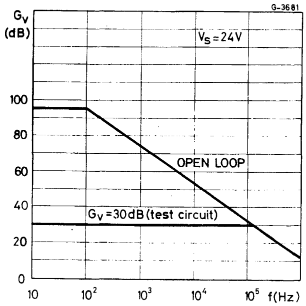


Fig. 4 - Output power vs. supply voltage

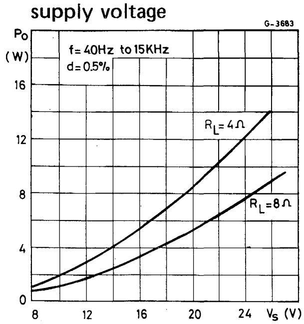


Fig. 5 - Output power vs. supply voltage

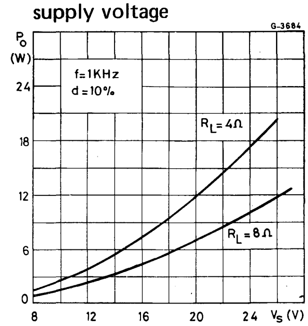


Fig. 6 - Distortion vs. output power

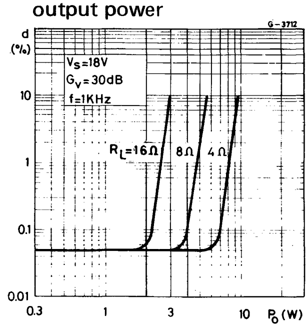


Fig. 7 - Distortion vs. output power

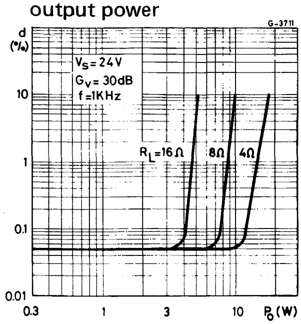


Fig. 8 - Output power vs. frequency

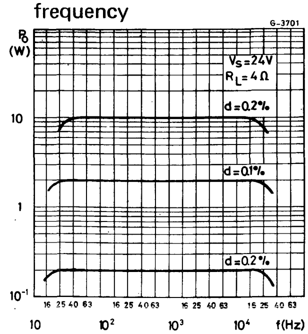


Fig. 9 - Output power vs. frequency

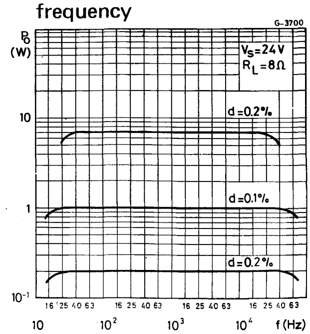


Fig. 10 - Output power vs. input voltage

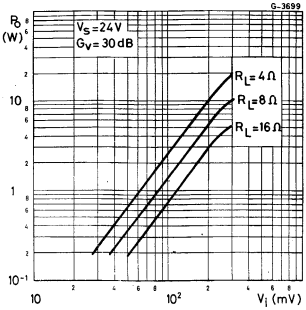


Fig. 11 - Output power vs. input voltage

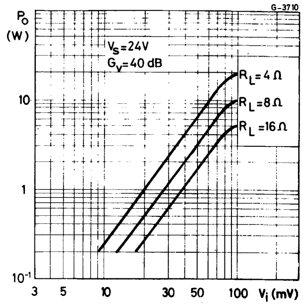


Fig. 12 - Total input noise vs. source resistance

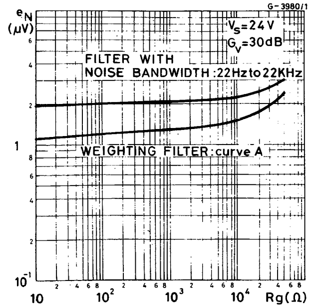


Fig. 13 - Values of capacitor C_X vs. bandwidth (BW) and gain (G_v)

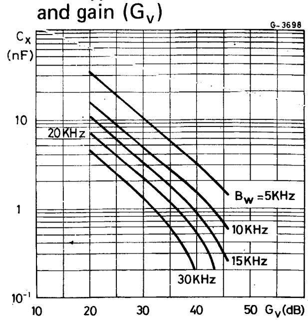


Fig. 14 - Supply voltage rejection vs. voltage gain

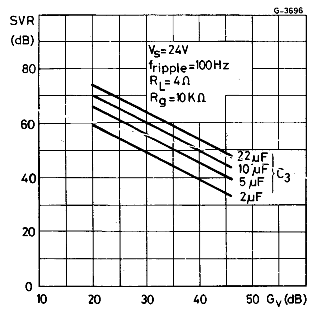


Fig. 15 - Supply voltage rejection vs. source resitance

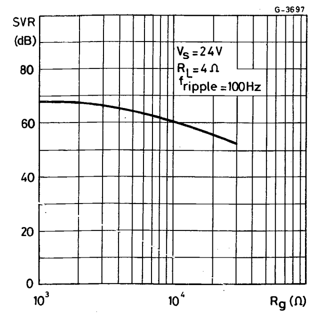


Fig. 16 - Power dissipation and efficiency vs. output power

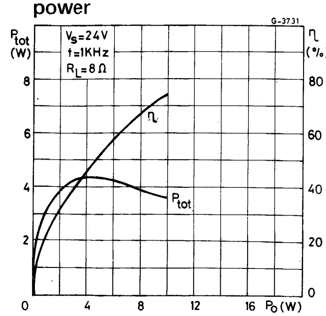


Fig. 17 - Power dissipation and efficiency vs. output power

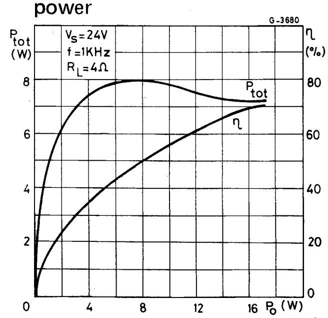
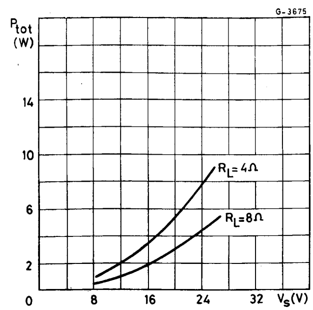


Fig. 18 - Max power dissipation vs. supply voltage



APPLICATION INFORMATION

Fig. 19 - Application circuit without muting

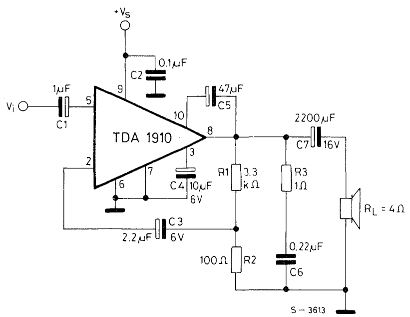


Fig. 20 - PC board and component lay-out of the circuit of fig. 19 (1:1 scale)

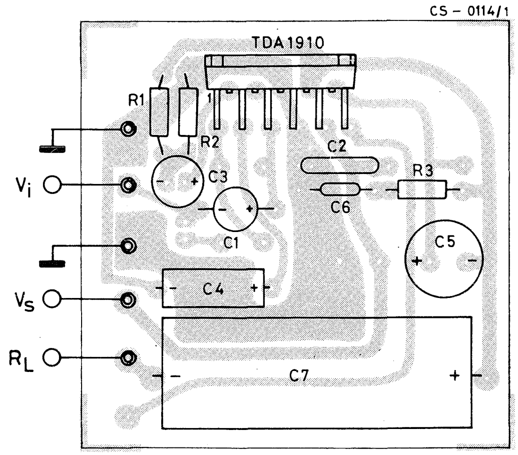
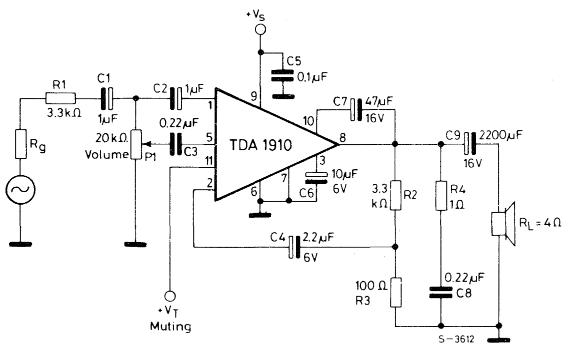


Fig. 21 - Application circuit with muting



Performance (circuits of fig. 19 and 21)

P_o = 12W (40 to 15000 Hz, d $\leq$0.5%)

V_s = 24V

I_d = 0.82A

G_v = 30 dB

APPLICATION INFORMATION (continued)

Fig. 22 - Two position DC tone control (10 dB boost 50 Hz and 20 KHz) using change of pin 1 resistance (muting function)

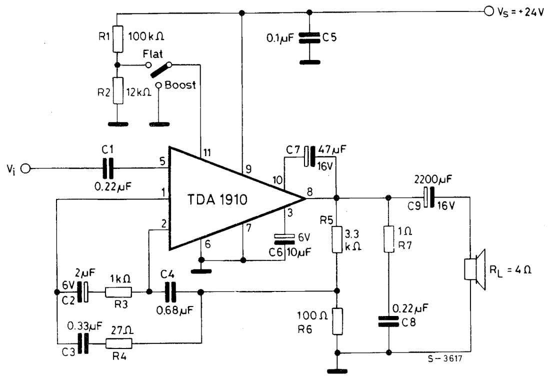


Fig. 23 - Frequency response of the circuit of fig. 22

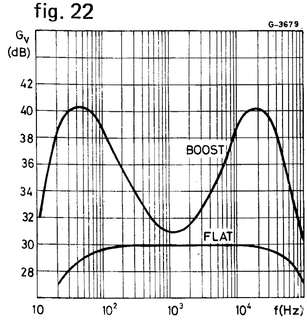


Fig. 24 - 10 dB 50 Hz boost tone control using change of pin 1 resistance (muting function)

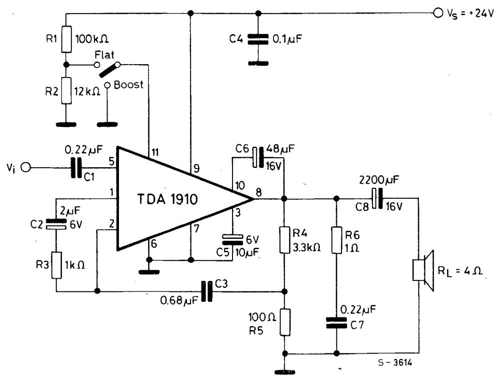


Fig. 25 - Frequency response of the circuit of fig. 24

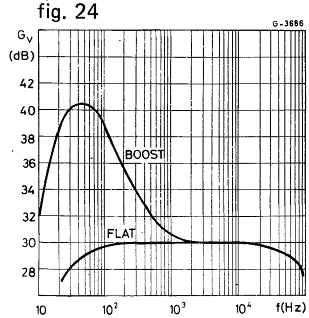


Fig. 26 - Squelch function in TV applications

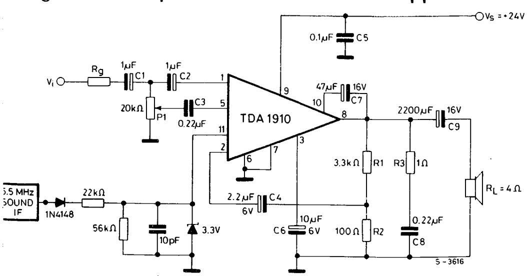
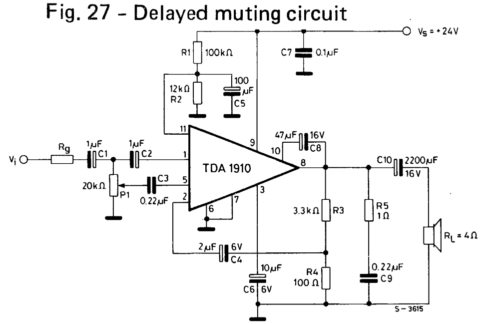


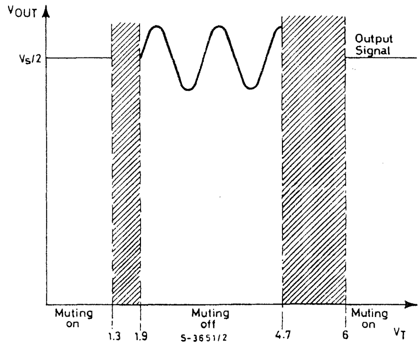
Fig. 27 - Delayed muting circuit



MUTING FUNCTION

The output signal can be inhibited applying a DC voltage V_T to pin 11, as shown in fig. 28

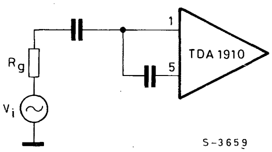
Fig. 28



The input resistance at pin 1 depends on the threshold voltage V_T at pin 11 and is typically.

$R_1 = 200\ K\Omega$	@	$1.9V \leqslant V_T \leqslant 4.7V$	muting-off
$R_1 = 10\ \Omega$	@	$0V \leqslant V_T \leqslant 1.3V$ $6V \leqslant V_T \leqslant V_s$	muting-on

Referring to the following input stage, the possible attenuation of the input signal and therefore of the output signal can be found using the following expression.



$$A_T = \frac{V_i}{V_5} = \frac{R_g + R_5//R_1}{R_5//R_1}$$

where $R_5 \cong 100\ K\Omega$

Considering $R_g = 10\ K\Omega$ the attenuation in the muting-on condition is typically $A_T = 60$ dB. In the muting-off condition, the attenuation is very low, typically 1.2 dB.
A very low current is necessary to drive the threshold voltage V_T because the input resistance at pin 11 is greater than 150 $K\Omega$. The muting function can be used in many cases, when a temporary inhibition of the output signal is requested, for example:

- in switch-on condition, to avoid preamplifier power-on transients (see fig. 27)
- during commutations at the input stages.
- during the receiver tuning.

The variable impedance capability at pin 1 can be useful in many applications and we have shown 2 examples in fig. 22 and 24, where it has been used to change the feedback network, obtaining 2 different frequency responses.

APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 21. Different values can be used.
The following table can help the designer.

Component	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value	Allowed range Min.	Max.
$R_g + R_1$	10KΩ	Input signal imped. for muting operation	Increase of the attenuation in muting-on condition. Decrease of the input sensitivity.	Decrease of the attenuation in muting on condition.		
R_2	3.3KΩ	Close loop gain setting.	Increase of gain.	Decrease of gain. Increase quiescent current.	9 R_3	
R_3	100Ω	Close loop gain setting.	Decrease of gain.	Increase of gain.		$R_2/9$
R_4	1Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads.			
P_1	20KΩ	Volume potentiometer.	Increase of the switch-on noise.	Decrease of the input impedance and the input level.	10KΩ	100KΩ
C_1 C_2 C_3	1 μF 1 μF 0.22 μF	Input DC decoupling.		Higher low frequency cutoff.		
C_4	2.2 μF	Inverting input DC decoupling.	Increase of the switch-on noise.	Higher low frequency cutoff.	0.1 μF	
C_5	0.1 μF	Supply voltage bypass.		Danger of oscillations.		
C_6	10 μF	Ripple Rejection.	Increase of SVR. Increase of the switch-on time.	Degradation of SVR.	2.2 μF	100 μF
C_7	47 μF	Bootstrap.		Increase of the distortion at low frequency.	10 μF	100 μF
C_8	0.22 μF	Frequency stability.		Danger of oscillation.		
C_9	2200 μF (R_L = 4Ω) 1000 μF (R_L = 8Ω)	Output DC decoupling.		Higher low frequency cutoff.		

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
   If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 31 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 29 - Output power and drain current vs. case temperature

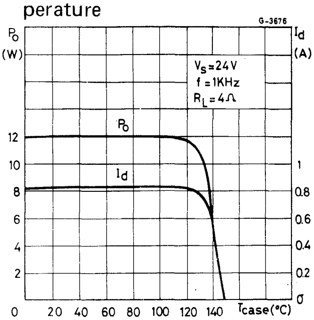


Fig. 30 - Output power and drain current vs. case temperature

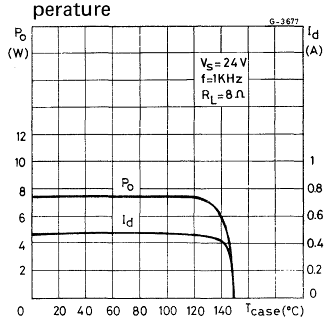
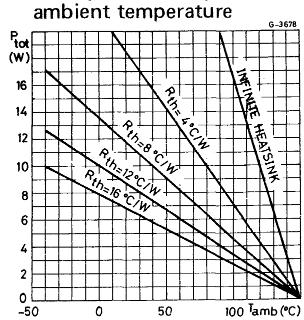


Fig. 31 - Maximum allowable power dissipation vs. ambient temperature

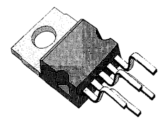


MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

10W CAR RADIO AUDIO AMPLIFIER

The TDA 2003 has improved performance with the same pin configuration as the TDA 2002. The additional features of TDA 2002, very low number of external components, ease of assembly, space and cost saving, are maintained.
The device provides a high output current capability (up to 3.5A) very low harmonic and crossover distortion.
Completely safe operation is guaranteed due to protection against DC and AC short circuit between all pins and ground, thermal over-range, load dump voltage surge up to 40V and fortuitous open ground.



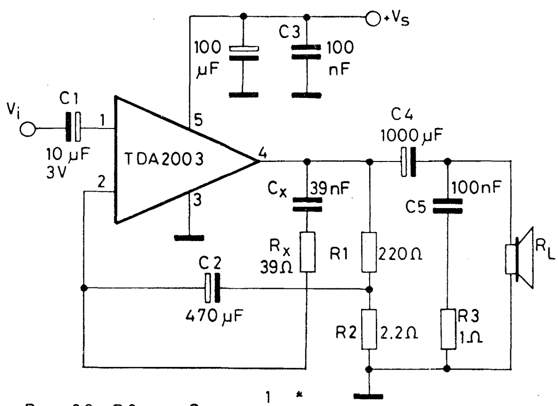
Pentawatt

ORDERING NUMBERS: TDA 2003H
TDA 2003V

ABSOLUTE MAXIMUM RATINGS

V_s	Peak supply voltage (50 ms)	40	V
V_s	DC supply voltage	28	V
V_s	Operating supply voltage	18	V
I_o	Output peak current (repetitive)	3.5	A
I_o	Output peak current (non repetitive)	4.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

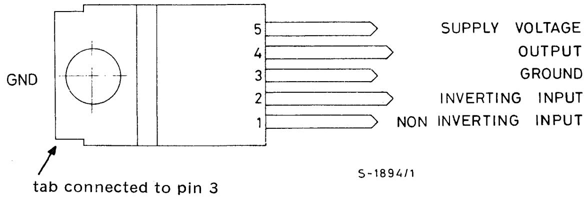
TEST CIRCUIT



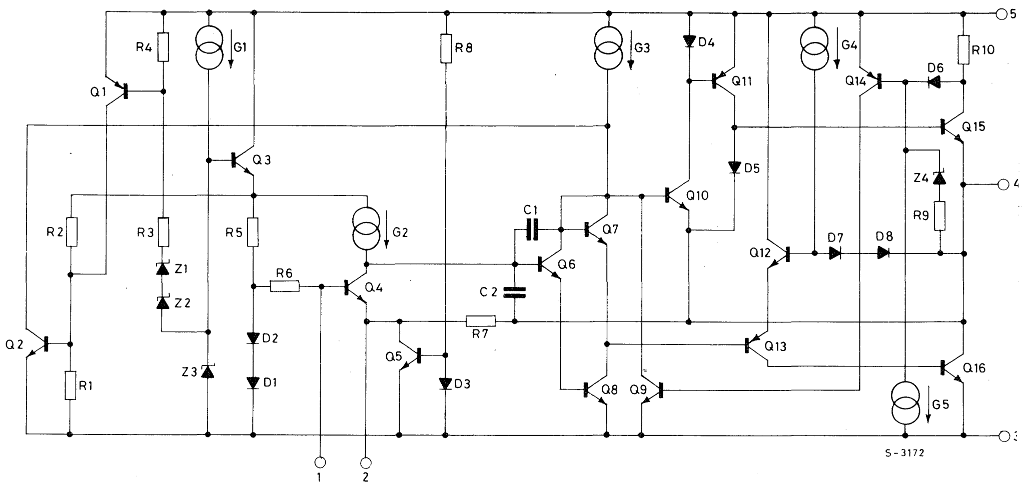
$R_X = 20 \cdot R2$; $C_X = \frac{1}{2\pi B R1}$ *

S - 3205

CONNECTION DIAGRAM
(top view)



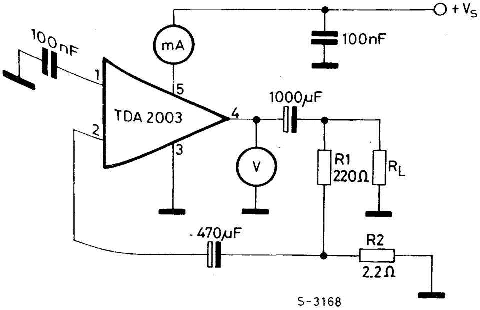
SCHEMATIC DIAGRAM



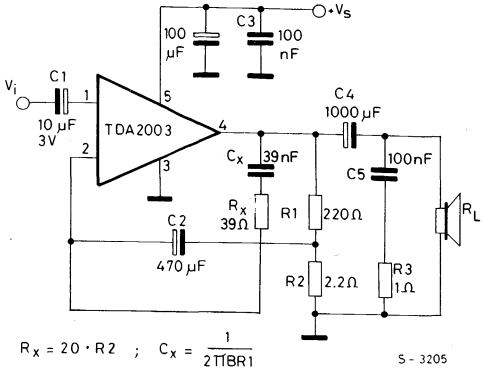
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

DC TEST CIRCUIT



AC TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_s = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS (Refer to DC test circuit)						
V_s	Supply voltage		8		18	V
V_o	Quiescent output voltage (pin 4)		6.1	6.9	7.7	V
I_d	Quiescent drain current (pin 5)			44	50	mA
AC CHARACTERISTICS (Refer to AC test circuit, G_v = 40 dB)						
P_o	Output power	d = 10% f = 1 kHz R_L = 4Ω R_L = 2Ω R_L = 3.2Ω R_L = 1.6Ω	 5.5 9	 6 10 7.5 12		 W W W W
$V_{i(rms)}$	Input saturation voltage		300			mV
V_i	Input sensitivity	f = 1 kHz P_o = 0.5W R_L = 4Ω P_o = 6W R_L = 4Ω P_o = 0.5W R_L = 2Ω P_o = 10W R_L = 2Ω		 14 55 10 50		 mV mV mV mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
B	Frequency response (–3 dB)	P_o = 1W R_L = 4Ω		40 to 15,000		Hz
d	Distortion	f = 1 kHz P_o = 0.05 to 4.5W R_L = 4Ω P_o = 0.05 to 7.5W R_L = 2Ω		 0.15 0.15		 % %
R_i	Input resistance (pin 1)	f = 1 kHz	70	150		kΩ
G_v	Voltage gain (open loop)	f = 1 kHz f = 10 kHz		80 60		dB dB
G_v	Voltage gain (closed loop)	f = 1 kHz R_L = 4Ω	39.3	40	40.3	dB
e_N	Input noise voltage (0)			1	5	μV
i_N	Input noise current (0)			60	200	pA
η	Efficiency	f = 1 kHz P_o = 6W R_L = 4Ω P_o = 10W R_L = 2Ω		 69 65		 % %
SVR	Supply voltage rejection	f = 100 Hz V_{ripple} = 0.5V R_g = 10 kΩ R_L = 4Ω	30	36		dB

(0) Filter with noise bandwidth: 22 Hz to 22 kHz

Fig. 1 – Quiescent output voltage vs. supply voltage

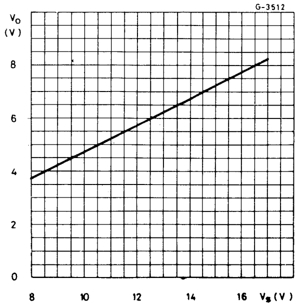


Fig. 2 – Quiescent drain current vs. supply voltage

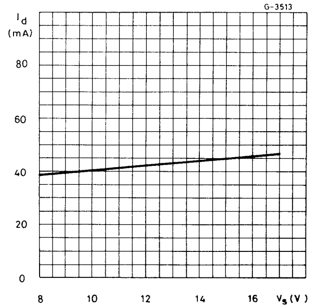
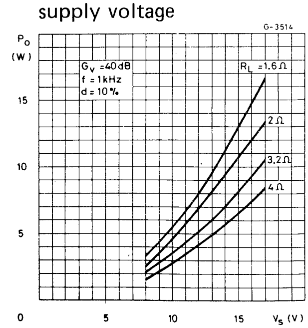


Fig. 3 – Output power vs. supply voltage



SGS-THOMSON MICROELECTRONICS

Fig. 4 - Output power vs. load resistance R_L

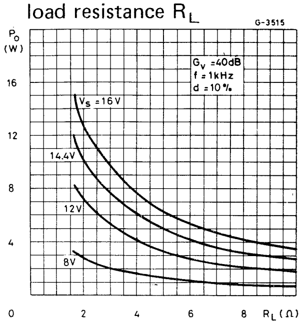


Fig. 5 - Gain vs. input sensitivity

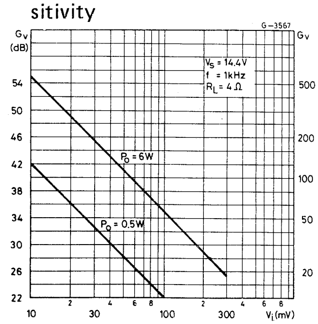


Fig. 6 - Gain vs. input sensitivity

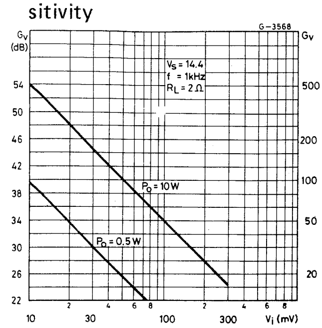


Fig. 7 - Distortion vs. output power

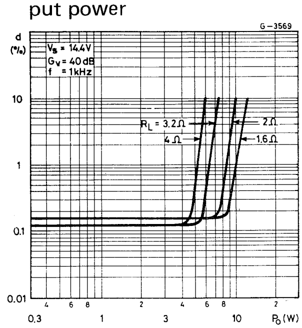


Fig. 8 - Distortion vs. frequency

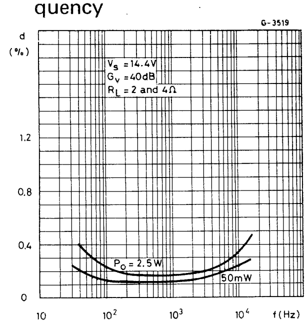


Fig. 9 - Supply voltage rejection vs. voltage gain

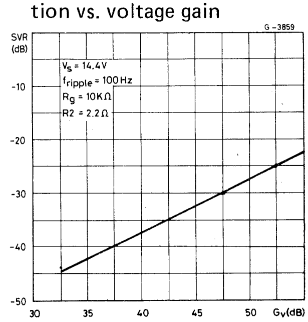


Fig. 10 - Supply voltage rejection vs. frequency

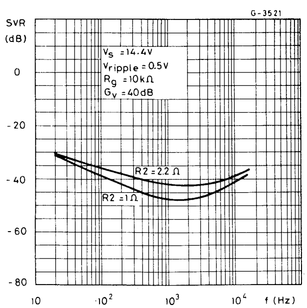


Fig. 11 - Power dissipation and efficiency vs. output power ($R_L = 4\Omega$)

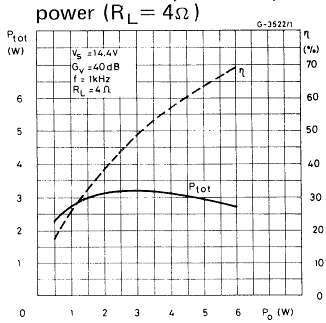


Fig. 12 - Power dissipation and efficiency vs. output power ($R_L = 2\Omega$)

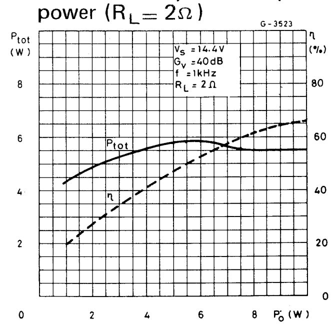


Fig. 13 - Maximum power dissipation vs. supply voltage (sine wave operation)

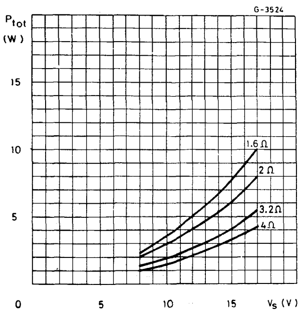


Fig. 14 - Maximum allowable power dissipation vs. ambient temperature

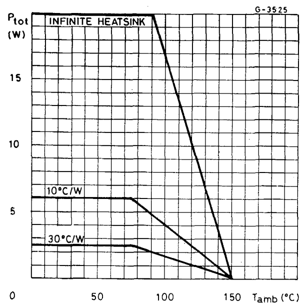
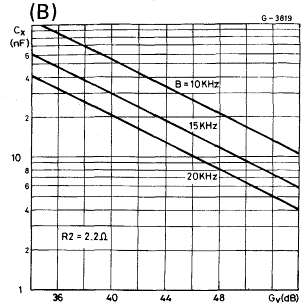


Fig. 15 - Typical values of capacitor (C_X) for different values of frequency response (B)



APPLICATION INFORMATION

Fig. 16 - Typical application circuit

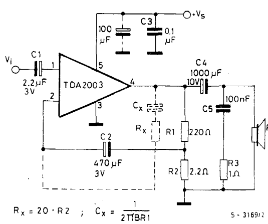


Fig. 17 - P.C. board and component layout for the circuit of fig. 16 (1:1 scale)

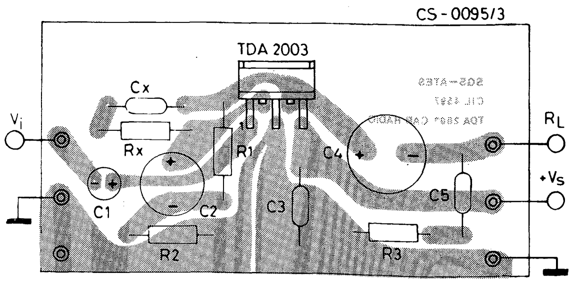
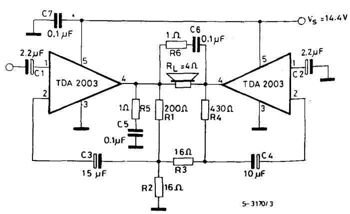
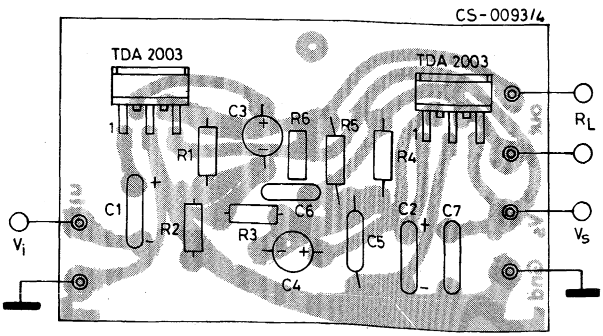


Fig. 18 - 20W bridge configuration application circuit (*)



(*) The values of the capacitors C3 and C4 are different to optimize the SVR (Typ.= 40 dB)

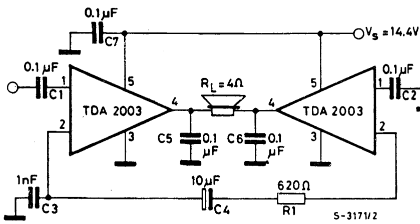
Fig. 19 - P.C. board and component layout for the circuit of fig. 18 (1:1 scale)



SGS-THOMSON MICROELECTRONICS

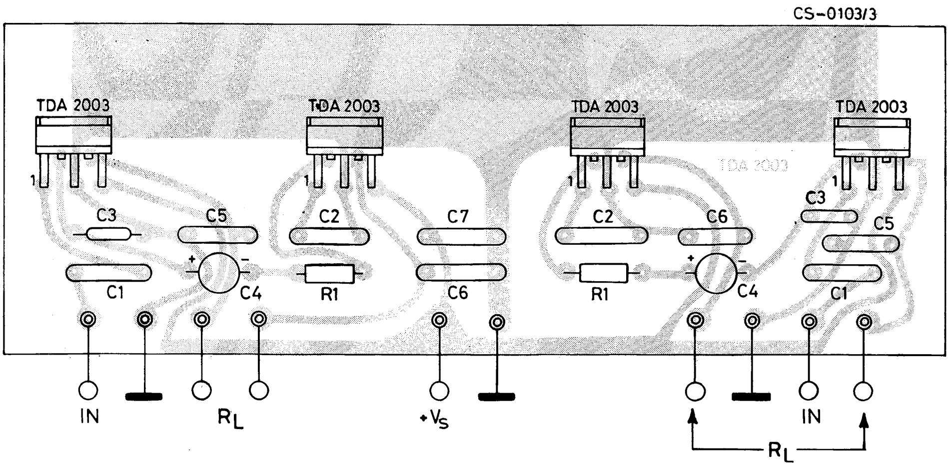
APPLICATION INFORMATION (continued)

Fig. 20 - Low cost bridge configuration application circuit (*) (P_o = 18W)



(*) In this application the device can support a short circuit between every side of the loudspeaker and ground.

Fig. 21 - P.C. board and component layout for the low-cost bridge amplifier of fig. 20, in stereo version (1:1 scale)



BUILT-IN PROTECTION SYSTEMS

Load dump voltage surge

The TDA 2003 has a circuit which enables it to withstand a voltage pulse train, on pin 5, of the type shown in fig. 23.
If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 5, in order to assure that the pulses at pin 5 will be held within the limits shown in fig. 22.

A suggested LC network is shown in fig. 23. With this network, a train of pulses with amplitude up to 120V and width of 2 ms can be applied at point A. This type of protection is ON when the supply voltage (pulsed or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 22

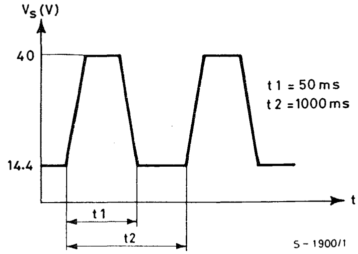
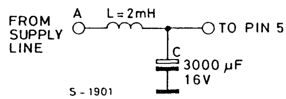


Fig. 23



Short-circuit (AC and DC conditions)

The TDA 2003 can withstand a permanent short-circuit on the output for a supply voltage up to 16V.

Polarity inversion

High current (up to 5A) can be handled by the device with no damage for a longer period than the blow--out time of a quick 1A fuse (normally connected in series with the supply).
This feature is added to avoid destruction if, during fitting to the car, a mistake on the connection of the supply is made.

Open ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA 2003 protection diodes are included to avoid any damage.

Inductive load

A protection diode is provided between pin 4 and 5 (see the internal schematic diagram) to allow use of the TDA 2003 with inductive loads. In particular, the TDA 2003 can drive a coupling transformer for audio modulation.

DC voltage

The maximum operating DC voltage on the TDA 2003 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries were series connected to crank the engine.

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), oran excessive ambient temperature can be easily withstood.
2) the heat-sink can have a smaller factor compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced.

Fig. 24 - Output power and drain current vs. case temperature (R_L = 4 Ω)

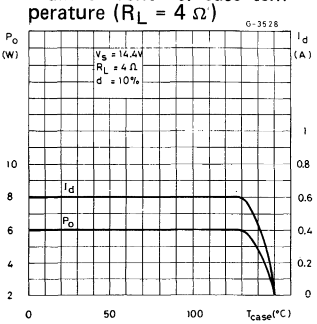
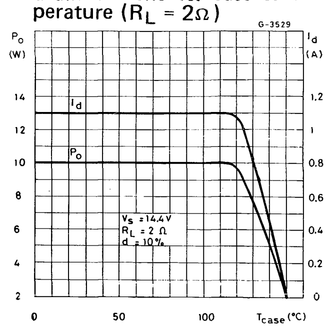


Fig. 25 - Output power and drain current vs. case temperature (R_L = 2Ω)



PRATICAL CONSIDERATION

Printed circuit board

The layout shown in fig. 17 is recommended. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground of the output through which a rather high current flows.

Assembly suggestion

No electrical insulation is required between the package and the heat-sink. Pin length should be as short as possible. The soldering temperature must not exceed 260°C for 12 seconds.

Application suggestions

The recommended component values are those sjown in the application circuits of fig. 16. Different values can be used. The following table is intended to aid the car-radio designer.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
C1	2.2 μF	Input DC decoupling		Noise at switch-on, switch-off
C2	470 μF	Ripple rejection		Degradation of SVR
C3	0.1 μF	Supply bypassing		Danger of oscillation
C4	1000 μF	Output coupling to load		Higher low frequency cutoff
C5	0.1 μF	Frequency stability		Danger of oscillation at high frequencies with inductive loads
C_X	$\cong \frac{1}{2 \pi B R1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
R1	$(G_V-1) \cdot R2$	Setting of gain		Increase of drain current
R2	2.2 Ω	Setting of gain and SVR	Degradation of SVR	
R3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_X	≅ 20 R2	Upper frequency cutoff	Poor high frequency attenuation	Danger of oscillation

10+10W STEREO AMPLIFIER FOR CAR RADIO

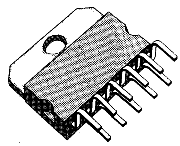
The TDA2004A is a class B dual audio power amplifier in MULTIWATT® package specifically designed for car radio applications; stereo amplifiers are easily designed using this device that provides a high current capability (up to 3.5A) and that can drive very low impedance loads (down to 1.6Ω).

Its main features are:

Low distortion.
Low noise.
High reliability of the chip and of the package with additional safety during operation thanks to protections against:

- output AC short circuit to ground;
- very inductive loads
- overrating chip temperature;
- load dump voltage surge;
- fortuitous open ground;

Space and cost saving: very low number of external components. very simple mounting system with no electrical isolation between the package and the heatsink.



Multiwatt-11

ORDERING NUMBER: TDA2004A

ABSOLUTE MAXIMUM RATINGS

V_s	Operating supply voltage	18	V
V_s	DC supply voltage	28	V
V_s	Peak supply voltage (for 50ms)	40	V
I_o (*)	Output peak current (non repetitive t = 0.1ms)	4.5	A
I_o (*)	Output peak current (repetitive f ⩾ 10Hz)	3.5	A
P_{tot}	Power dissipation at T_{case} = 60°C	30	W
T_j, T_{stg}	Storage and junction temperature	-40 to 150	°C

(*) The max. output current is internally limited.

CONNECTION DIAGRAM

(Top view)

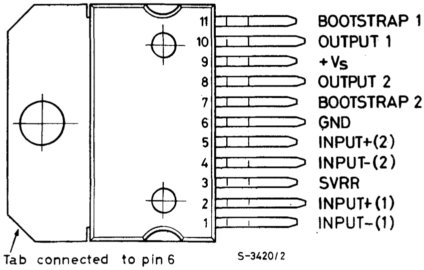


Fig. 1 - Test and application circuit

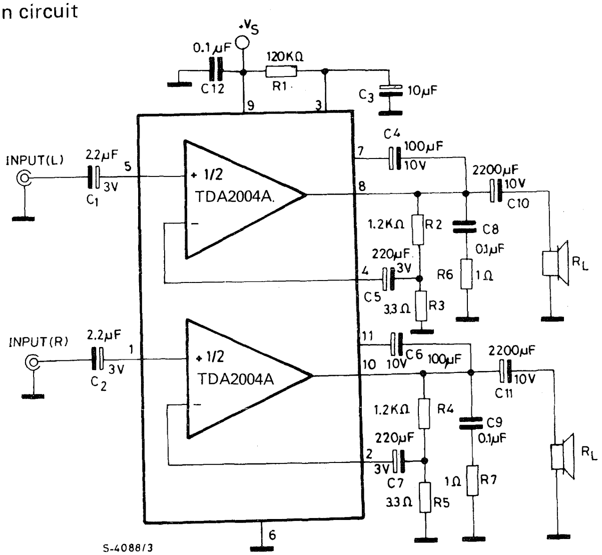
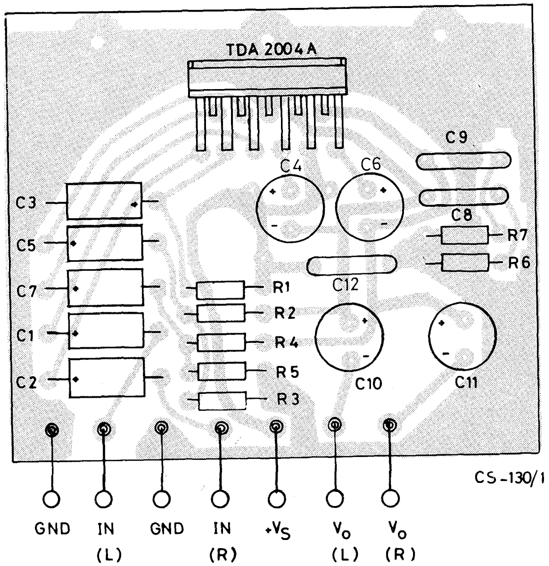


Fig. 2 - PC board and components layout (scale 1:1)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C, G_v= 50 dB, $R_{th\ (heatsink)}$ = 4°C/W, unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		18	V
V_o	Quiescent output voltage	V_s = 14.4V V_s = 13.2V	6.6 6.0	7.2 6.6	7.8 7.2	V V
I_d	Total quiescent drain current	V_s = 14.4V V_s = 13.2V		65 62	120 120	mA mA
I_{SB}	Stand-by current	Pin 3 grounded		5		mA
P_o	Output power (each channel)	f = 1 KHz d = 10% V_s = 14.4V R_L= 4Ω R_L= 3.2Ω R_L= 2Ω R_L= 1.6Ω V_s = 13.2V R_L= 3.2Ω R_L= 1.6Ω V_s = 16V R_L= 2 Ω	 6 7 9 10 6 9 	 6.5 8 10(*) 11 6.5 10 12		 W W W W W W W
d	Distortion (each channel)	f = 1 KHz V_s = 14.4V R_L= 4Ω P_o= 50 mW to 4W V_s = 14.4V R_L= 2Ω P_o= 50 mW to 6W V_s = 13.2V R_L= 3.2Ω P_o= 50 mW to 3W V_s = 13.2V R_L= 1.6Ω P_o= 50 mW to 6W		 0.2 0.3 0.2 0.3	 1 1 1 1	 % % % %
CT	Cross talk	V_s = 14.4V V_o= 4 V_{rms} R_L= 4Ω f = 1 KHz f = 10 KHz R_g = 5 KΩ	 50 40	 60 45		 dB dB
V_i	Input saturation voltage		300			mV
R_i	Input resistance (non inverting input)	f = 1 KHz	70	200		KΩ
f_L	Low frequency roll off (-3 dB)	R_L= 4Ω R_L= 2Ω R_L= 3.2Ω R_L= 1.6Ω			35 50 40 55	Hz Hz Hz Hz
f_H	High frequency roll off (-3 dB)	R_L = 1.6Ω to 4Ω	15			KHz
G_v	Voltage gain (open loop)	f = 1 KHz		90		dB

ELECTRICAL CHARACTERISTICS (continued)

	Parameters	Test conditions	Min.	Typ.	Max.	Unit
G_V	Voltage gain (closed loop)	f = 1 KHz	48	50	51	dB
	Closed loop gain matching			0.5		dB
e_N	Total input noise voltage	R_g = 10 KΩ(°)		1.5	5	μV
SVR	Supply voltage rejection	f_{ripple} = 100 Hz R_g = 10 KΩ C_3 = 10 μF V_{ripple} = 0.5V_{rms}	35	45		dB
η	Efficiency	V_s = 14.4V f = 1 KHz R_L = 4Ω P_o = 6.5W R_L = 2Ω P_o = 10W V_s = 13.2V f = 1 KHz R_L = 3.2Ω P_o = 6.5W R_L = 1.6Ω P_o = 10W		 70 60 70 60		 % % % %
T_j	Thermal shut down junction temperature			145		°C

(*) 9.3W without bootstrap.
(°) Bandwidth filter: 22 Hz to 22 KHz.

Fig. 3 - Quiescent output voltage vs. supply voltage

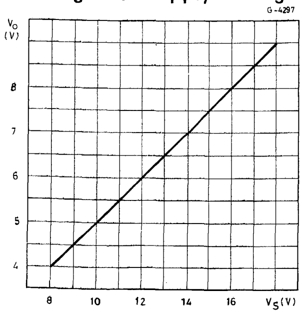


Fig. 4 - Quiescent drain current vs. supply voltage

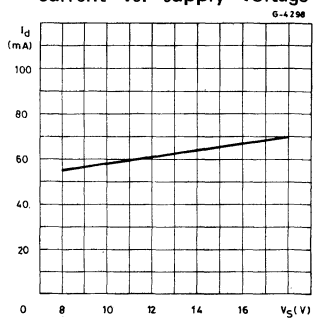


Fig. 5 - Distortion vs. output power

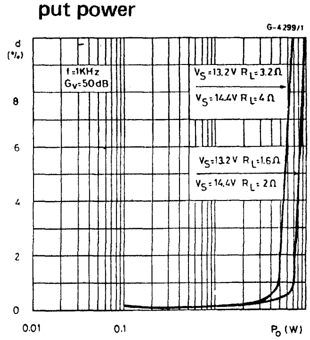


Fig. 6 - Output power vs. supply voltage

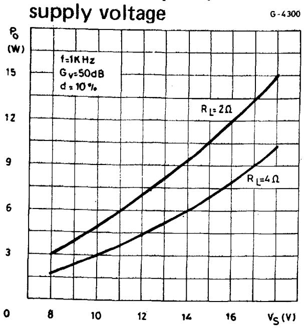


Fig. 7 - Output power vs. supply voltage

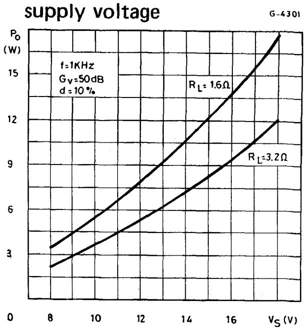


Fig. 8 - Distortion vs. frequency

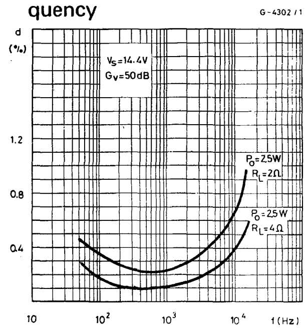


Fig. 9 - Distortion vs. frequency

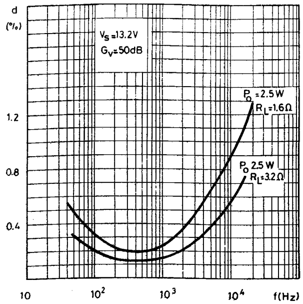


Fig. 10 - Supply voltage rejection vs. C_3

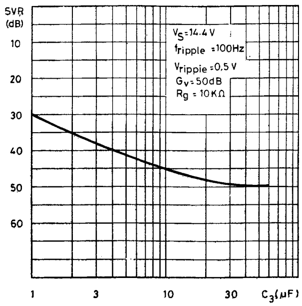


Fig. 11 - Supply voltage rejection vs. frequency

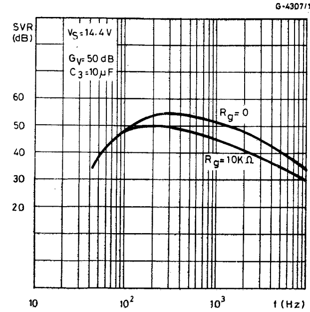


Fig. 12 - Supply voltage rejection vs. values of capacitors C_2 and C_3

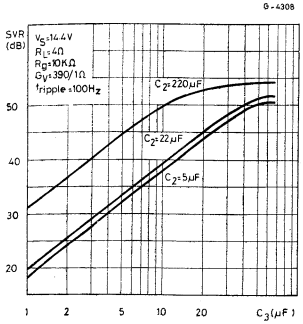


Fig. 13 - Supply voltage rejection vs. values of capacitors C_2 and C_3

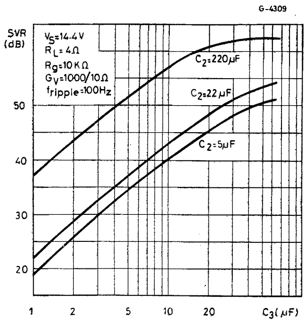


Fig. 14 - Gain vs. input sensitivity

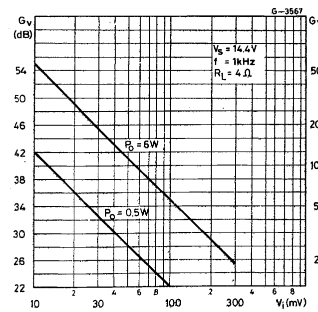


Fig. 15 - Maximum allowable power dissipation vs. ambient temperature

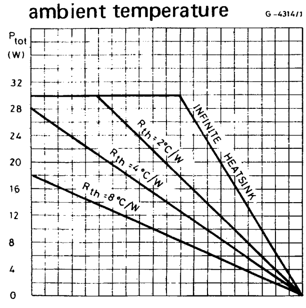


Fig. 16 - Total power dissipation and efficiency vs. output power

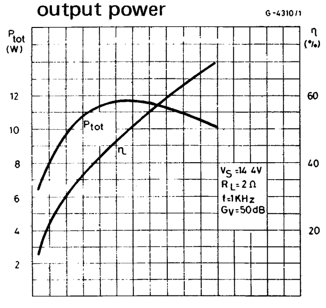
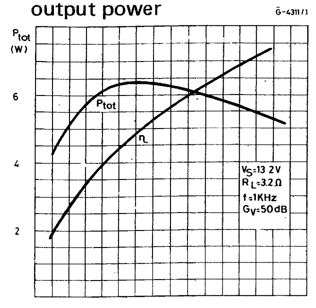


Fig. 17 - Total power dissipation and efficiency vs. output power



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 1. Different values can be used; the following table can help the designer.

Component	Recomm. value	Purpose	Larger than	Smaller than
R_1	120 KΩ	Optimisation of the output signal simmetry	Smaller $P_{o\ max}$	Smaller $P_{o\ max}$
R_2 and R_4	1 KΩ	Close loop gain setting (*)	Increase of gain	Decrease of gain
R_3 and R_5	3.3 Ω		Decrease of gain	Increase of gain
R_6 and R_7	1 Ω	Frequency stability	Danger of oscillation at high frequency with inductive load	
C_1 and C_2	2.2 μF	Input DC decoupling	High turn-on delay	High turn-on pop Higher low frequency cutoff. Increase of noise.
C_3	10 μF	Ripple rejection	Increase of SVR. Increase of the switch-on time.	Degradation of SVR.
C_4 and C_6	100 μF	Bootstrapping		Increase of distortion at low frequency.
C_5 and C_7	100 μF	Feedback Input DC decoupling.		
C_8 and C_9	0.1 μF	Frequency stability.		Danger of oscillation.
C_{10} and C_{11}	1000 μF to 2200 μF	Output DC decoupling.		Higher low-frequency cut-off.

(*) The closed-loop gain must be higher than 26dB

BUILT-IN PROTECTION SYSTEMS

Load dump voltage surge

The TDA2004A has a circuit which enables it to withstand a voltage pulse train, on pin 9, of the type shown in Fig. 19.

If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.

A suggested LC network is shown in Fig. 18. With this network, a train of pulse with amplitude up to 120V and with of 2ms can be applied to point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 18

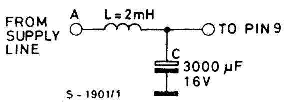
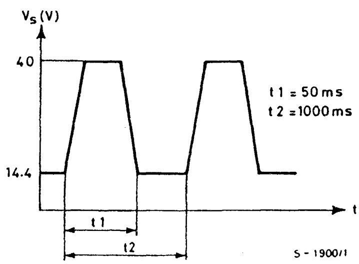


Fig. 19



Short circuit (AC conditions)

The TDA2004A can withstand an accidental short-circuit from the output to ground caused by a wrong connection during normal working.

Polarity inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This feature is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open ground

When the radio is the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA2004A protection diodes are included to avoid any damage.

Inductive load

A protection diode is provided to allow use of the TDA2004A with inductive loads.

DC voltage

The maximum operating DC voltage on the TDA2004 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is the P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 15 shown this dissipable power as a function of ambient temperature for different thermal resistance.

20W BRIDGE AMPLIFIER FOR CAR RADIO

The TDA2005 is class B dual audio power amplifier in MULTIWATT® package specifically designed for car radio application: **power booster amplifiers** are easily designed using this device that provides a high current capability (up to 3.5A) and that can drive very low impedance loads (down to 1.6Ω in stereo applications) obtaining an output power of more than 20W (bridge configuration).

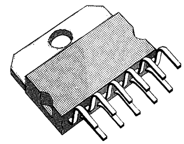
High output power: $P_o = 10 + 10W$ @ $R_L = 2\Omega$, d = 10%; $P_o = 20W$ @ $R_L = 4\Omega$, d = 10%.

High reliability of the chip and package with additional complete safety during operation thanks to protection against:

- output DC and AC short circuit to ground;
- overrating chip temperature
- load dump voltage surge
- fortuitous open ground
- very inductive loads

Flexibility in use: bridge or stereo booster amplifiers with or without boostrap and with programmable gain and bandwidth.

Space and cost saving: very low number of external components, very simple mounting system with no electrical isolation between the package and the heatsink (one screw only).
In addition, the circuit offers **loudspeaker protection** during short circuit for one wire to ground.



Multiwatt-11®

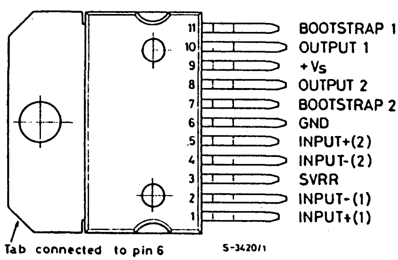
ORDERING NUMBERS:
TDA2005M - Bridge application
TDA2005S - Stereo application

ABSOLUTE MAXIMUM RATINGS

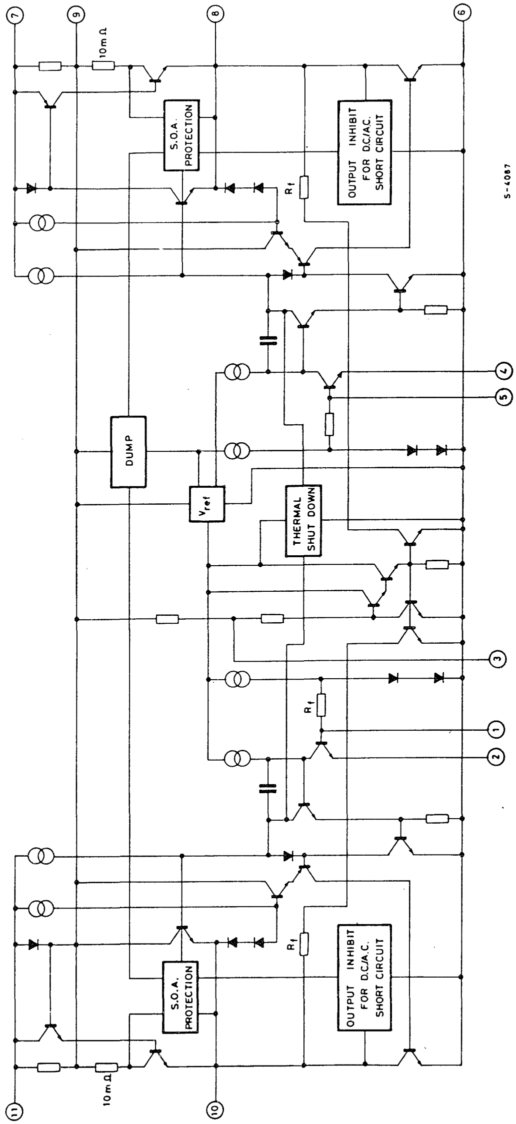
V_s	Operating supply voltage	18	V
V_s	DC supply voltage	28	V
V_s	Peak supply voltage (for 50ms)	40	V
I_o (*)	Output peak current (non repetitive t = 0.1ms)	4.5	A
I_o (*)	Output peak current (repetitive f ⩾ 10Hz)	3.5	A
P_{tot}	Power dissipation at $T_{case} = 60°C$	30	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

(*) The max. output current is internally limited.

CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

BRIDGE AMPLIFIER APPLICATION (TDA 2005M)

Fig. 1 - Test and application circuit (Bridge amplifier)

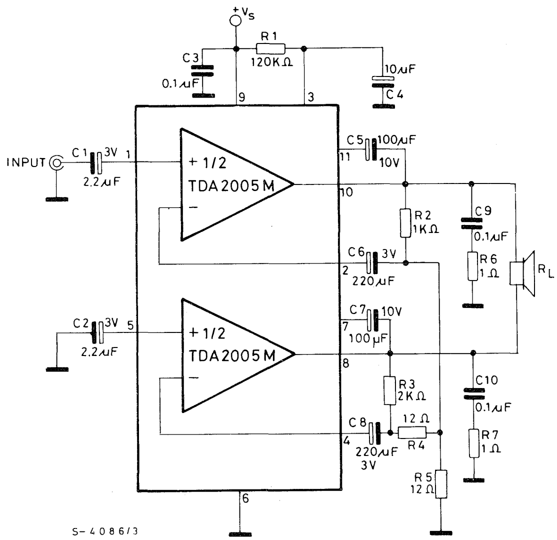
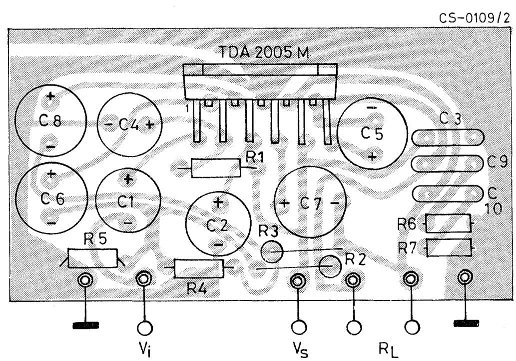


Fig. 2 - P.C. board and component layout (scale 1:1)



ELECTRICAL CHARACTERISTICS (Refer to the **bridge** application circuit, T_{amb} = 25°C, G_v = 50 dB, $R_{th\ (heatsink)}$ = 4°C/W, unless otherwise specified).

	Parameters	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		18	V
V_{os}	Output offset voltage(°) (between pin 8 and 10)	V_s = 14.4V V_s = 13.2V			150 150	mV mV
I_d	Total quiescent drain current	V_s = 14.4V R_L = 4Ω		75	150	mA
		V_s = 13.2V R_L = 3.2 Ω		70	160	mA
P_o	Output power	d = 10% f = 1 KHz V_s = 14.4V R_L = 4Ω R_L = 3.2Ω V_s = 13.2V R_L = 3.2Ω	 18 20 17	 20 22 19		 W W W
d	Distortion	f = 1 KHz V_s = 14.4V R_L = 4Ω P_o = 50 mW to 15W V_s = 13.2V R_L = 3.2Ω P_o = 50 mW to 13W			 1 1	 % %
V_i.	Input sensitivity	f = 1 KHz P_o = 2W R_L = 4Ω P_o = 2W R_L = 3.2Ω		 9 8		 mV mV
R_i	Input resistance	f = 1 KHz	70			KΩ
f_L	Low frequency roll off (-3 dB)	R_L = 3.2 Ω			40	Hz
f_H	High frequency roll off (-3 dB)	R_L = 3.2 Ω	20			KHz
G_v	Closed loop voltage gain	f = 1 KHz		50		dB
e_N	Total input noise voltage	R_g = 10 KΩ(°°)		3	10	μV
SVR	Supply voltage rejection	R_g = 10 KΩ C_4 = 10 μF f_{ripple} = 100 Hz V_{ripple} = 0.5 V	45	55		dB
η	Efficiency	V_s = 14.4V f = 1 KHz P_o = 20W R_L = 4Ω P_o = 22W R_L = 3.2Ω V_s = 13.2V f = 1 KHz P_o = 19W R_L = 3.2Ω		 60 60 58		 % % %
T_j	Thermal shut-down junction temperature	V_s = 14.4V R_L = 4Ω f = 1 KHz P_{tot} = 13W		145		°C
V_{OSH}	Output voltage with one side of the speaker shorted to ground	V_s = 14.4V R_L = 4Ω V_s = 13.2V R_L = 3.2Ω			2	V

(°) For TDA 2005M only.
(°°) Bandwidth filter: 22 Hz to 22 KHz.

Fig. 3 - Output offset voltage vs. supply voltage

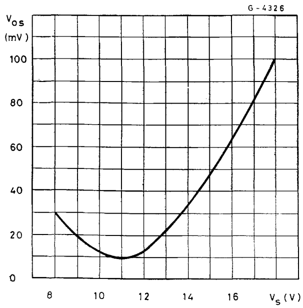


Fig. 4 - Distortion vs. output power (Bridge amplifier)

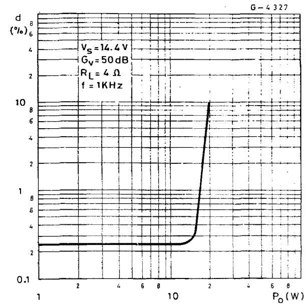
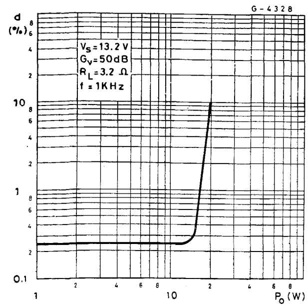


Fig. 5 - Distorsion vs. output power (Bridge amplifier)



BRIDGE AMPLIFIER DESIGN

The following considerations can be useful when designing a bridge amplifier.

Parameter		Single ended	Bridge
$V_{o\,max}$	Peak output voltage (before clipping)	$\frac{1}{2}(V_s - 2\,V_{CE\,sat})$	$V_s - 2\,V_{CE\,sat}$
$I_{o\,max}$	Peak output current (before clipping)	$\frac{1}{2}\frac{(V_s - 2\,V_{CE\,sat})}{R_L}$	$\frac{V_s - 2\,V_{CE\,sat}}{R_L}$
$P_{o\,max}$	rms output power (before clipping)	$\frac{1}{4}\frac{(V_s - 2\,V_{CE\,sat})^2}{2\,R_L}$	$\frac{(V_s - 2\,V_{CE\,sat})^2}{2\,R_L}$

where: $V_{CE\,sat}$ = output transistors saturation voltage
V_S = allowable supply voltage
R_L = load impedance.

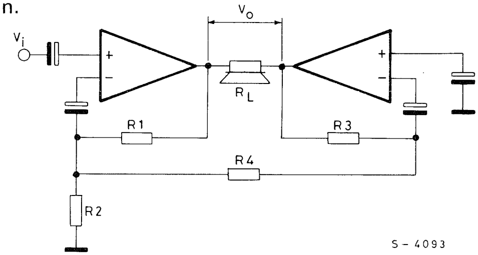
Voltage and current swings are twice for a bridge amplifier in comparison with single ended amplifier. In order words, with the same R_L the bridge configuration can deliver an output power that is four times the output power of a single ended amplifier, while, with the same max output current the bridge configuration can deliver an output power that is twice the output power of a single ended amplifier. Core must be taken when selecting V_s and R_L in order to avoid an output peak current above the absolute maximum rating.

From the expression for $I_{o\,max}$, assuming V_s = 14.4V and $V_{CE\,sat}$ = 2V, the minimum load that can be driven by TDA2005 in bridge configuration is:

$$R_{L\,min} = \frac{V_s - 2\,V_{CEsat}}{I_{o\,max}} = \frac{14.4 - 4}{3.5} = 2.97\ \Omega$$

BRIDGE AMPLIFIER DESIGN (continued)

Fig. 6 - Bridge configuration.



The voltage gain of the bridge configuration is given by (see fig. 6):

$$G_v = \frac{V_o}{V_i} = 1 + \frac{R_1}{\left(\frac{R_2 \cdot R_4}{R_2 + R_4}\right)} + \frac{R_3}{R_4}$$

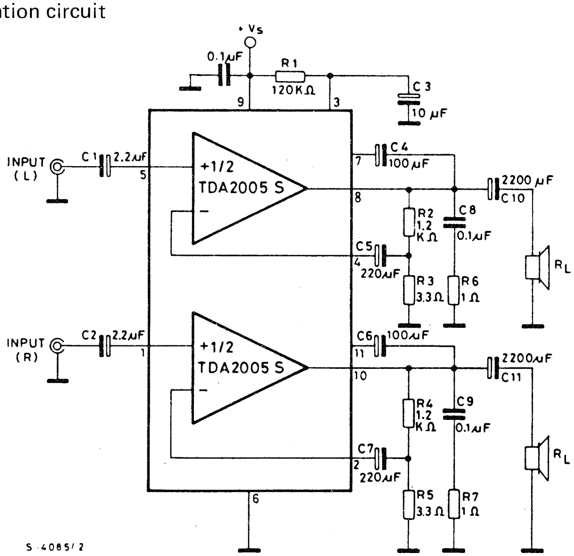
For sufficiently high gains (40 ÷ 50 dB) it is possible to put $R_2 = R_4$ and $R_3 = 2\ R_1$, simplifing the formula in:

$$G_v = 4\ \frac{R_1}{R_2}$$

G_v (dB)	R_1 (Ω)	$R_2 = R_4$ (Ω)	R_3 (Ω)
40	1000	39	2000
50	1000	12	2000

STEREO AMPLIFIER APPLICATION (TDA 2005S)

Fig. 7 - Typical application circuit



ELECTRICAL CHARACTERISTICS (Refer to the **stereo** application circuit, T_{amb} = 25°C, G_v = 50 dB, $R_{th\ (heatsink)}$ = 4°C/W, unless otherwise specified).

	Parameters	Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			8		18	V
V_o	Quiescent output voltage	V_s = 14.4V V_s = 13.2V		6.6 6	7.2 6.6	7.8 7.2	V V
I_d	Total quiescent drain current	V_s = 14.4V V_s = 13.2V			65 62	120 120	mA mA
P_o	Output power (each channel)	f = 1 KHz V_s = 14.4V V_s = 13.2V V_s = 16V	d = 10% R_L = 4Ω R_L = 3.2Ω R_L = 2Ω R_L = 1.6Ω R_L = 3.2Ω R_L = 1.6Ω R_L = 2Ω	 6 7 9 10 6 9 	 6.5 8 10 11 6.5 10 12		 W W W W W W W
d	Distortion (each channel)	f = 1 KHz V_s = 14.4V P_o = 50 mW to 4W V_s = 14.4V P_o = 50 mW to 6W V_s = 13.2V P_o = 50 mW to 3W V_s = 13.2V P_o = 40 mW to 6W	 R_L = 4Ω R_L = 2Ω R_L = 3.2Ω R_L = 1.6Ω 		 0.2 0.3 0.2 0.3	 1 1 1 1	 % % % %
CT	Cross talk (°)	V_s = 14.4V R_L = 4Ω V_o = 4V_{rms} R_g = 5 KΩ	f = 1 KHz		60		dB
			f = 10 KHz		45		dB
V_i	Input saturation voltage			300			mV
V_i	Input sensitivity	f = 1 KHz	P_o = 1W R_L = 4Ω R_L = 3.2Ω		 6 5.5		mV
R_i	Input resistance	f = 1 KHz		70	200		KΩ
f_L	Low frequency roll off (-3 dB)	R_L = 2Ω				50	Hz
f_H	High frequency roll off (-3 dB)	R_L = 2Ω		15			KHz
G_v	Voltage gain (open loop)	f = 1 KHz			90		dB
G_v	Voltage gain (closed loop)	f = 1 KHz		48	50	51	dB
ΔG_v	Closed loop gain matching				0.5		dB
e_N	Total input noise voltage	R_g = 10 KΩ (°°)			1.5	5	μV

(°) For TDA 2005S only.
(°°) Bandwidth filter: 22 Hz to 22 KHz.

ELECTRICAL CHARACTERISTICS (continued)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection	R_g= 10 KΩ f_{ripple}= 100 Hz C_3= 10 μF V_{ripple}= 0.5V	35	45		dB
η	Efficiency	V_s = 14.4V f = 1 KHz R_L= 4Ω P_o= 6.5W R_L= 2Ω P_o= 10W V_s = 13.2V f = 1 KHz R_L= 3.2Ω P_o= 6.5W R_L= 1.6Ω P_o= 10W		 70 60 70 60		 % % % %
T_j	Thermal shut-down junction temperature			145		°C

Fig. 8 - Quiescent output voltage vs. supply voltage

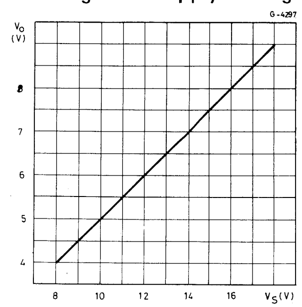


Fig. 9 - Quiescent drain current vs. supply voltage

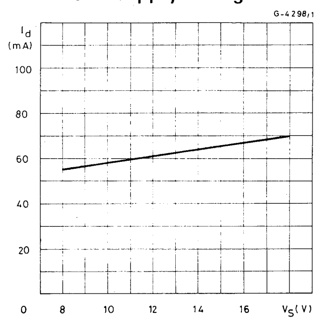


Fig. 10 - Distortion vs. output power

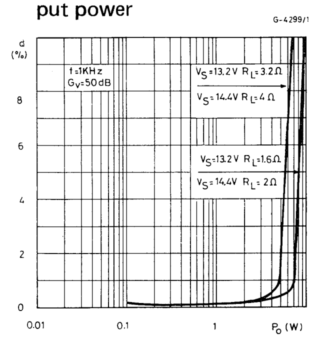


Fig. 11 - Output power vs. supply voltage

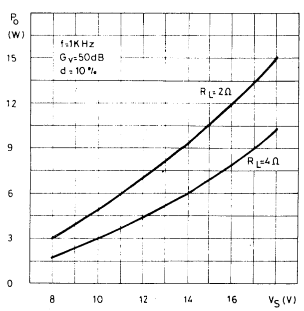


Fig. 12 - Output power vs. supply voltage

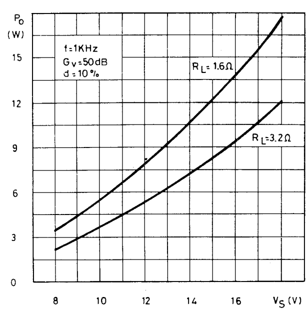
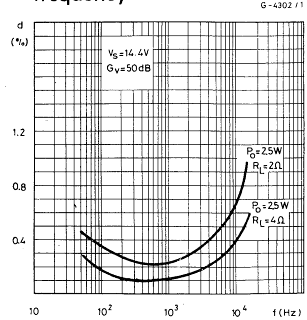


Fig. 13 - Distortion vs. frequency



SGS-THOMSON MICROELECTRONICS

Fig. 14 - Distorsion vs. frequency

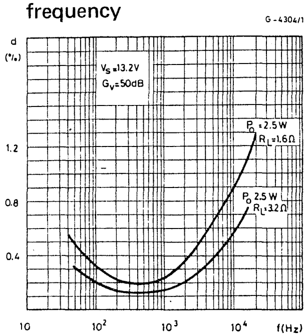


Fig. 15 - Supply voltage rejection vs. C_3

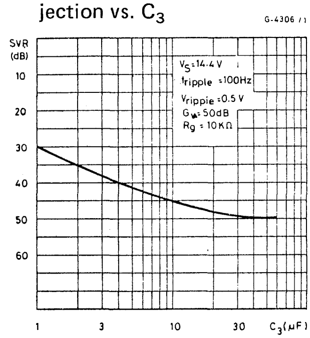


Fig. 16 - Supply voltage rejection vs. frequency

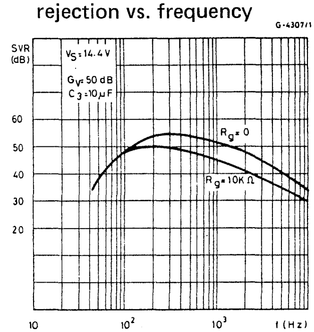


Fig. 17 - Supply voltage rejection vs. values of capacitors C_2 and C_3

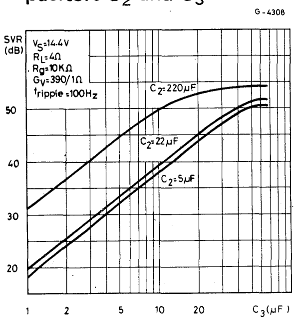


Fig. 18 - Supply voltage rejection vs. values of capacitors C_2 and C_3

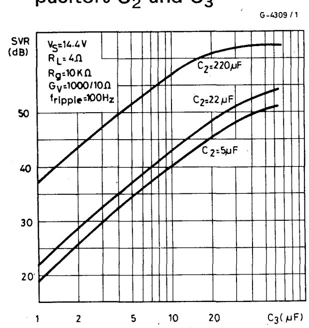


Fig. 19 - Gain vs. input sensitivity

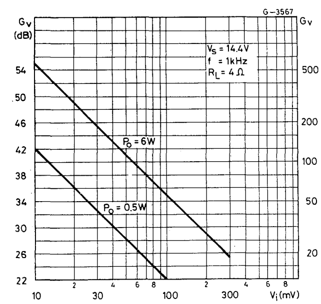


Fig. 20 - Gain vs. input sensitivity

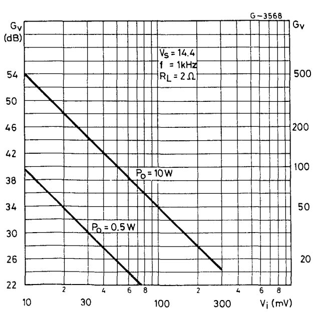


Fig. 21 - Total power dissipation and efficiency vs. output power (bridge)

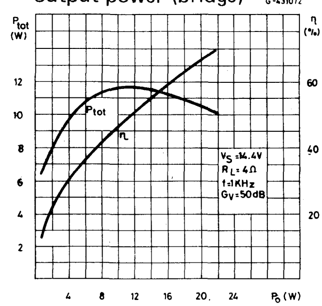
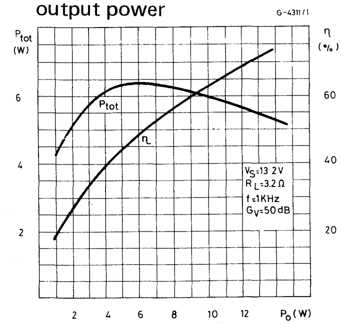


Fig. 22 - Total power dissipation and efficiency vs. output power



APPLICATION SUGGESTION

The recommended values of the components are those shown on Bridge application circuit of fig. 1. Different values can be used, the following table can help the designer.

Component	Recommended Value	Purpose	Larger than	Smaller than
R_1	120 KΩ	Optimization of the output symmetry	Smaller $P_{o\ max}$	Smaller $P_{o\ max}$
R_2	1 KΩ	Closed loop gain setting (see BRIDGE AMPLIFIER DESIGN) (*)		
R_3	2 KΩ			
R_4 and R_5	12 Ω			
R_6 and R_7	1 Ω	Frequency stability	Danger of oscillation at high frequency with inductive loads	
C_1	2.2 µF	Input DC decoupling	High turn on delay	Higher turn on pop. Higher low frequency cutoff. Increase of noise.
C_2	2.2 µF	Optimization of turn on pop and turn on delay.		
C_3	0.1 µF	Supply by pass		Danger of oscillation.
C_4	10 µF	Ripple Rejection	Increase of SVR. Increase of the switch-on time.	Degradation of SVR.
C_5 and C_7	100 µF	Bootstrapping		Increase of distortion at low frequency.
C_6 and C_8	220 µF	Feedback input DC decoupling, low frequency cutoff.		Higher low frequency cutoff.
C_9 and C_{10}	0.1 µF	Frequency stability.		Danger of oscillation.

(*) The closed loop gain must be higher than 32dB.

APPLICATION INFORMATION

Fig. 23 - Bridge amplifier without boostrap

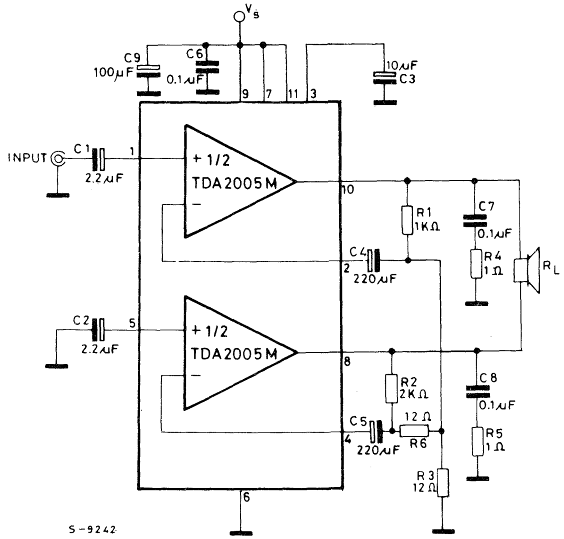
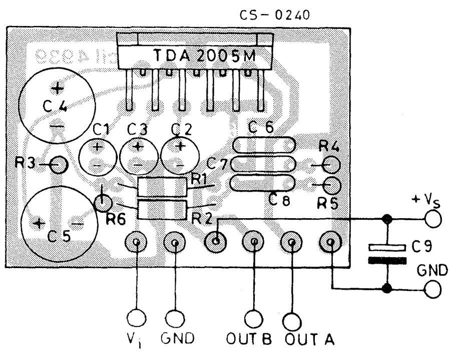


Fig. 24 - P.C. board and component layout of the circuit of Fig. 23 (1 : 1 scale)



APPLICATION INFORMATION (continued)

Fig. 25 - Dual - Bridge amplifier

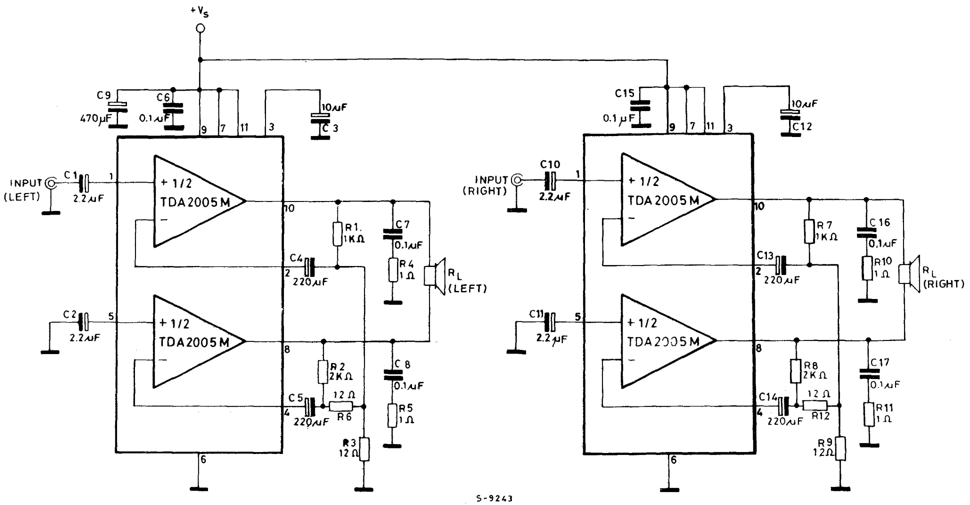
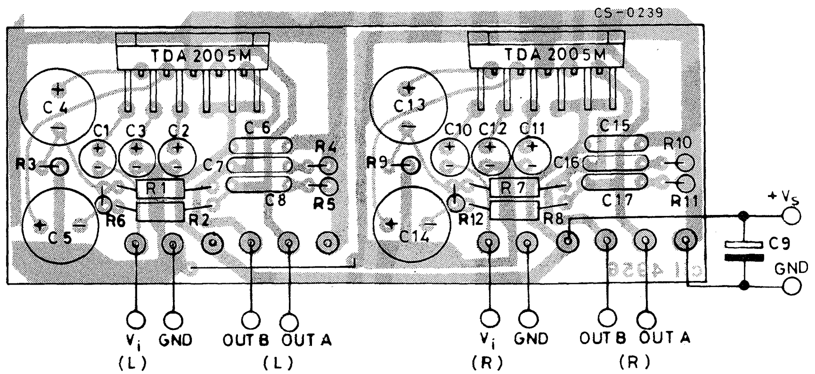


Fig. 26 - P.C. board and components layout of circuit of Fig. 25 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 27 - Low cost bridge amplifier (G_v = 42dB)

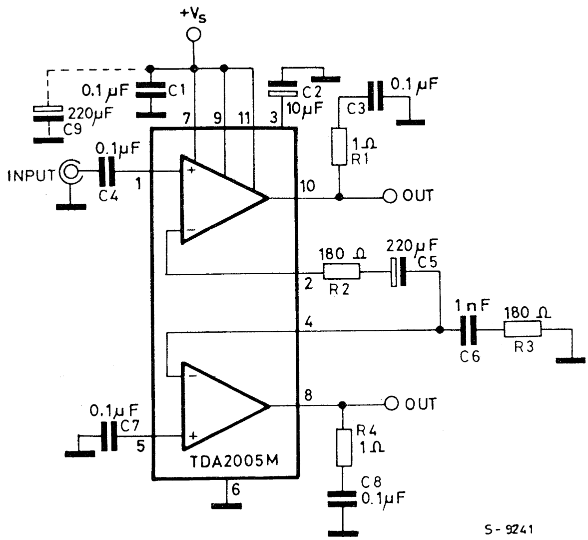
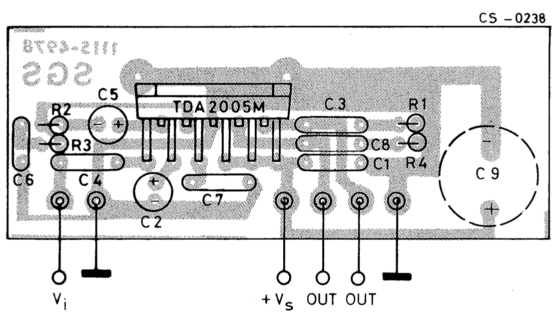


Fig. 28 - P.C. and component layout of the circuit of Fig. 27 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 29 - 10 + 10W stereo amplifier with tone balance and loudness control

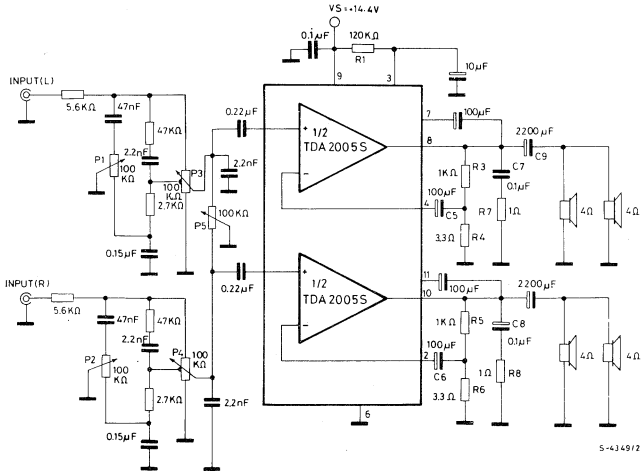


Fig. 30 - Tone control response (circuit of Fig. 29)

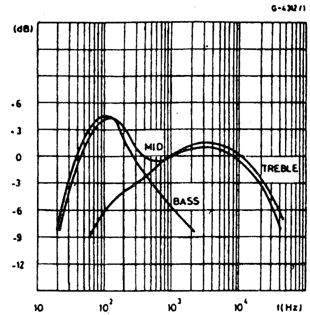


Fig. 31 - 20W Bus amplifier

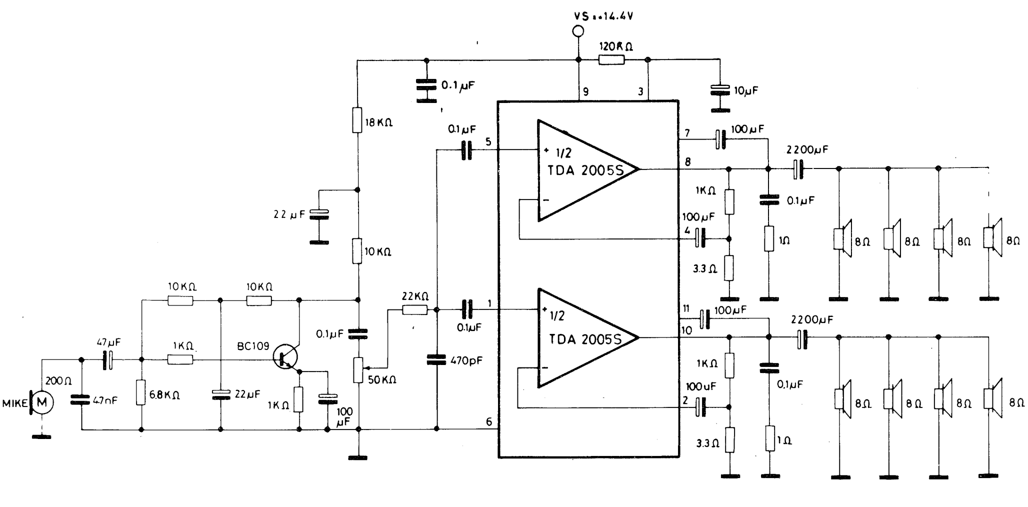


Fig. 32 - Simple 20W two way amplifier (F_c = 2KHz)

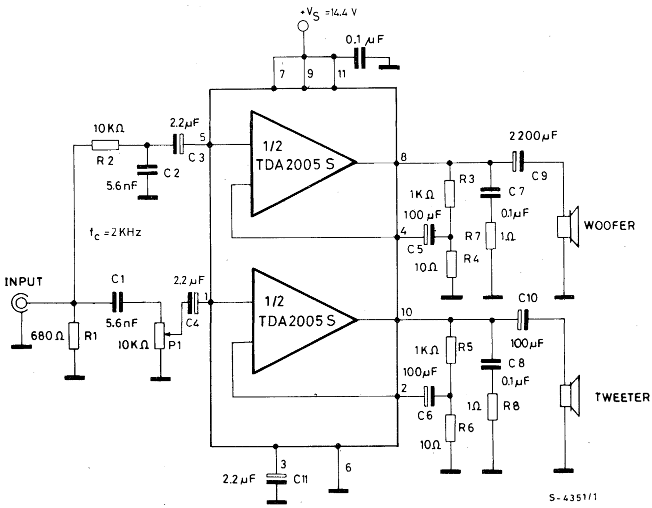
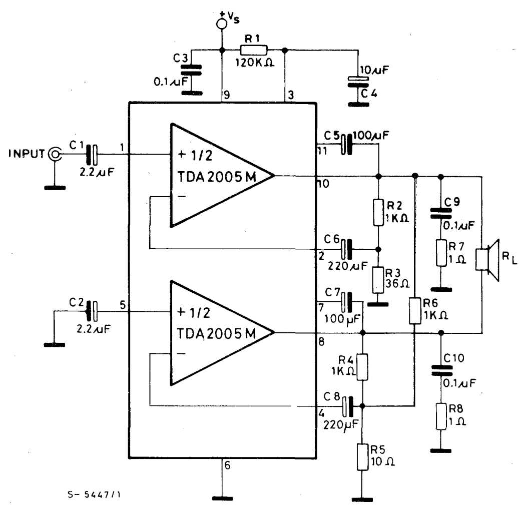
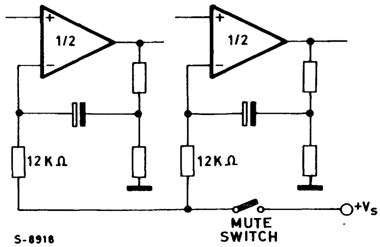


Fig. 33 - Bridge amplifier circuit suited for low-gain applications (G_V = 34dB)



APPLICATION INFORMATION (continued)

Fig. 34 - Example of muting circuit



BUILT-IN PROTECTION SYSTEMS

Load dump voltage surge

The TDA2005 has a circuit which enables it to withstand a voltage pulse train, on pin 9, of the type shown in Fig. 36.
If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held withing the limits shown.
A suggested LC network is shown in Fig. 35. With this network, a train of pulses with amplitude up to 120V and width of 2ms can be applied at point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 35

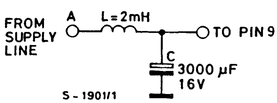
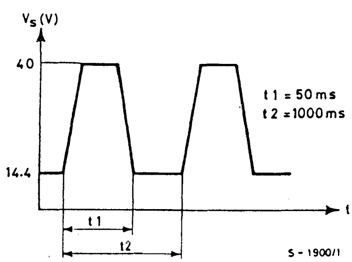


Fig. 36



Short circuit (AC and DC conditions)

The TDA2005 can withstand a permanent short-circuit on the output for a supply voltage up to 16V.

Polarity inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This feature is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA2005 protection diodes are included to avoid any damage.

Inductive load

A protection diode is provided to allow use of the TDA2005 with inductive loads.

DC voltage

The maximum operating DC voltage for the TDA2005 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

BUILT-IN PROTECTION SYSTEMS (continued)

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 37 shows the dissipable power as a function of ambient temperature for different thermal resistance.

Loudspeaker protection

The circuit offers loudspeaker protection during short circuit for one wire to ground.

Fig. 37 - Maximum allowable power dissipation vs. ambient temperature

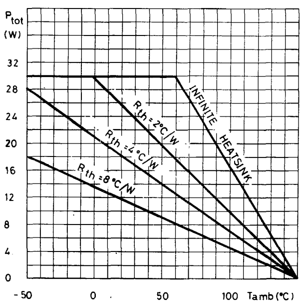


Fig. 38 - Output power and drain current vs. case temperature

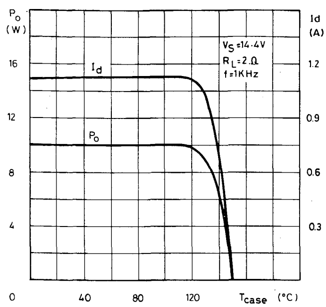
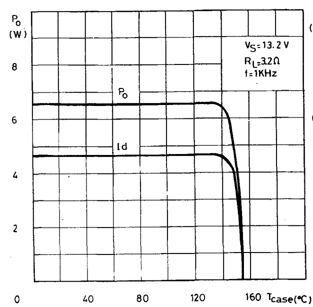


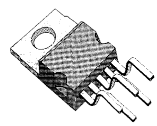
Fig. 39 - Output power and drain current vs. case temperature



TDA2006

12W AUDIO AMPLIFIER

The TDA2006 is a monolithic integrated circuit in Pentawatt package, intended for use as a low frequency class "AB" amplifier. At ± 12V, d = 10% typically it provides 12W output power on a 4Ω load and 8W on a 8Ω. The TDA2006 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shutdown system is also included. The TDA2006 is pin to pin equivalent to the TDA2030.



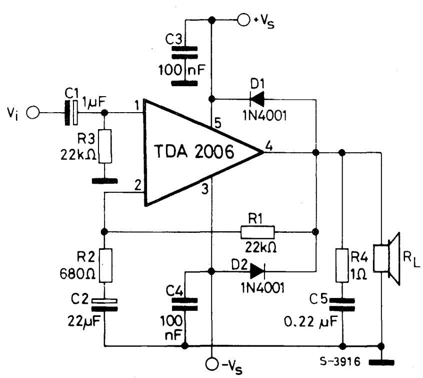
Pentawatt

ORDER CODE: TDA2006H
TDA2006V

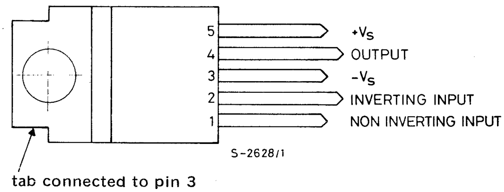
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 15	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 12	V
I_o	Output peak current (internally limited)	3	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

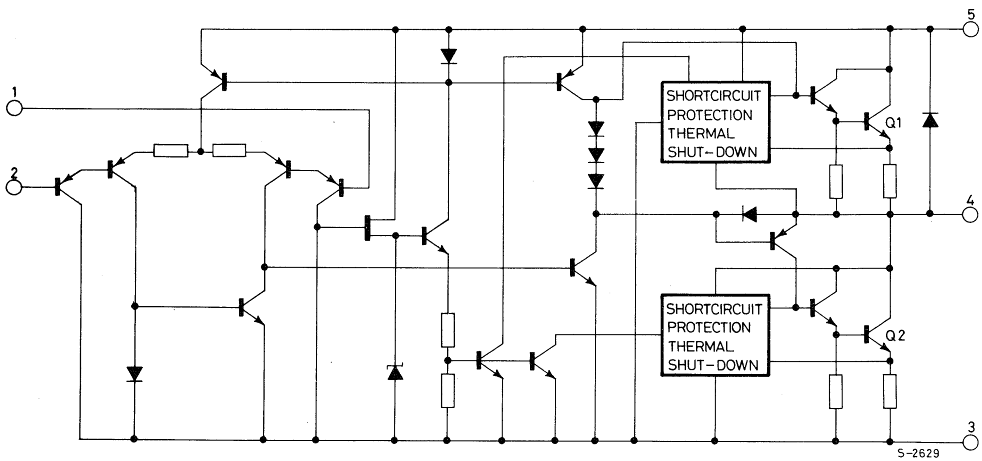
TEST AND APPLICATION CIRCUIT



CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\text{-}j\ case}$	Thermal resistance junction–case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; $V_s = \pm 12V$, $T_{amb} = 25°C$ unless otherwise specified)

	Paremeter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 6		± 15	V
I_d	Quiescent drain current	$V_s = \pm 15V$		40	80	mA
I_b	Input bias current			0.2	3	μA
V_{OS}	Input offset voltage			± 8		mV
I_{OS}	Input offset current			± 80		nA
V_{OS}	Output offset voltage			± 10	± 100	mV
P_o	Output power	d = 10% f = 1KHz R_L = 4Ω R_L = 8Ω	 6	 12 8		 W W
d	Distortion	P_o = 0.1 to 8W R_L = 4Ω f = 1KHz		0.2		%
		P_o = 0.1 to 4W R_L = 8Ω f = 1KHz		0.1	1	%
V_i	Input sensitivity	f = 1KHz P_o = 10W R_L = 4Ω P_o = 6W R_L = 8Ω		 200 220		 mV mV
B	Frequency response (-3dB)	P_o = 8W R_L = 4Ω	20 Hz to 100 KHz			
R_i	Input resistance (pin 1)	f = 1KHz	0.5	5		MΩ
G_v	Voltage gain (open loop)			75		dB
G_v	Voltage gain (closed loop)		29.5	30	30.5	dB
e_N	Input noise voltage	B (-3dB) = 22Hz to 22KHz R_L = 4Ω		3	10	μV
i_N	Input noise current			80	200	pA
SVR	Supply voltage rejection	R_L = 4Ω R_g = 22KΩ f_{ripple} = 100Hz (*)	40	50		dB
I_d	Drain current	P_o = 12W R_L = 4Ω P_o = 8W R_L = 8Ω		850 500		mA mA
T_j	Thermal shutdown junction temperature				145	°C

(*) Referring to Fig. 15, single supply.

Fig. 1 - Output power vs. supply voltage

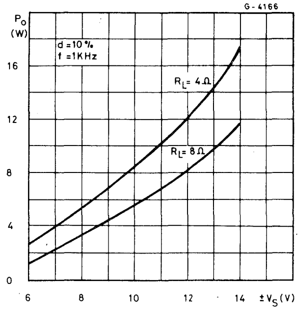


Fig. 2 - Distortion vs. output power

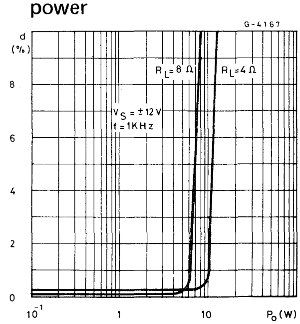


Fig. 3 - Distortion vs. frequency

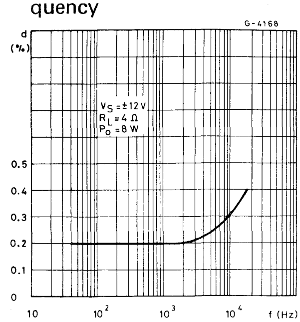


Fig. 4 - Distortion vs. frequency

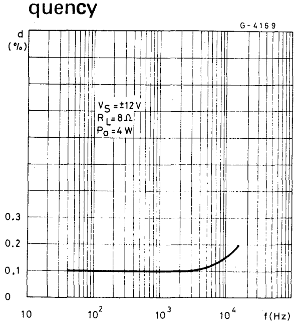


Fig. 5 - Sensitivity vs. output power

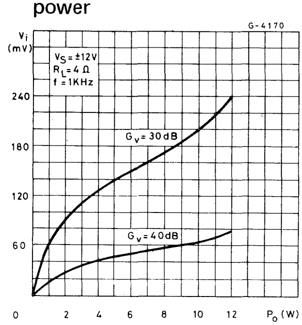


Fig. 6 - Sensitivity vs. output power

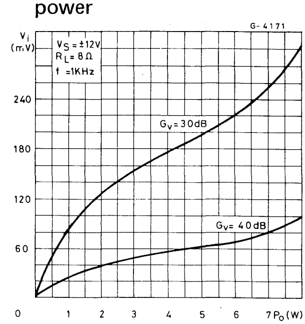


Fig. 7 - Frequency response with different values of the rolloff capacitor C_8 (see fig. 13)

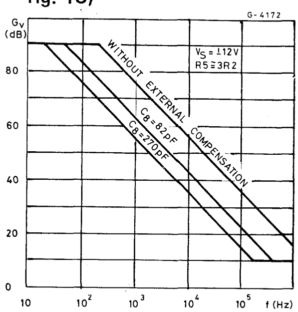


Fig. 8 - Value of C_8 vs. voltage gain for different bandwidths (see fig. 13)

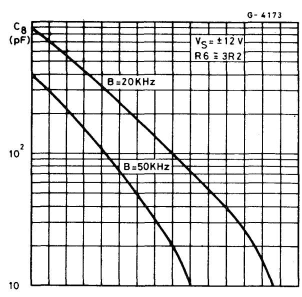
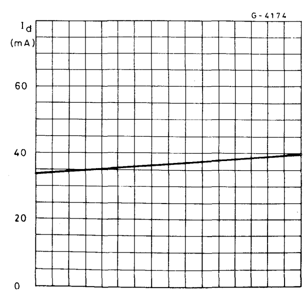


Fig. 9 - Quiescent current vs. supply voltage



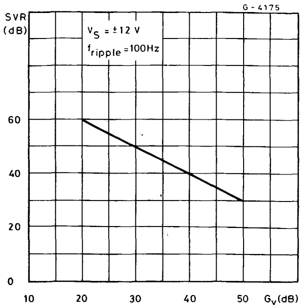


Fig. 10 - Supply voltage rejection vs. voltage gain

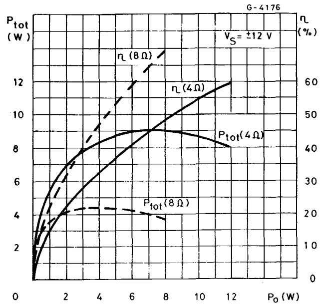


Fig. 11 - Power dissipation and efficiency vs. output power

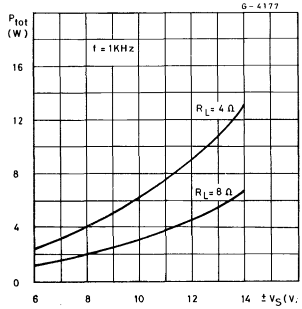


Fig. 12 - Maximum power dissipation vs. supply voltage (sine wave operation)

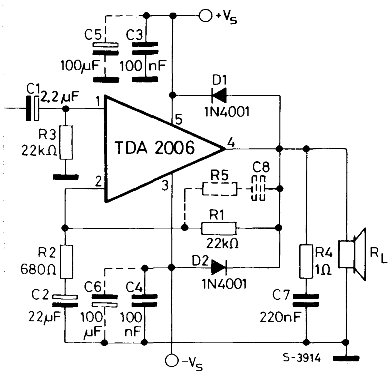


Fig. 13 - Application circuit with split power supply

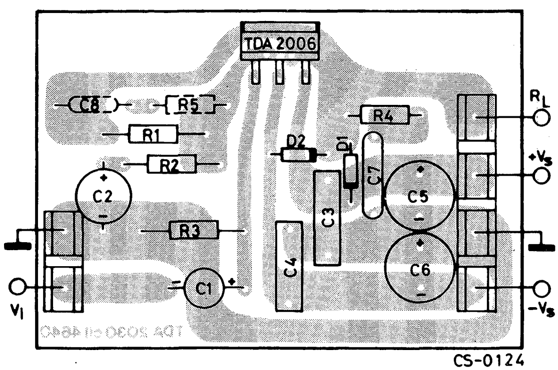


Fig. 14 - P.C. board and component layout for the circuit of fig. 13

Fig. 15 - Application circuit with single power supply

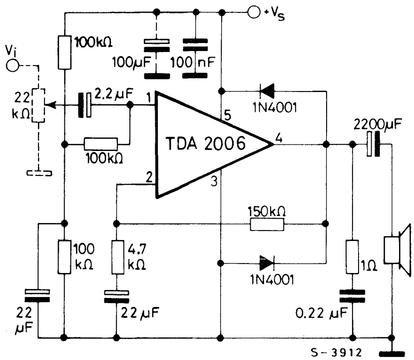


Fig. 16 - P.C. board and component layout for the circuit of fig. 15

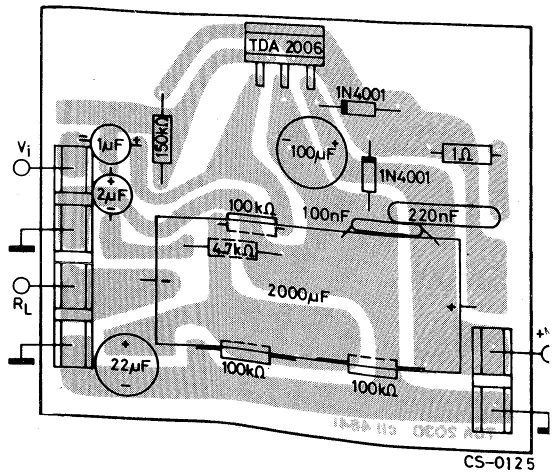
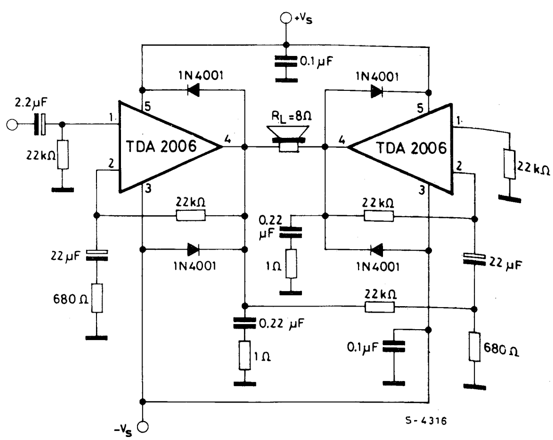


Fig. 17 - Bridge amplifier configuration with split power supply (Po = 24W, $V_s = \pm$ 12V)



PRACTICAL CONSIDERATION

Printed circuit board

The layout shown in Fig. 14 should be adopted by the designers. If different layout are used, the ground points of input 1 and input 2 must be well decoupled from ground of the output on which a rather high current flows.

Assembly suggestion

No electrical isolation is needed between the package and the heat-sink with single supply voltage configuration.

Application suggestion

The recommended values of the components are the ones shown on application circuits of Fig. 13. Different values can be used. The following table can help the designers.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R_1	22 KΩ	Closed loop gain setting	Increase of gain	Decrease of gain (*)
R_2	680Ω	Closed loop gain setting	Decrease of gain (*)	Increase pf gain
R_3	22 KΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R_4	1Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_5	$3\,R_2$	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C_1	2.2 μF	Input DC decoupling		Increase of low freqencies cut off
C_2	22 μF	Inverting input DC decoupling		Increase of low frequencies cutoff
C_3C_4	0.1 μF	Supply voltage by pass		Danger of oscillation
C_5C_6	100 μF	Supply voltage by pass		Danger of oscillation
C_7	0.22 μF	Frequency stability		Danger of oscillation
C_8	$\frac{1}{2\pi B R_1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
D_1D_2	1N4001	To protect the device against output voltage spikes.		

(*) Closed loop gain must be higher than 24dB

SHORT CIRCUIT PROTECTION

The TDA2006 has an original circuit which limits the current of the output transistors. Fig. 18 shows that the maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area (Fig. 19).

This function can therefore be considered as being peak power limiting rather than simple current limiting.
It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

Fig. 18 - Maximum output current vs. voltage $V_{Ce(sat)}$ across each output transistor

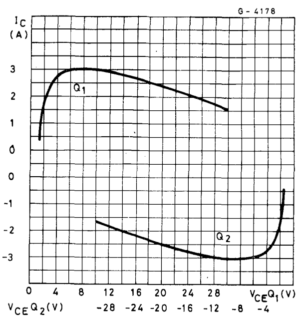
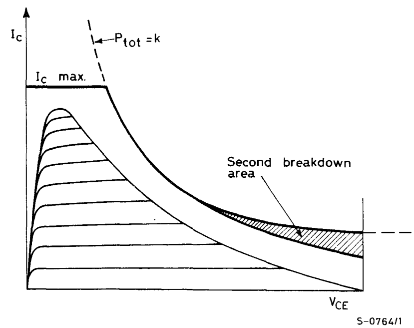


Fig. 19 - Safe operating area and collector characteristics of the protected power transistor



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increases up to 150°C, the thermal shutdown simply reduces the power dissipation and the current consumption.

Fig. 20 - Output power and drain current vs. case temperature ($R_L = 4\Omega$)

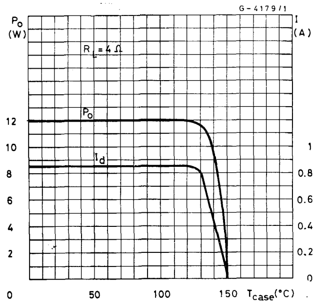
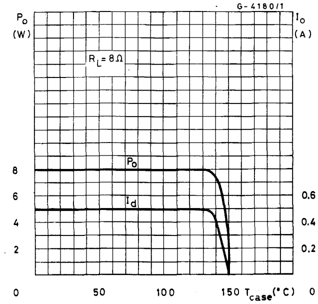


Fig. 21 - Output power and drain current vs. case temperature ($R_L = 8\Omega$)



The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 22 shows the dissipable power as a function of ambient temperature for different thermal resistances.

Fig. 22 - Maximum allowable power dissipation vs. ambient temperature

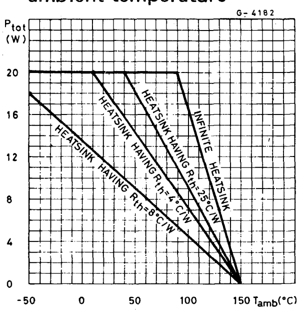
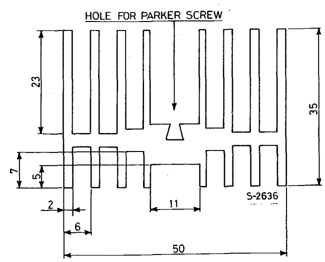


Fig. 23 - Example of heatsink



Dimension suggestion

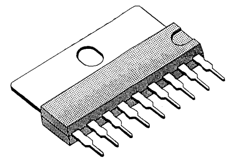
The following table shows the lenght of the heatsink in fig. 23 for several values of P_{tot} and R_{th}.

P_{tot} (W)	12	8	6
Lenght of heatsink (mm)	60	40	30
R_{th} of heatsink (°C/W)	4.2	6.2	8.3

6+6W STEREO AMPLIFIER

The TDA 2007 is a class AB dual Audio power amplifier assembled in single in line 9 pins package, specially designed for stereo application in music centers TV receivers and portable radios. Its main features are:

- High output power
- High current capability
- Thermal overload protection
- Space and cost saving: very low number of external components and simple mounting thanks to the SIP. 9 package.



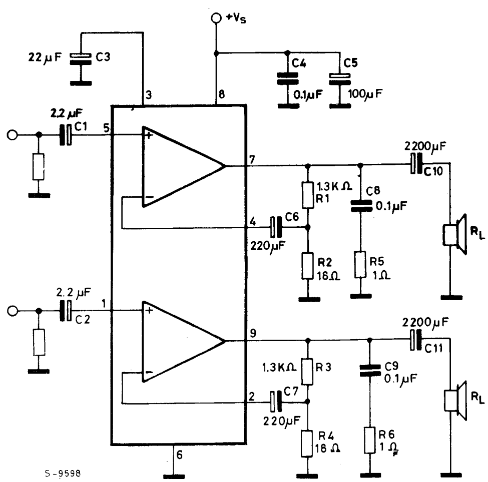
SIP. 9

ORDERING NUMBER: TDA 2007

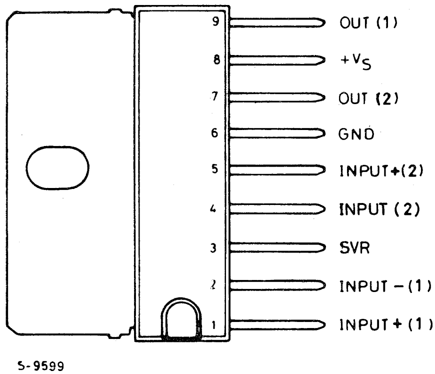
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
I_o	Output peak current (repetitive f ⩾ 20 Hz)	3	A
I_o	Output peak current (non repetitive, t = 100 μs)	3.5	A
P_{tot}	Power dissipation at T_{case} = 70°C	10	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

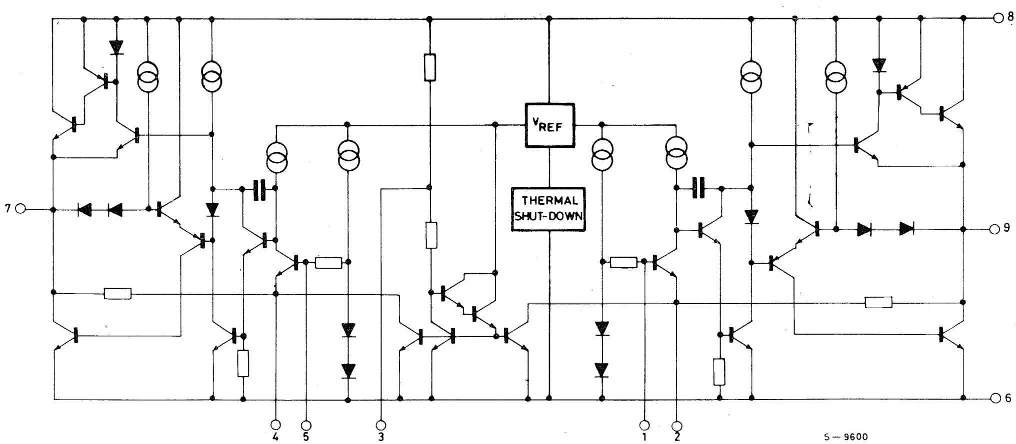
STEREO TEST CIRCUIT



CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	8	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the **stereo** application circuit, T_{amb} = 25°C, V_s = 18V, G_v = 36 dB, unless otherwise specified)

Parameters		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			8		26	V
V_o	Quiescent output voltage				8.5		V
I_d	Total quiescent drain current				48	90	mA
P_o	Output power (each channel)	f = 100 Hz to 16 KHz d = 0.5% V_s = 18V R_L = 4Ω V_s = 22V R_L = 8Ω		 5.5 5.5	 6 6		 W W
d	Distortion (each channel)	f = 1 KHz, V_s = 18V, R_L = 4Ω P_o = 100 mW to 3W			0.1		%
		f = 1 KHz, V_s = 22V, R_L = 8Ω P_o = 100 mW to 3W			0.05		%
CT	Cross talk (°°°)	R_L = ∞	f = 1 KHz	50	60		dB
		R_g = 10 KΩ	f = 10 KHz	40	50		dB
V_i	Input saturation voltage (rms)			300			mV
R_i	Input resistance	f = 1 KHz		70	200		KΩ
f_L	Low frequency roll off (-3 dB)	R_L = 4Ω, C10 = C11= 2200 μF			40		Hz
f_H	High frequency roll off (-3 dB)				80		KHz
G_v	Voltage gain (closed loop)	f = 1 KHz		35.5	36	36.5	dB
ΔG_v	Closed loop gain matching				0.5		dB
e_N	Total input noise voltage	R_g = 10 KΩ (°)			1.5		μV
		R_g = 10 KΩ (°°)			2.5	8	μV
SVR	Supply voltage rejection (each channel)	R_g = 10 KΩ f_{ripple}= 100 Hz V_{ripple}= 0.5V		43	55		dB
T_J	Thermal shut-down junction temperature				145		°C

(°) Curve A. (°°) 22 Hz to 22 KHz. (°°°) Optimized test box.

Fig. 1 - Stereo test circuit (G_v = 36 dB)

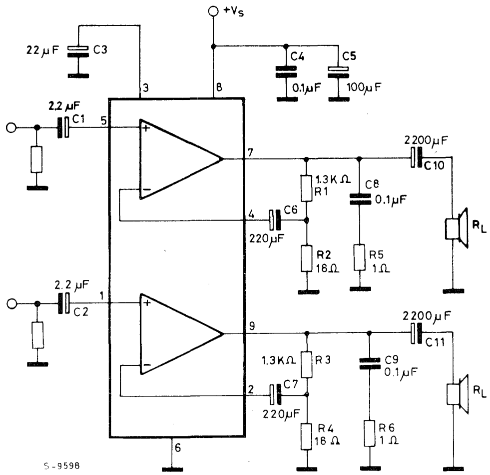


Fig. 2 - P.C. board and components layout of the circuit of fig. 1 (1 : 1 scale)

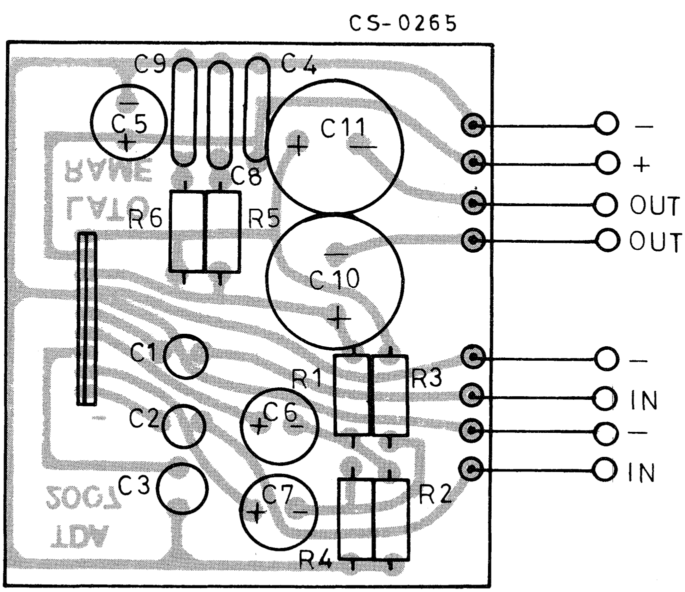


Fig. 3 - Output power vs. supply voltage (d = 0.5%)

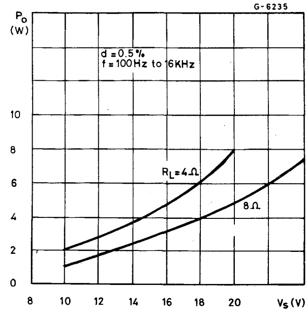


Fig. 4 - Output power vs. supply voltage (d = 10%)

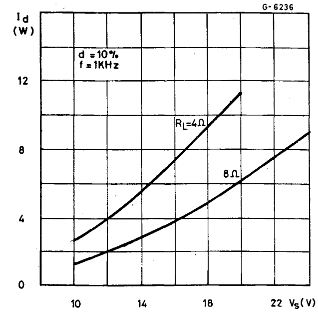


Fig. 5 - Quiescent current vs. supply voltage

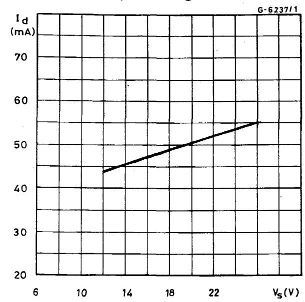


Fig. 6 - Supply voltage rejection vs. value of capacitor C3

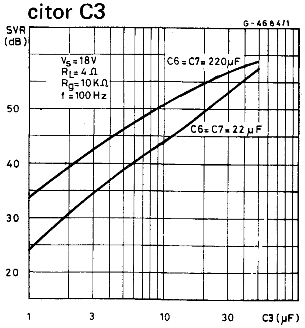


Fig. 7 - Supply voltage rejection vs. frequency

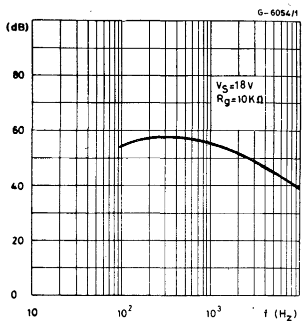


Fig. 8 - Total power dissipation vs. output power

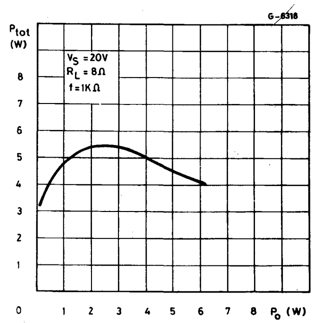


Fig. 9 - Cross-talk vs. frequency

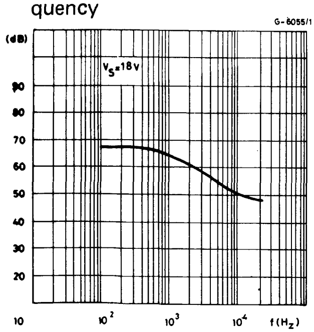


Fig. 10 - Simple short-circuit protection

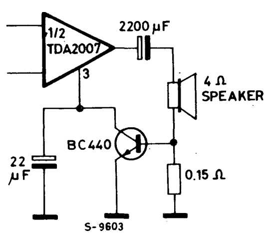
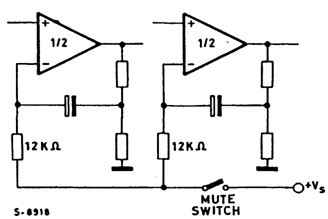
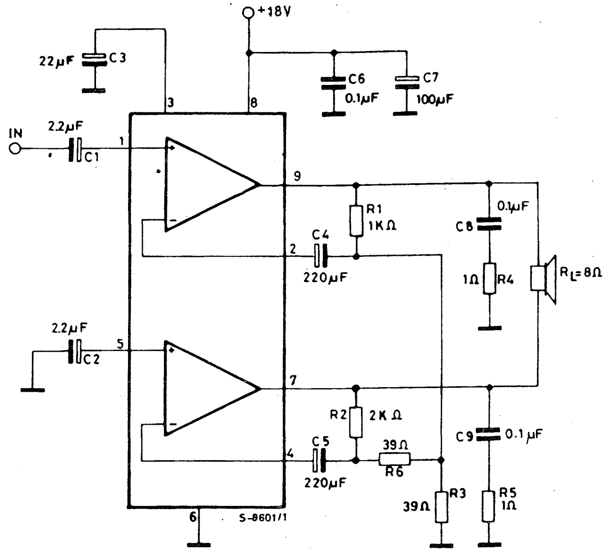


Fig. 11 - Example of muting circuit



APPLICATION INFORMATION

Fig. 12 - 12W bridge amplifier (d = 0,5%, G_v = 40dB)



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 1. Different values can be used; the following table can help the designer.

Component	Recomm. value	Purpose	Larger than	Smaller than
R1 and R3	1.3 KΩ	Close loop gain setting(*)	Increase of gain	Decrease of gain
R2 and R4	18 Ω		Decrease of gain	Increase of gain
R5 and R6	1 Ω	Frequency stability	Danger of oscillation at high frequency with inductive load	
C1 and C2	2.2 μF	Input DC decoupling	High turn-on delay	High turn-on pop Higher low frequency cutoff. Increase of noise
C3	22 μF	Ripple rejection	Better SVR. Increase of the switch-on time	Degradation of SVR.
C6 and C7	220 μF	Feedback Input DC decoupling		
C8 and C9	0.1 μF	Frequency stability		Danger of oscillation
C10 and C11	1000 μF to 2200 μF	Output DC decoupling		Higher low-frequency cut-off

(*) The closed loop gain must be higher than 26 dB.

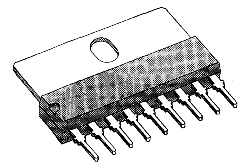
SGS-THOMSON MICROELECTRONICS

TDA2007A

6 + 6W SHORT-CIRCUIT PROTECTED STEREO AMPLIFIER

ADVANCE DATA

- HIGH OUTPUT POWER
- HIGH CURRENT CAPABILITY
- AC SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION



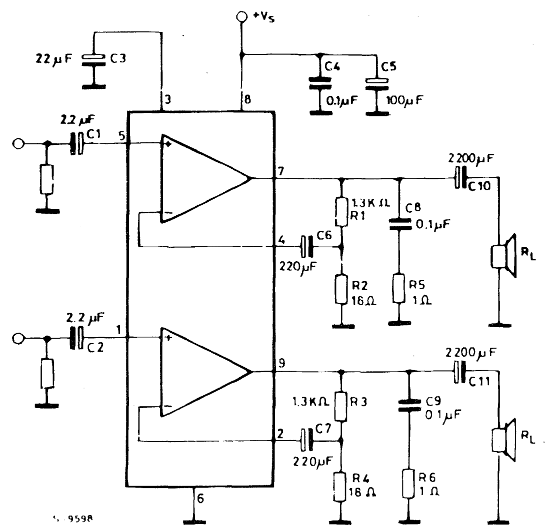
SIP. 9

ORDERING NUMBER : TDA2007A

DESCRIPTION

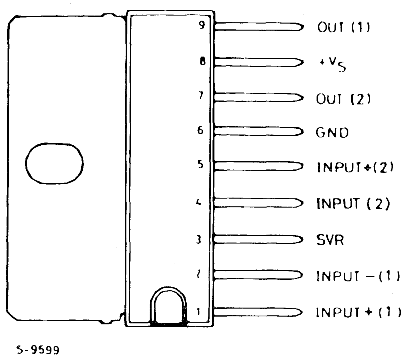
The TDA2007A is a class AB dual Audio power amplifier assembled in single in line 9 pins package, specially designed for stereo application in music centers TV receivers and portable radios.

STEREO TEST CIRCUIT

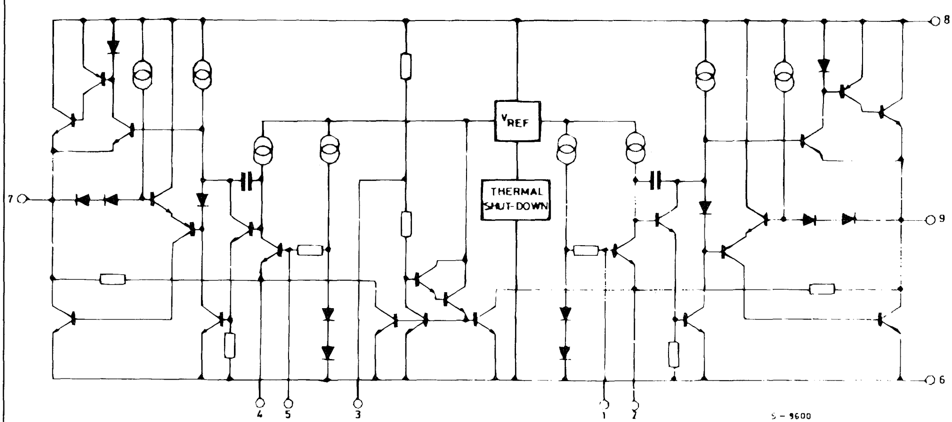


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	8	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	28	V
I_o	Output Peak Current (repetitive f ≥ 20 Hz)	3	A
I_o	Output Peak Current (non repetitive t = 100 μs)	3.5	A
P_{tot}	Power Dissipation at T_{case} = 70 °C	10	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

ELECTRICAL CHARACTERISTICS (refer to the stereo application circuit, T_{amb} = 25 °C, V_s = 18 V, G_v = 36 dB, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		8		26	V
V_o	Quiescent Output Volt.			8.5		V
I_d	Total Quiescent Drain Current			50	90	mA
P_o	Output Power (each channel)	f = 100 Hz to 16 kHz d = 0.5 % V_s = 18 V R_L = 4 Ω V_s = 22 V R_L = 8 Ω	 5.5 5.5	 6 6		 W W
d	Distortion (each channel)	f = 1 kHz, V_s = 18 V, R_L = 4 Ω P_o = 100 mW to 3 W		0.1		%
		f = 1 kHz, V_s = 22 V, R_L = 8 Ω P_o = 100 mW to 3 W		0.05		%
CT	Cross Talk (°°°)	R_L = ∞, R_g = 10 kΩ; f = 1 kHz	50	60		dB
		R_L = ∞, R_g = 10 kΩ; f = 10 kHz	40	50		dB
V_i	Input Sat. Volt. (rms)		300			mV
R_i	Input Resistance	f = 1 kHz	70	200		kΩ
f_L	Low Frequency Roll Off (– 3 dB)	R_L = 4 Ω, C10 = C11 = 2200 μF)		40		Hz
f_H	High Frequency Roll Off (– 3 dB)	R_L = 4 Ω, C10 = C11 = 2200 μF)		80		kHz
G_v	Voltage Gain (closed loop)	f = 1 kHz	35.5	36	36.5	dB
Δ G_v	Closed Loop Gain Matching			0.5		dB
e_N	Total Input Noise Voltage	R_g = 10 kΩ (°)		1.5		μV
		R_g = 10 kΩ (°°)		2.5	8	μV
SVR	Supply Voltage Rejection (each channel)	R_g = 10 kΩ f_{ripple} = 100 Hz V_{ripple} = 0.5 V		55		dB
T_j	Thermal Shut-down Junction Temperature			145		°C

(°) Curve A. (°°) 22Hz to 22KHz.

Figure 1 : Stereo Test Circuit (G_V = 36 dB).

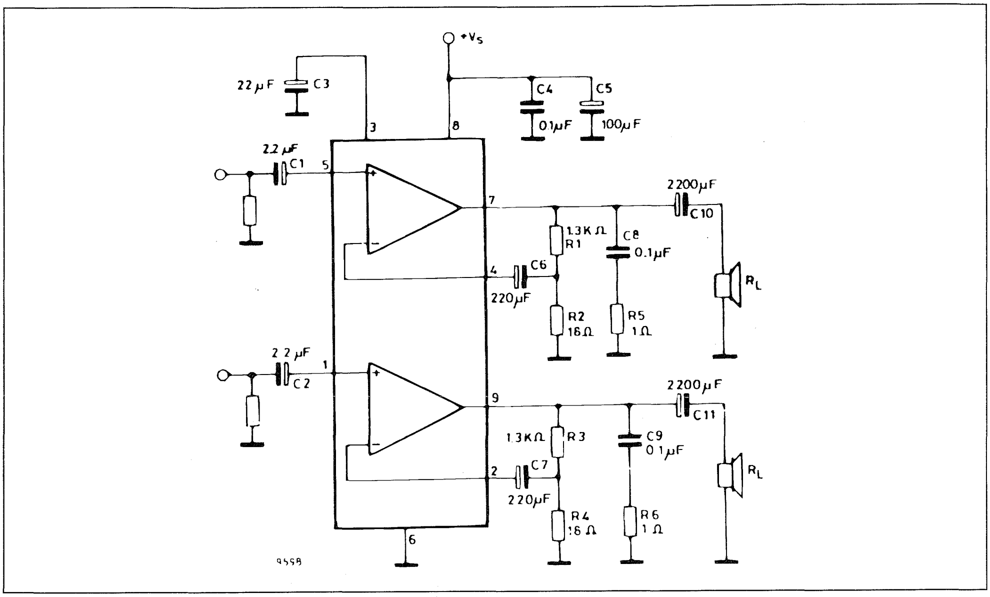
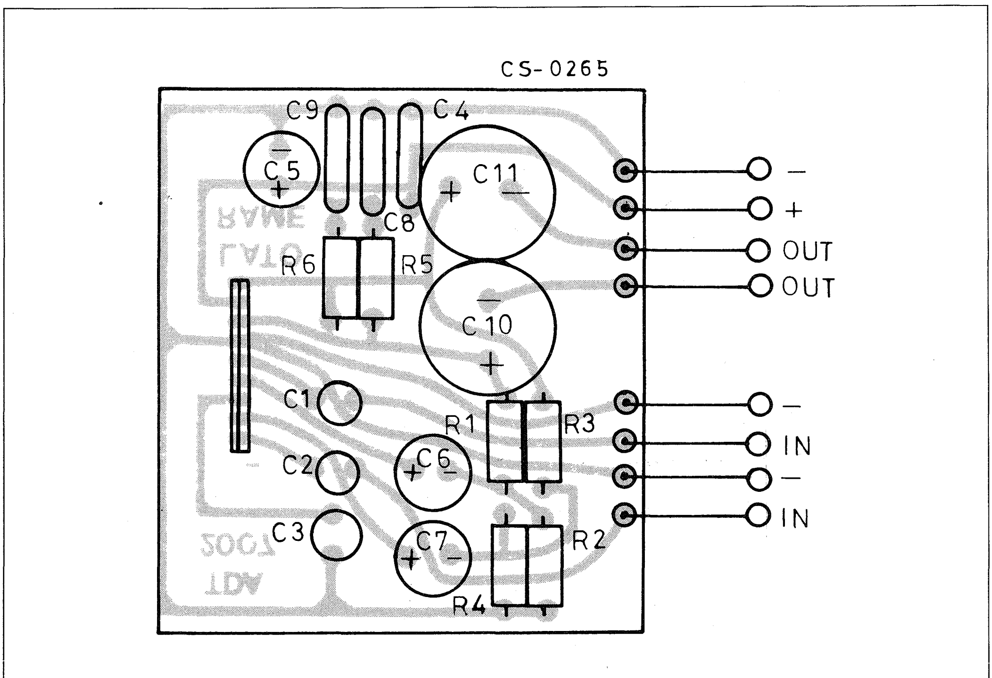


Figure 2 : P.C. Board and Components layout of the Circuit of Fig.1 (1 : 1 scale).



APPLICATION SUGGESTION

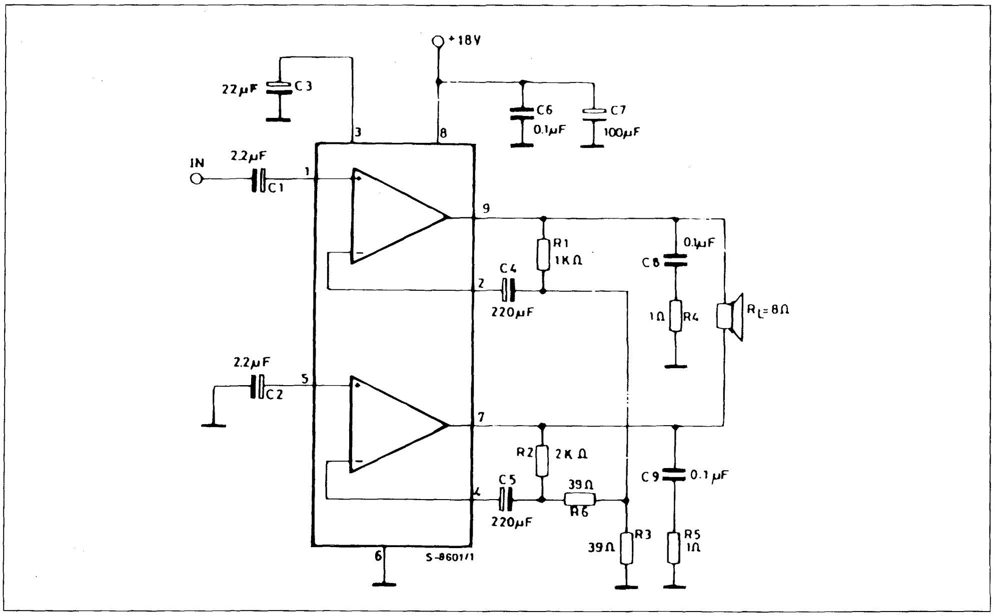
The recommended values of the components are those shown on application circuit of fig.1. Different values can be used ; the following table can help the designer.

Component	Recommanded Value	Purpose	Larger Than	Smaller Than
R1, R3	1.3 kΩ	Close Loop Gain Setting (*)	Increase of Gain	Decrease of Gain
R2 and R4	18 Ω		Decrease of Gain	Increase of Gain
R5 and R6	1 Ω	Frequency Stability	Danger of Oscillation at High Frequency with Inductive Load	
C1 and C2	2.2 µF	Input DC Decoupling	High Turn-on Delay	High Turn-on Pop Higher Low Frequency Cutoff. Increase of Noise
C3	22 µF	Ripple Rejection	Better SVR Increase of the Switch-on Time	Degradation of SVR
C6 and C7	220 µF	Feedback Input DC Decoupling		
C8 and C9	0.1 µF	Frequency Stability		Danger of Oscillation
C10 and C11	1000 µF to 2200 µF	Output DC Decoupling		Higher Low-frequency Cut-off

(*) The closed loop gain must be higher than 26 dB.

APPLICATION INFORMATION

Figure 3 : 12 W Bridge Amplifier (d = 0.5%, G_V = 40 dB).



SGS-THOMSON MICROELECTRONICS

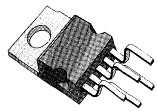
TDA2008

12W AUDIO AMPLIFIER (V_S=22V, R_L=4Ω)

The TDA2008 is a monolithic class B audio power amplifier in Pentawatt® package designed for driving low impedance loads (down to 3.2Ω). The device provides a high output current capability (up to 3A), very low harmonic and crossover distortion.

In addition, the device offers the following features:

- very low number of external components;
- assembly ease, due to Pentawatt® power package with no electrical insulation requirements;
- space and cost saving;
- high reliability;
- flexibility in use;
- thermal protection.



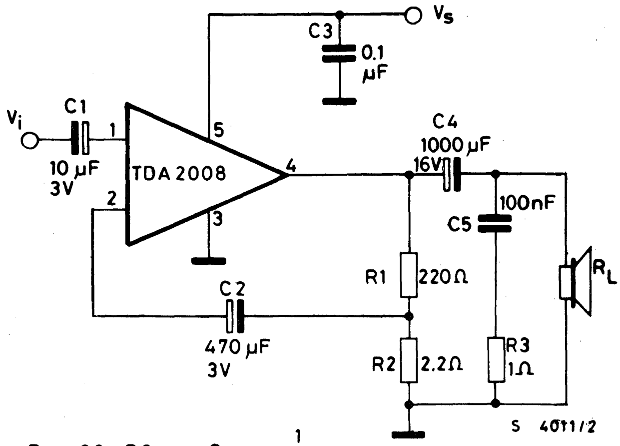
Pentawatt

ORDERING NUMBER: TDA2008V

ABSOLUTE MAXIMUM RATINGS

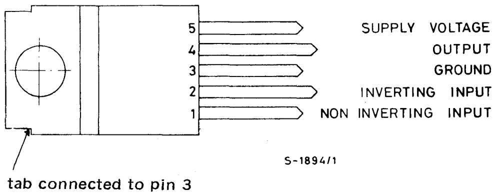
V_s	DC supply voltage	28	V
I_o	Output peak current (repetitive)	3	A
I_o	Output peak current (non repetitive)	4	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TYPICAL APPLICATION CIRCUIT

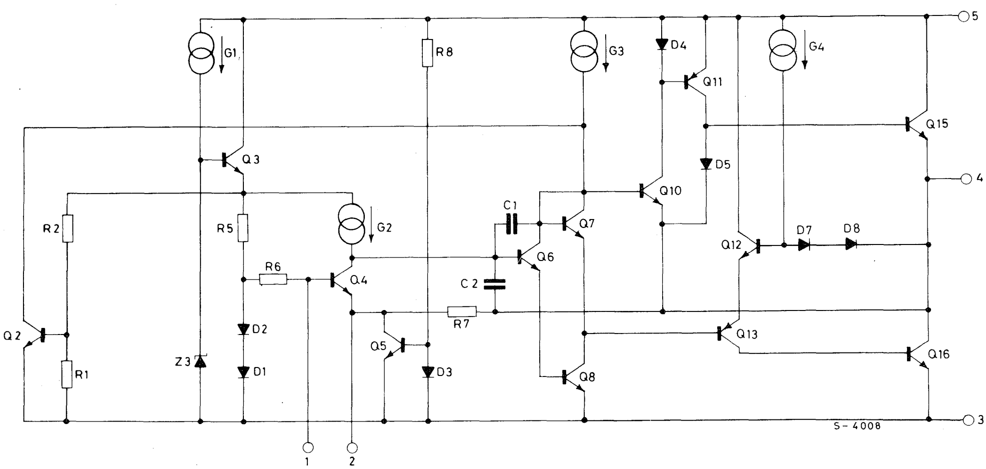


$$R_x = 20 \cdot R2 \quad ; \quad C_x = \frac{1}{2\pi B R1}$$

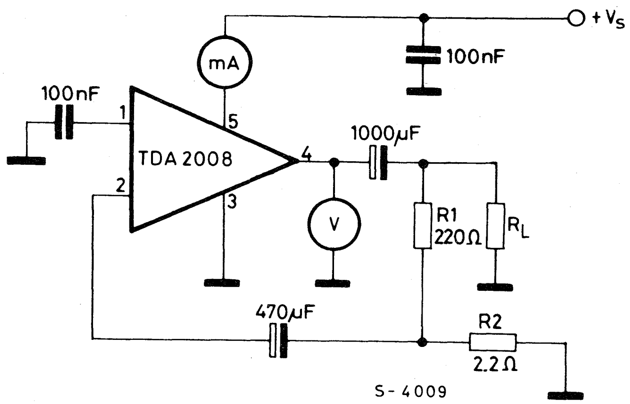
CONNECTION DIAGRAM (top view)



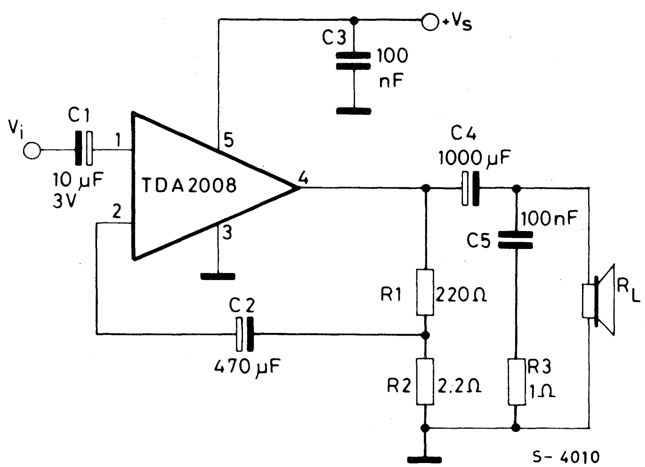
SCHEMATIC DIAGRAM



DC TEST CIRCUIT



AC TEST CIRCUIT



THERMAL DATA

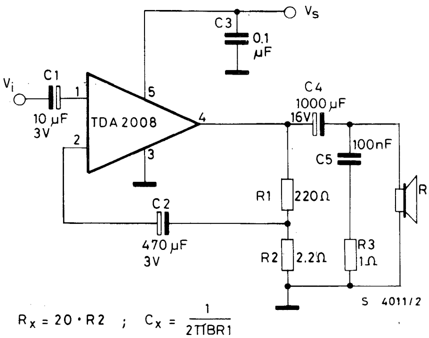
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s = 22V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			10		28	V
V_o	Quiescent output voltage (pin 4)				10.5		V
I_d	Quiescent drain current (pin 5)				65	115	mA
P_o	Output power	d = 10%	R_L = 8Ω		8		W
		f = 1 KHz	R_L = 4Ω	10	12		W
V_i (RMS)	Input saturation voltage			300			mV
V_i	Input sensitivity	f = 1 KHz P_o = 0.5W P_o = 8W P_o = 0.5W P_o = 12W	 R_L = 8Ω R_L = 8Ω R_L = 4Ω R_L = 4Ω		 20 80 14 70		 mV mV mV mV
B	Frequency response (-3 dB)	P_o = 1W R_L = 4Ω		40 to 15 000			Hz
d	Distortion	f = 1 KHz P_o = 0.05 to 4W R_L = 8Ω P_o = 0.05 to 6W R_L = 4Ω			 0.12 0.12	 1 1	 % %
R_i	Input resistance (pin 1)	f = 1 KHz		70	150		KΩ
G_v	Voltage gain (open loop)	f = 1 KHz	R_L = 8Ω		80		dB
G_v	Voltage gain (closed loop)	f = 1 KHz	R_L = 8Ω	39.5	40	40.5	dB
e_N	Input noise voltage	BW= 22Hz to 22 KHz			1	5	μV
i_N	Input noise current	BW= 22Hz to 22 KHz			60	200	pA
SVR	Supply voltage rejection	V_{ripple} = 0.5V R_g = 10KΩ R_L = 4Ω	f = 100 Hz	30	36		dB

APPLICATION INFORMATION

Fig. 1 - Typical application circuit



$R_x = 20 \cdot R2$; $C_x = \frac{1}{2\pi BR1}$

Fig. 2 - P.C. board and component layout for the circuit of fig. 1 (1:1 scale)

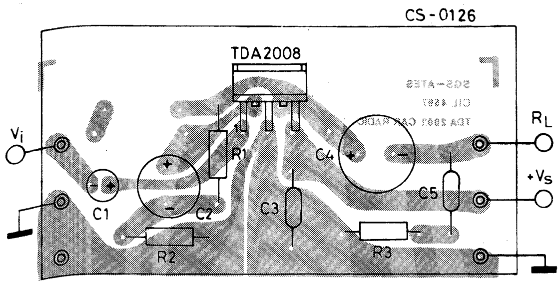


Fig. 3 - 25W bridge configuration application circuit (°)

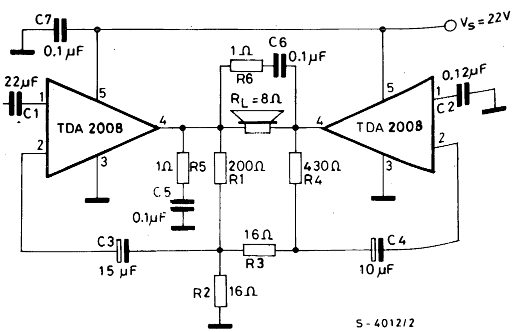
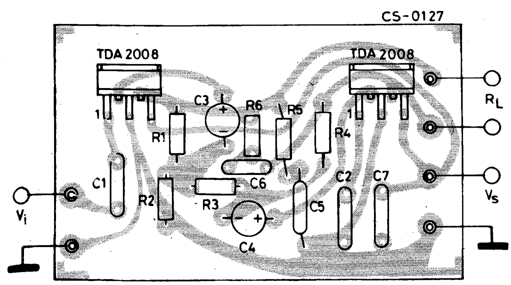


Fig. 4 - P.C. board and component layout for the circuit of fig. 3 (1:1 scale)



(°) The value of the capacitors C3 and C4 are different to optimize the SVR (Typ. = 40 dB)

Fig. 5 - Quiescent current vs. supply voltage

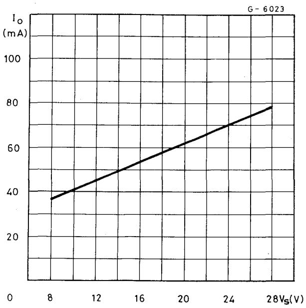


Fig. 6 - Output voltage vs. supply voltage

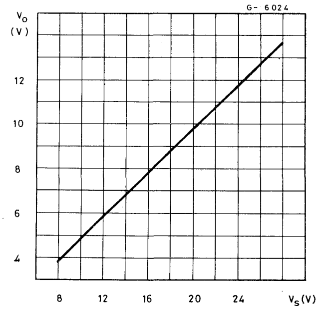


Fig. 7 - Output power vs. supply voltage

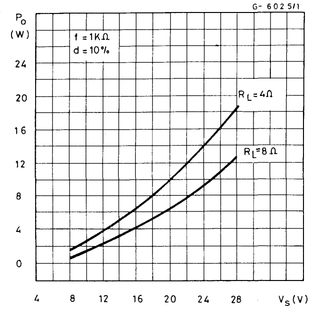


Fig. 8 - Distortion vs. frequency

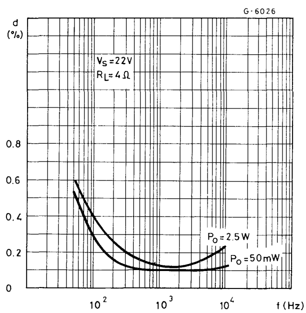


Fig. 9 - Supply voltage rejection vs. frequency

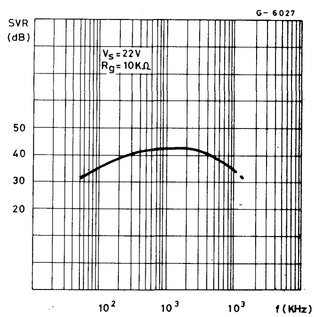
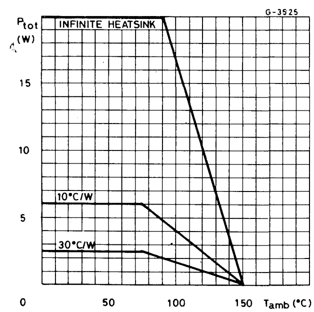


Fig. 10 - Maximum allowable power dissipation vs. ambient temperature



PRACTICAL CONSIDERATIONS

Printed circuit board

The layout shown in Fig. 2 is recommended. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground of the output through which a rather high current flows.

Assembly suggestion

No electrical insulation is needed between the package and the heat-sink. Pin length should be as short as possible. The soldering temperature must not exceed 260°C for 12 seconds.

Application suggestions

The recommended component values are those shown in the application circuits of Fig. 1. Different values can be used. The following table is intended to aid the car-radio designer.

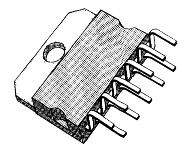
Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
C1	2.2μF	Input DC decoupling.		Noise at switch-on, switch-off.
C2	470μF	Ripple rejection.		Degradation of SVR.
C3	0.1μF	Supply bypassing.		Danger of oscillation.
C4	1000μF	Output coupling.		Higher low frequency cutoff.
C5	0.1μF	Frequency stability.		Danger of oscillation at high frequencies with inductive loads.
R1	$(G_V - 1) \cdot R2$	Setting of gain. (*)		Increase of drain current.
R2	2.2Ω	Setting of gain and SVR.	Degradation of SVR.	
R3	1Ω	Frequency stability.	Danger of oscillation at high frequencies with inductive loads.	

(*) The closed loop gain must be higher than 26dB.

10+10W HIGH QUALITY STEREO AMPLIFIER

The TDA2009 is class AB dual Hi-Fi Audio power amplifier assembled in Multiwatt® package, specially designed for high quality stereo application as Hi-Fi and music centers. Its main features are:

- High output power (10 + 10W min. @ d = 0.5%)
- High current capability (up to 3.5A)
- Thermal overload protection
- Space and cost saving: very low number of external components and simple mounting thanks to the Multiwatt® package.



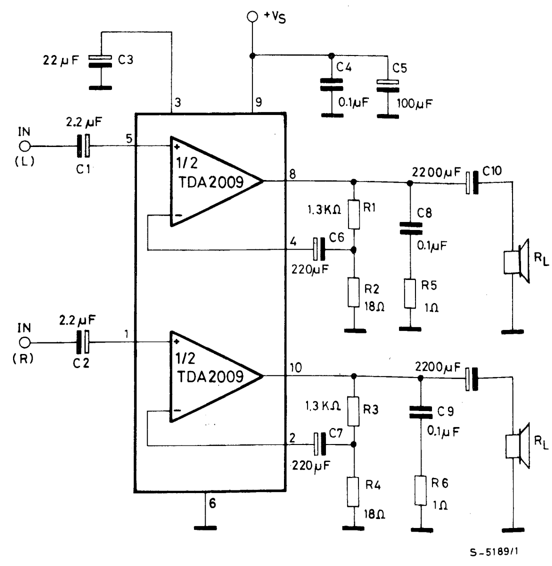
Multiwatt-11

ORDERING NUMBER: TDA2009

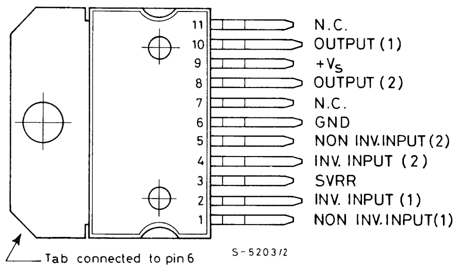
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
I_o	Output peak current (repetitive f ≥ 20Hz)	3.5	A
I_o	Output peak current (non repetitive, t = 100μs)	4.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

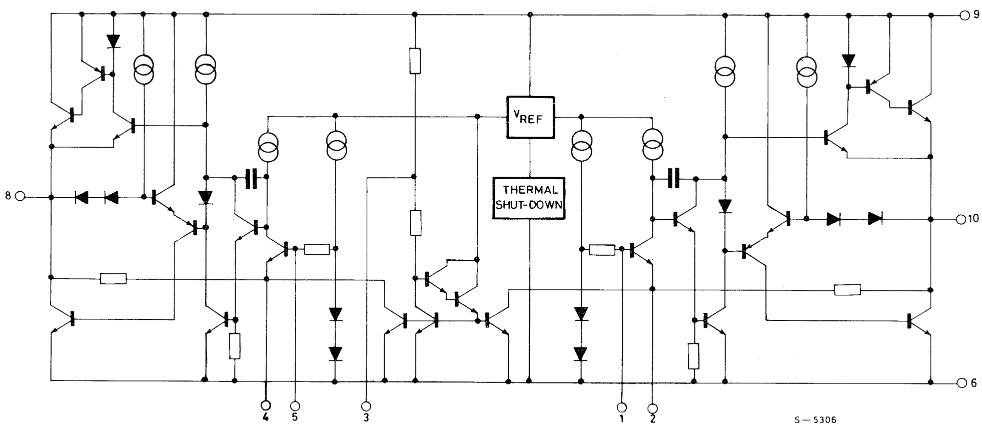
TEST CIRCUIT



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the **stereo** application circuit, T_{amb} = 25°C, V_s = 23V, G_v = 36 dB, unless otherwise specified)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		28	V
V_o	Quiescent output voltage	V_s = 23V		11		V
I_d	Total quiescent drain current	V_s = 28		55	120	mA
P_o	Output power	f = 50 Hz to 16 KHz d = 0.5% V_s = 23V R_L = 4 Ω R_L = 8 Ω V_s = 18V R_L = 4 Ω R_L = 8 Ω	 10 5.5 	 11 6.5 6.5 4		 W W W W
d	Distortion	f = 1 KHz V_s = 23V R_L = 4 Ω P_o = 100 mW to 8W V_s = 23V R_L = 8 Ω P_o = 100 mW to 3W		0.05 0.05		%
CT	Cross talk (°°°)	R_L = ∞ f = 1 KHz	50	65		dB
		R_g = 10 KΩ f = 10 KHz	40	50		dB
V_i	Input saturation voltage (rms)		300			mV
R_i	Input resistance	f = 1 KHz non inverting input	70	200		KΩ
f_L	Low frequency roll off (–3 dB)	R_L = 4Ω		20		Hz
f_H	High frequency roll off (–3 dB)	R_L = 4Ω		80		KHz
G_v	Voltage gain (closed loop)	f = 1 KHz	35.5	36	36.5	dB
ΔG_v	Closed loop gain matching			0.5		dB
e_N	Total input noise voltage	R_g = 10 KΩ (°)		1.5		μV
		R_g = 10 KΩ (°°)		2.5	8	μV
SVR	Supply voltage rejection	R_g = 10 KΩ f_{ripple} = 100 Hz V_{ripple} = 0.5V	43	55		dB
T_J	Thermal shut–down junction temperature			145		°C

(°) Curve A. (°°) 22 Hz to 22 KHz. (°°°) Optimized test box.

Fig. 1 - Test and application circuit ($G_v = 36$ dB)

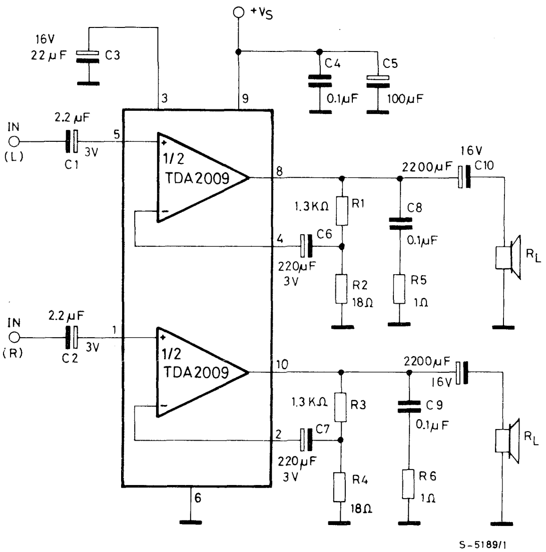


Fig. 2 - P.C. board and components layout of the circuit of fig. 1 (1 : 1 scale)

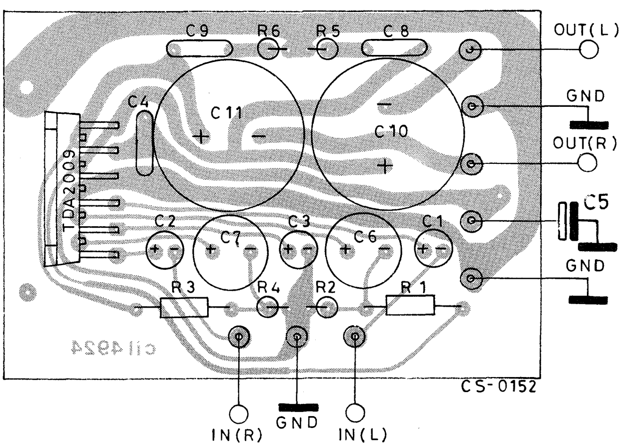


Fig. 3 - Output power vs. supply voltage

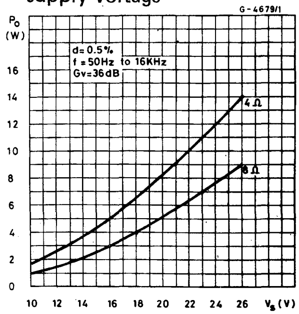


Fig. 4 - Output power vs. supply voltage

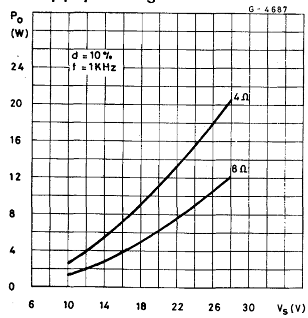


Fig. 5 - Distortion vs. output power

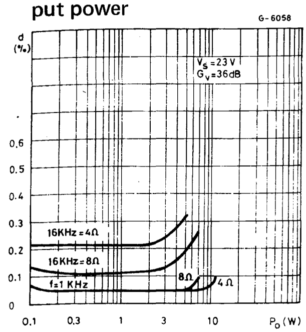


Fig. 6 - Distortion vs. frequency

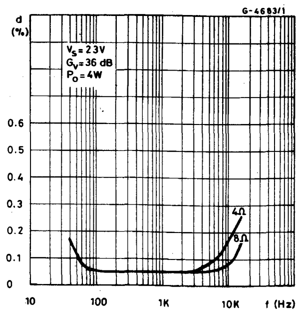


Fig. 7 - Quiescent current vs. supply voltage

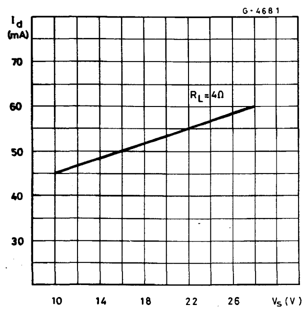


Fig. 8 - Supply voltage rejection vs. value of capacitor C3

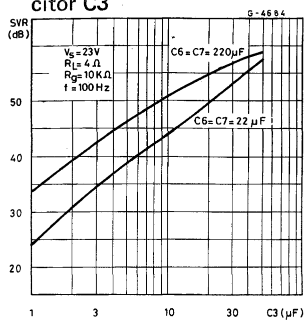


Fig. 9 - Supply voltage rejection vs. frequency

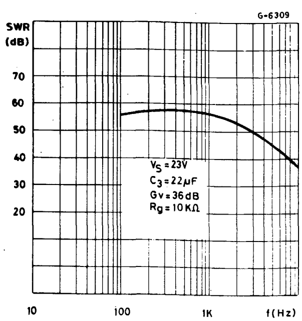


Fig. 10 - Total power dissipation an efficiency vs. output power

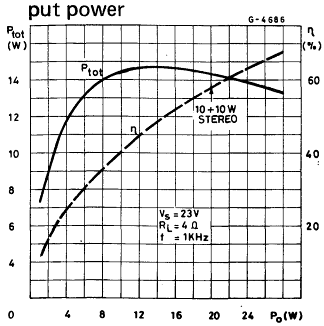


Fig. 11 - Total power dissipation and efficiency vs. output power

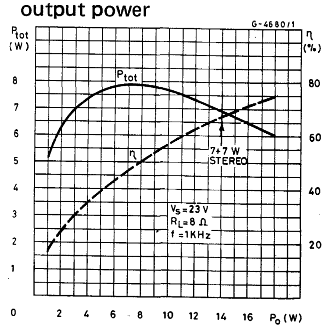


Fig. 12 - Cross-talk vs. frequency

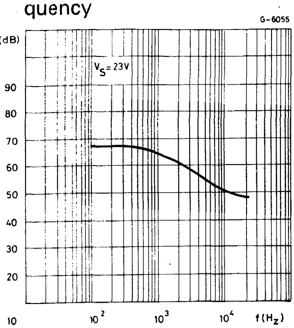


Fig. 13 - Output power vs. closed loop gain

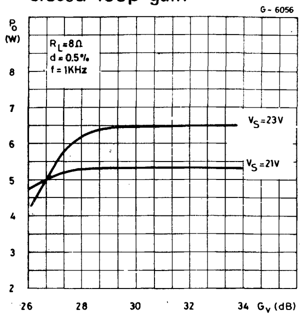
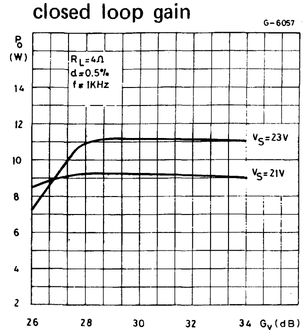


Fig. 14 - Output power vs. closed loop gain



APPLICATION INFORMATION

Fig. 15 - Simple short-circuit protection

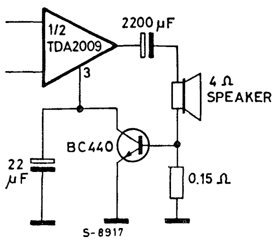


Fig. 16 - Example of muting circuit

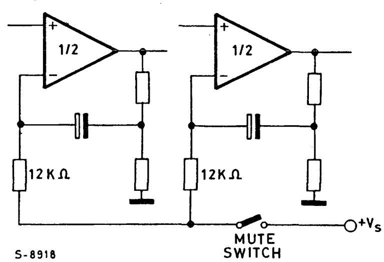


Fig. 17 - 10 + 10W stereo amplifier with tone balance and loudness control

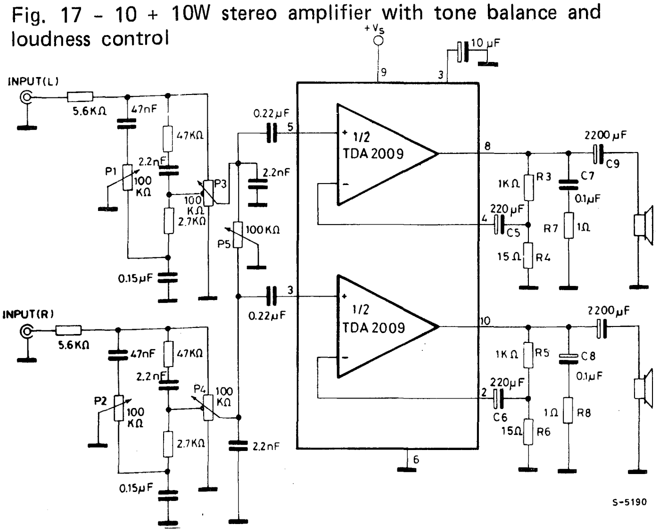
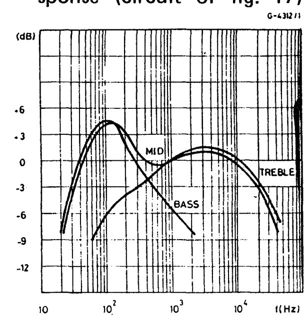


Fig. 18 - Tone control response (circuit of fig. 17)



APPLICATION INFORMATION (continued)

Fig. 19 - High quality 10 + 20W two way amplifier for stereo music center (one channel only)

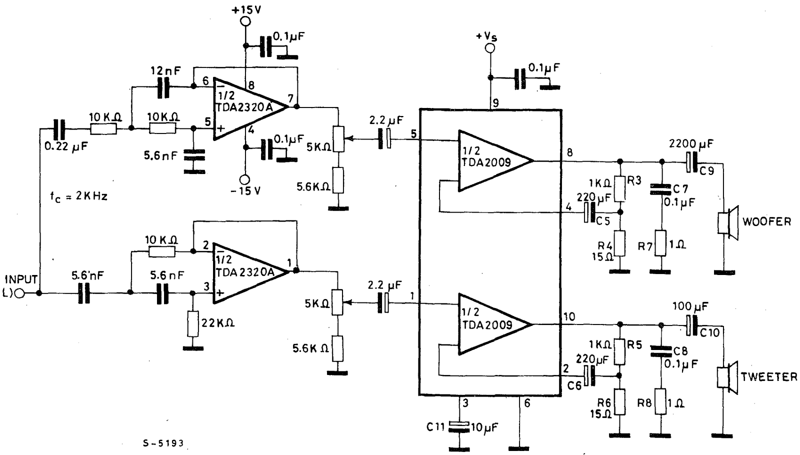


Fig. 20 - 18W bridge amplifier (d = 0.5%, G_v = 40dB)

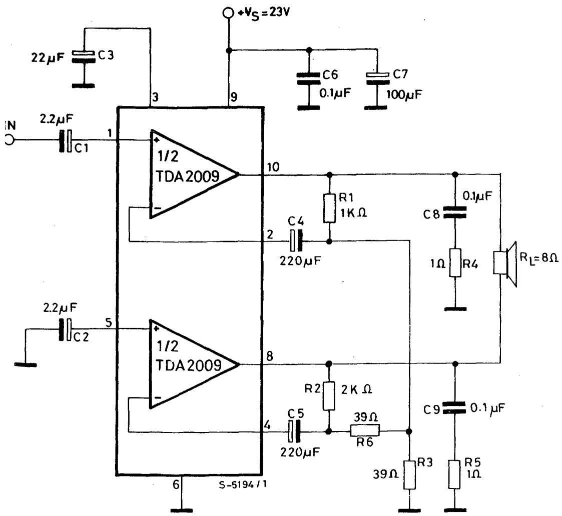
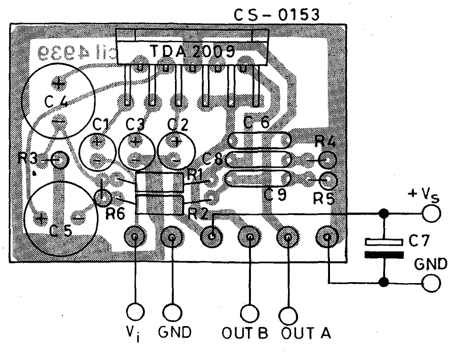


Fig. 21 - P.C. board and components layout of the circuit of fig. 20 (1 : 1 scale)



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 1 . Different values can be used; the following table can help the designer.

Component	Recomm. value	Purpose	Larger than	Smaller than
R1 and R3	1.2 KΩ	Close loop gain setting(*)	Increase of gain	Decrease of gain
R2 and R4	18 Ω		Decrease of gain	Increase of gain
R5 and R6	1 Ω	Frequency stability	Danger of oscillation at high frequency with inductive load	
C1 and C2	2.2 μF	Input DC decoupling	High turn-on delay	High turn-on pop Higher low frequency cutoff. Increase of noise
C3	22 μF	Ripple rejection	Better SVR. Increase of the switch-on time	Degradation of SVR.
C6 and C7	220 μF	Feedback Input DC decoupling.		
C8 and C9	0.1 μF	Frequency stability.		Danger of oscillation.
C10 and C11	1000 μF to 2200 μF	Output DC decoupling.		Higher low-frequency cut-off.

(*) The closed loop gain must be higher than 26dB

BUILD-IN PROTECTION SYSTEMS

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even it is permanent), or an excessive ambient temperature can be easily withstood.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuits. There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 22 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 22 - Maximum allowable power dissipation vs. ambient temperature

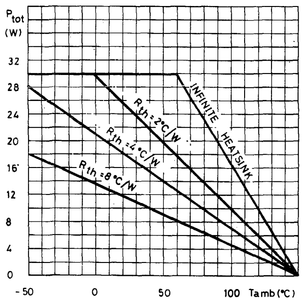
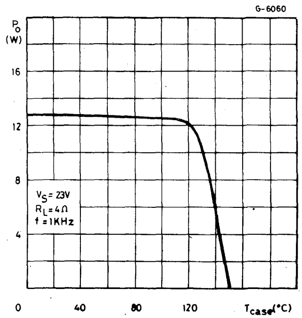


Fig. 23 - Output power vs. case temperature



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

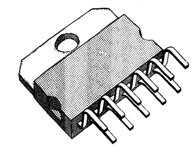
SGS-THOMSON MICROELECTRONICS

TDA2009A

10+10W SHORT CIRCUIT PROTECTED STEREO AMPLIFIER

The TDA2009A is class AB dual Hi-Fi Audio power amplifier assembled in Multiwatt® package, specially designed for high quality stereo application as Hi-Fi and music centers. Its main features are:

- High output power (10 + 10W min. @ d = 1%)
- High current capability (up to 3.5A)
- AC short circuit protection
- Thermal overload protection
- Space and cost saving: very low number of external components and simple mounting thanks to the Multiwatt® package.



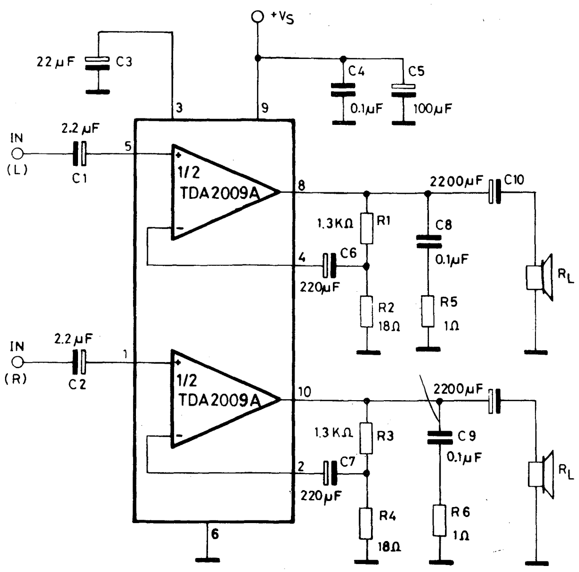
Multiwatt-11

ORDERING NUMBER: TDA2009A

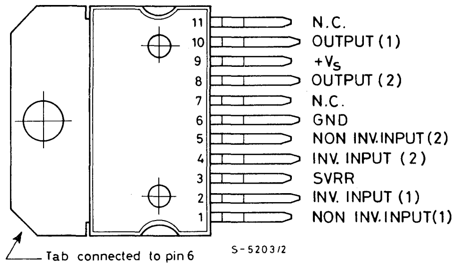
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
I_o	Output peak current (repetitive f ⩾ 20Hz)	3.5	A
I_o	Output peak current (non repetitive, t = 100μs)	4.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

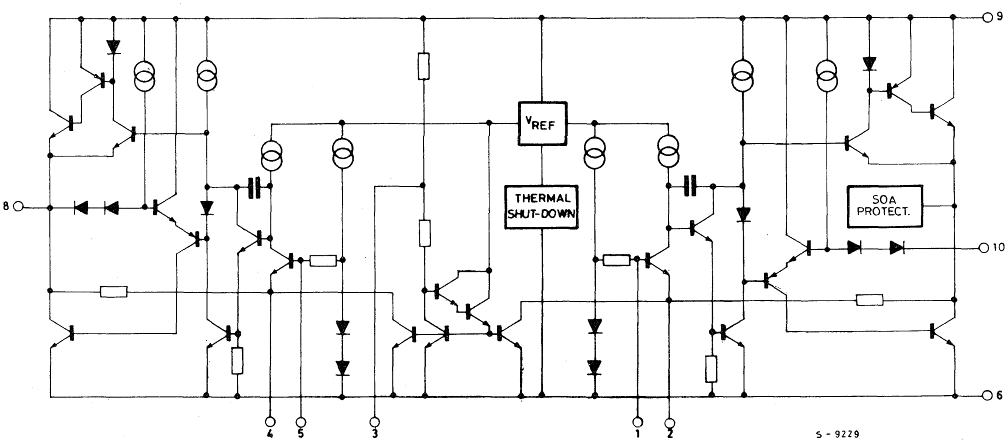
TEST CIRCUIT



CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the stereo application circuit, T_{amb} = 25°C, V_s = 24V, G_v = 36 dB, unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			8		28	V
V_o	Quiescent output voltage	V_s = 24V			11.5		V
I_d	Total quiescent drain current	V_s = 28V			60	120	mA
P_o	Output power (each channel)	d = 1% V_s = 24V f = 1KHz R_L = 4Ω R_L = 8Ω			12.5 7		W W
		f = 40Hz to 12.5KHz R_L = 4Ω R_L = 8Ω		10 5			W W
		V_s = 18V f = 1KHz R_L = 4Ω R_L = 8Ω			7 4		W W
d	Distortion (each channel)	f = 1KHz V_s = 24V P_o = 0.1 to 7W R_L = 4Ω P_o = 0.1 to 3.5W R_L = 8Ω			0.2 0.1		% %
		V_s = 18V P_o = 0.1 to 5W R_L = 4Ω P_o = 0.1 to 2.5W R_L = 8Ω			0.2 0.1		% %
CT	Cross talk	R_L = ∞	f = 1KHz		60		dB
		R_g = 10KΩ	f = 10KHz		50		dB
V_i	Input saturation voltage (rms)			300			mV
R_i	Input resistance	f = 1KHz non inverting input		70	200		KΩ
f_L	Low frequency roll of (-3dB)	R_L = 4Ω			20		Hz
f_H	High frequency roll off (-3dB)				80		KHz
G_v	Voltage gain (closed loop)	f = 1KHz		35.5	36	36.5	dB
ΔG_v	Closed loop gain matching				0.5		dB
e_N	Total input noise voltage	R_g = 10KΩ (°)			1.5		µV
		R_g = 10KΩ (°°)			2.5	8	µV
SVR	Supply voltage rejection (each channel)	R_g = 10KΩ f_{ripple} = 100Hz V_{ripple} = 0.5V			55		dB
T_J	Thermal shut-down junction temperature				145		°C

(°) Curve A (°°) 22Hz to 22KHz

Fig. 1 - Test and application circuit (G_v = 36dB)

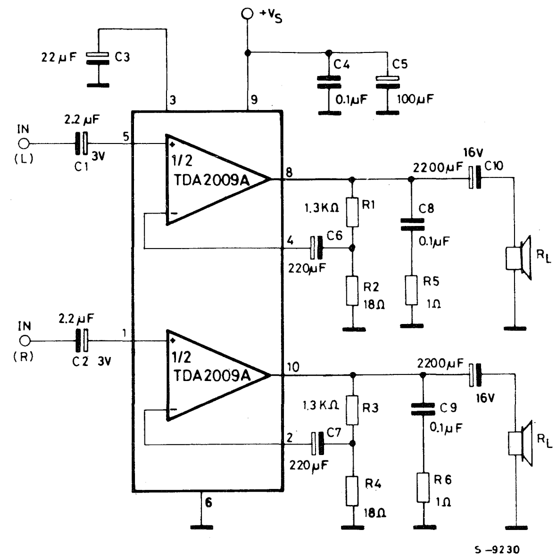


Fig. 2 - P.C. board components layout of the circuit of fig. 1 (1 : 1 scale)

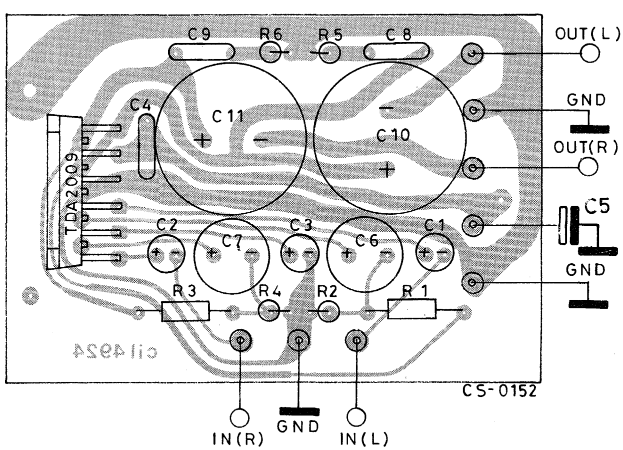


Fig. 3 - Output power vs. supply voltage

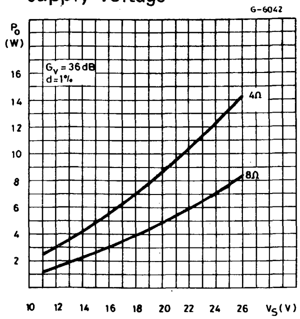


Fig. 4 - Output power vs. supply voltage

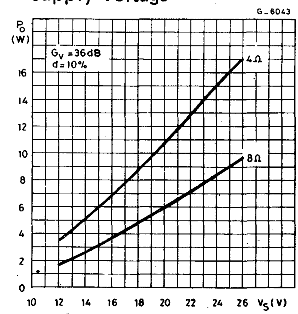


Fig. 5 - Distortion vs. output power

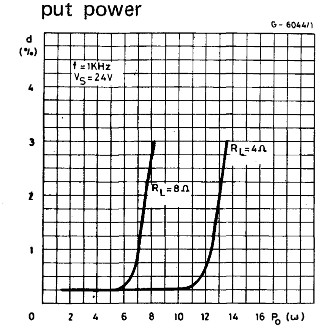


Fig. 6 - Distortion vs. frequency

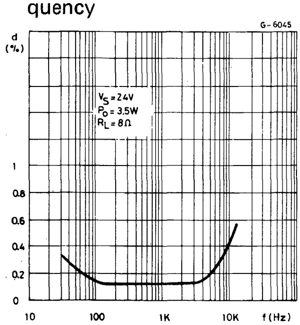


Fig. 7 - Distortion vs. frequency

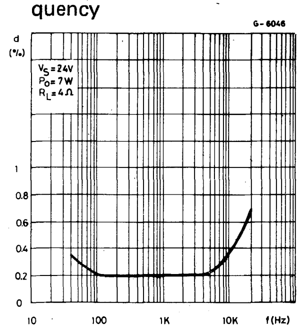


Fig. 8 - Quiescent current vs. supply voltage

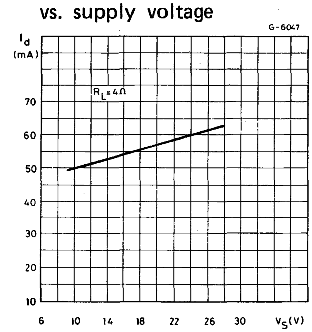


Fig. 9 - Supply voltage rejection vs. frequency

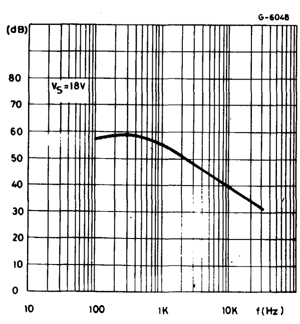


Fig. 10 - Total power dissipation and efficiency vs. output power

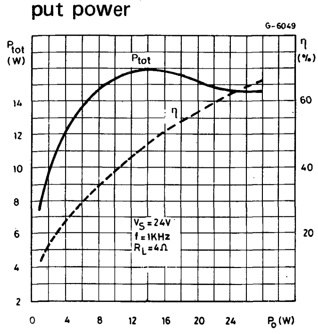
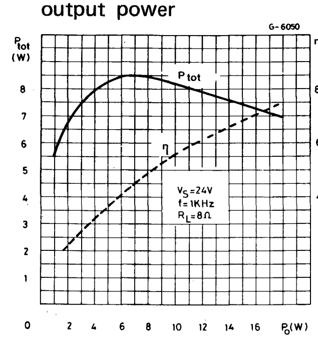


Fig. 11 - Total power dissipation and efficiency vs. output power



APPLICATION INFORMATION

Fig. 12 – Example of muting circuit

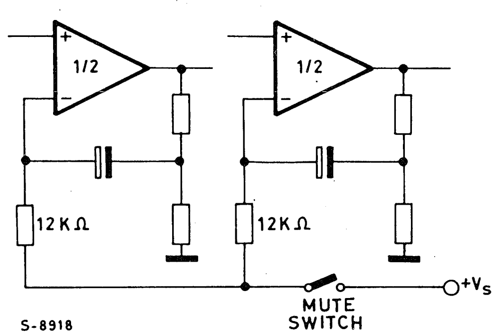


Fig. 13 – 10W + 10W stereo amplifier with tone balance and loudness control

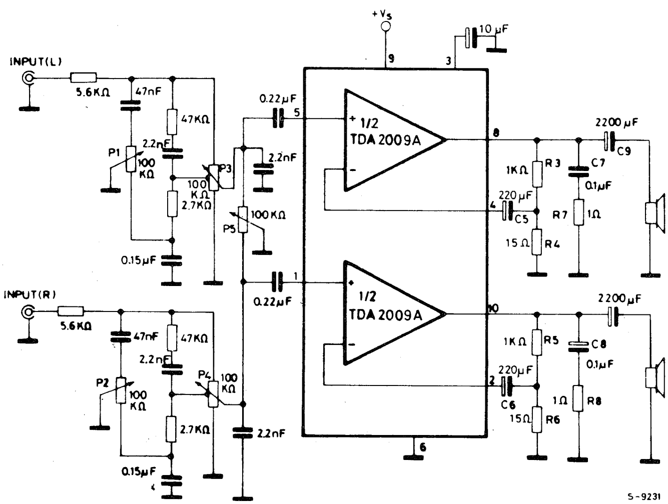
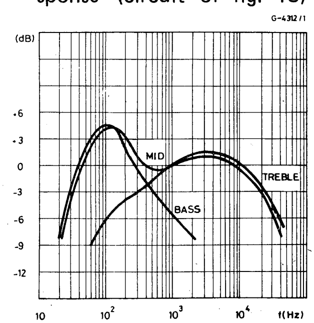


Fig. 14 – Tone control response (circuit of fig. 13)



APPLICATION INFORMATION (continued)

Fig. 15 - High quality 20 + 20W two way amplifier for stereo music center (one challel only)

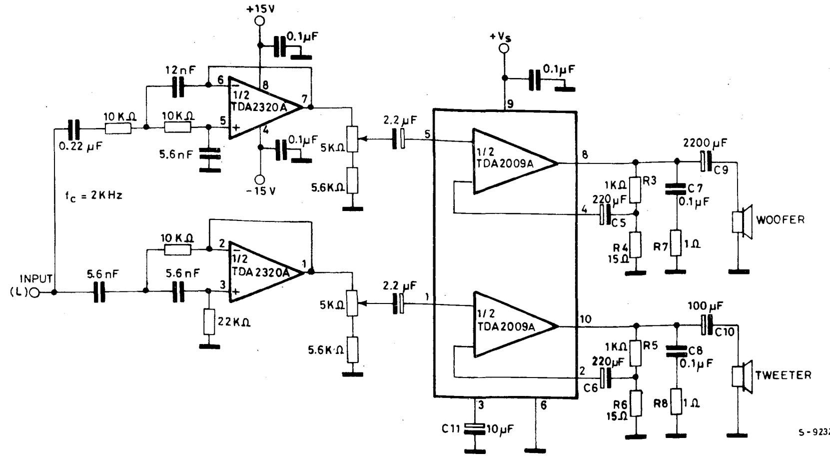


Fig. 16 - 18 W bridge amplifier (d = 1%, G_v = 40dB)

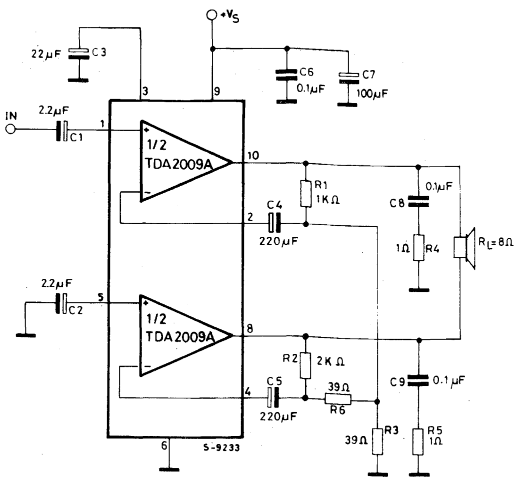
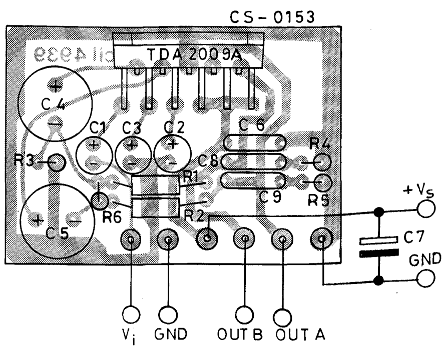


Fig. 17 - P.C. board and components layout of the circuit of fig. 16 (1 : 1 scale)



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 1. Different values can be used; the following table can help the designer.

Component	Recomm. value	Purpose	Larger than	Smaller than
R1 and R3	1.2KΩ	Close loop gain setting (*)	Increase of gain	Decrease of gain
R2 and R4	18KΩ		Decrease of gain	Increase of gain
R5 and R6	1Ω	Frequency stability	Danger of oscillation at high frequency with inductive load	
C1 and C2	2.2μF	Input DC decoupling	High turn-on delay	High turn-on pop Higher low frequency cutoff. Increase of noise
C3	22μF	Ripple rejection	Better SVR. Increase of the Switch-on time	Degradation of SVR
C6 and C7	220μF	Feedback input DC decoupling.		
C8 and C9	0.1μF	Frequency stability		Danger of oscillation
C10 and C11	1000μF to 2200μF	Output DC decoupling.		Higher low-frequency cut-off

(*) Closed loop gain must be higher than 26dB

BUILD-IN PROTECTION SYSTEMS

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_o are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 18 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Short circuit (AC Conditions). The TDA2009A can withstand an accidental short circuit from the output and ground made by a wrong connection during normal play operation.

Fig. 18 - Maximum allowable power dissipation vs. ambient temperature

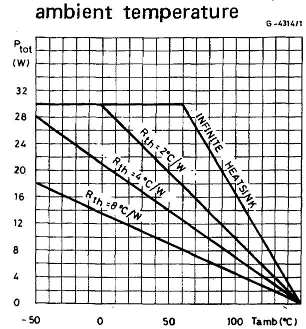


Fig. 19 - Output power vs. case temperature

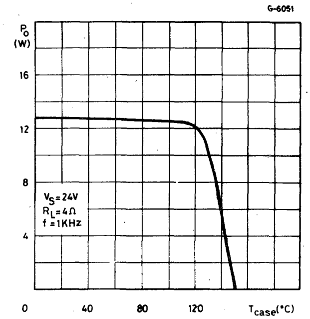
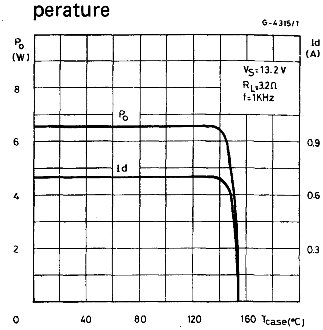


Fig. 20 - Output power and drain current vs. case temperature

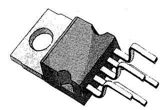


MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

14W Hi-Fi AUDIO AMPLIFIER

The TDA2030 is a monolithic integrated circuit in Pentawatt® package, intended for use as a low frequency class AB amplifier. Typically it provides 14W output power (d = 0.5%) at 14V/ 4Ω; at ± 14V the guaranteed output power is 12W on a 4Ω load and 8W on a 8Ω (DIN45500). The TDA2030 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included.



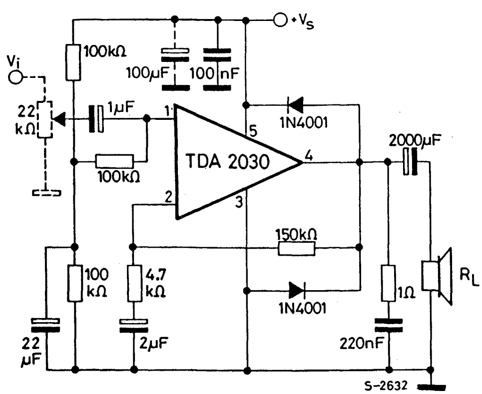
Pentawatt

ORDERING NUMBER: TDA2030H
TDA2030V

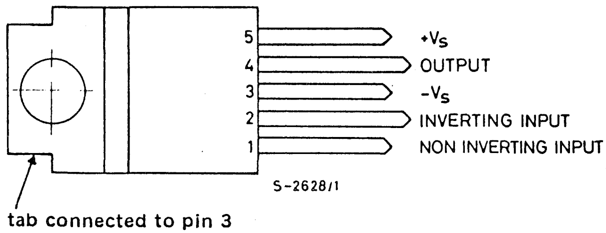
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Output peak current (internally limited)	3.5	A
P_{tot}	Power dissipation at $T_{case} = 90°C$	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

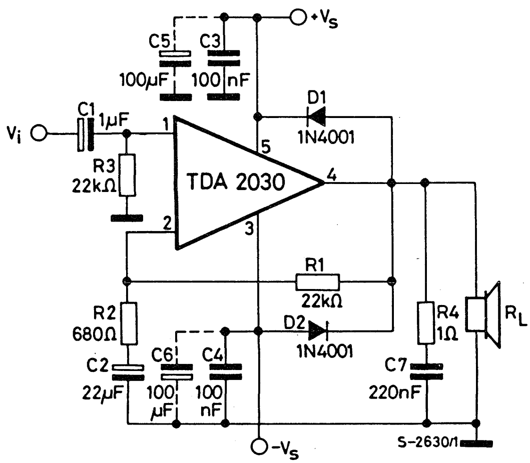
TYPICAL APPLICATION



CONNECTION DIAGRAM
(top view)



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = \pm 14V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 6		± 18	V
I_d	Quiescent drain current	$V_s = \pm 18V$		40	60	mA
I_b	Input bias current			0.2	2	μA
V_{os}	Input offset voltage			± 2	± 20	mV
I_{os}	Input offset current			± 20	± 200	nA
P_o	Output power	d = 0.5% G_v = 30 dB f = 40 to 15 000 Hz $R_L = 4\Omega$ $R_L = 8\Omega$	 12 8	 14 9		 W W
		d = 10% G_v = 30 dB f = 1 kHz $R_L = 4\Omega$ $R_L = 8\Omega$		 18 11		 W W
d	Distortion	P_o = 0.1 to 12W $R_L = 4\Omega$ G_v = 30 dB f = 40 to 15 000 Hz		0.2	0.5	%
		P_o = 0.1 to 8W $R_L = 8\Omega$ G_v = 30 dB f = 40 to 15 000 Hz		0.1	0.5	%
B	Power Bandwidth (-3 dB)	G_v = 30 dB P_o = 12W $R_L = 4\Omega$		10 to 140 000		Hz
R_i	Input resistance (pin 1)		0.5	5		MΩ
G_v	Voltage gain (open loop)			90		dB
G_v	Voltage gain (closed loop)	f = 1 kHz	29.5	30	30.5	dB
e_N	Input noise voltage	B = 22 Hz to 22 KHz		3	10	μV
i_N	Input noise current			80	200	pA
SVR	Supply voltage rejection	$R_L = 4\Omega$ G_v = 30 dB R_g = 22 kΩ V_{ripple} = 0.5 V_{eff} f_{ripple} = 100 Hz	40	50		dB
I_d	Drain current	P_o = 14W $R_L = 4\Omega$ P_o = 9W $R_L = 8\Omega$		900 500		mA mA
T_j	Thermal shut-down junction temperature			145		°C

Fig. 1 - Output power vs. supply voltage

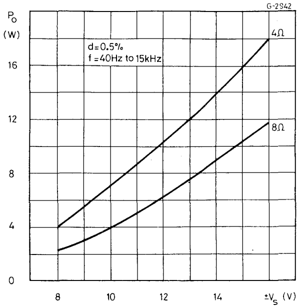


Fig. 2 - Output power vs. supply voltage

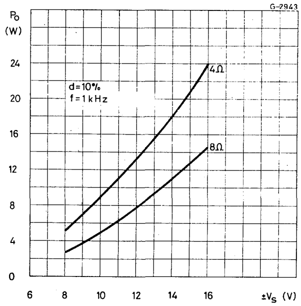


Fig. 3 - Distortion vs. output power

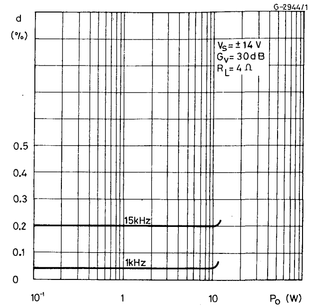


Fig. 4 - Distortion vs. output power

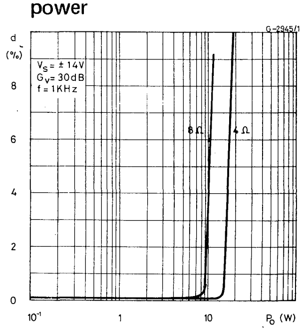


Fig. 5 - Distortion vs. output power

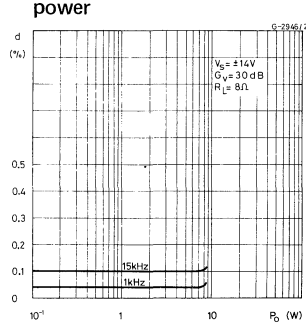


Fig. 6 - Distortion vs. frequency

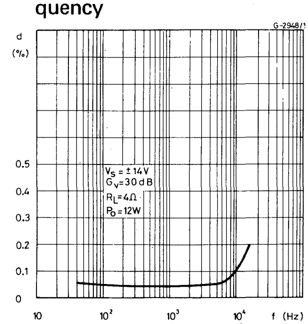


Fig. 7 - Distortion vs. frequency

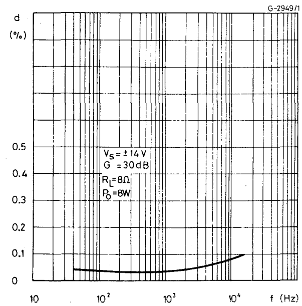


Fig. 8 - Frequency response with different values of the rolloff capacitor C8 (see fig. 13)

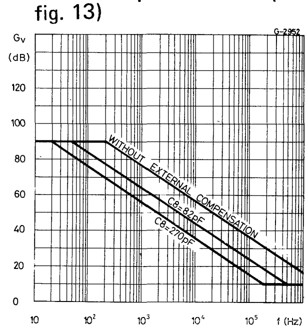


Fig. 9 - Quiescent current vs. supply voltage

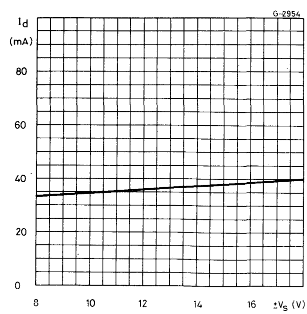


Fig. 10 - Supply voltage rejection vs. voltage gain

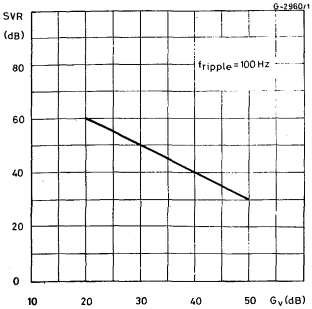


Fig. 11 - Power dissipation and efficiency vs. output power

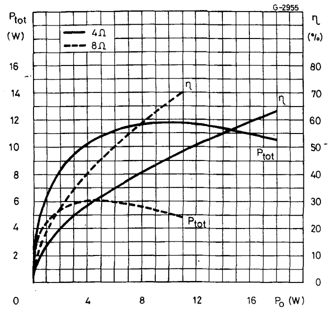
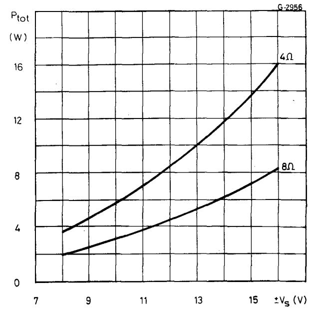


Fig. 12 - Maximum power dissipation vs. supply voltage (sine wave operation)



APPLICATION INFORMATION

Fig. 13 - Typical amplifier with split power supply

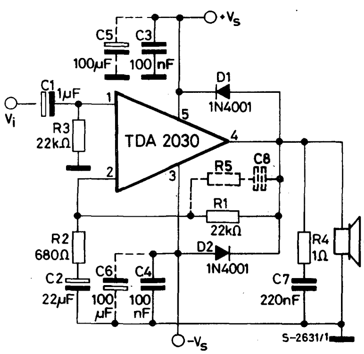
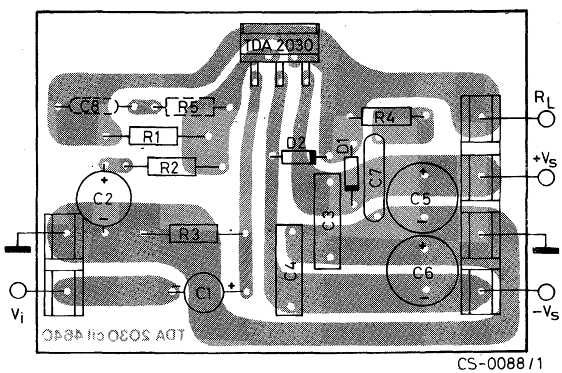


Fig. 14 - P.C. board and component layout for the circuit of fig. 13 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 15 - Typical amplifier with single power supply

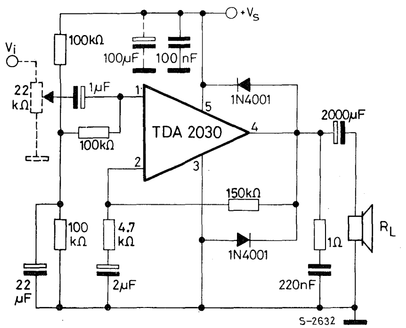


Fig. 16 - P.C. board and component layout for the circuit of fig. 15 (1:1 scale)

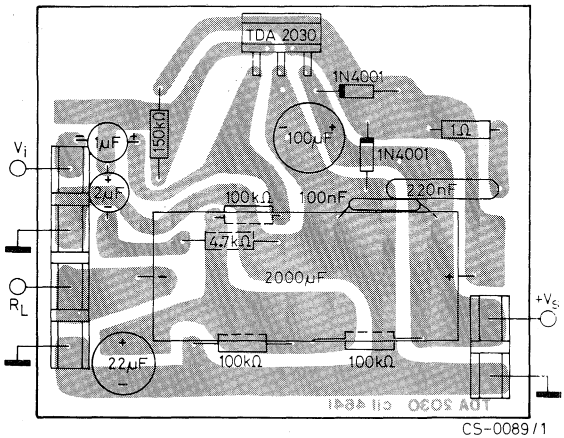
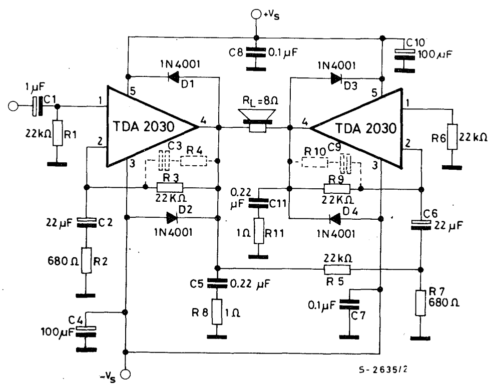


Fig. 17 - Bridge amplifier configuration with split power supply (P_o= 28W, V_s= ±14V)



PRACTICAL CONSIDERATIONS

Printed circuit board

The layout shown in Fig. 16 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

Assembly suggestion

No electrical isolation is needed between the package and the heatsink with single supply voltage configuration.

Application suggestions

The recommended values of the components are those shown on application circuit of fig. 13. Different values can be used. The following table can help the designer.

Component	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22 kΩ	Closed loop gain setting	Increase of gain	Decrease of gain (*)
R2	680 Ω	Closed loop gain setting	Decrease of gain (*)	Increase of gain
R3	22 kΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R4	1 Ω	Frequency stability	Danger of oscillat. at high frequencies with induct. loads	
R5	≅ 3 R2	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C1	1 μF	Input DC decoupling		Increase of low frequencies cutoff
C2	22 μ F	Inverting DC decoupling		Increase of low frequencies cutoff
C3,C4	0.1 μF	Supply voltage bypass		Danger of oscillation
C5,C6	100 μF	Supply voltage bypass		Danger of oscillation
C7	0.22 μF	Frequency stability		Danger of oscillat.
C8	$\cong \frac{1}{2\pi B R1}$	Upper frequency cutoff	Smaller bandwidth	Larger bandwidth
D1,D2	1N4001	To protect the device against output voltage spikes		

(*) Closed loop gain must be higher than 24dB

SHORT CIRCUIT PROTECTION

The TDA2030 has an original circuit which limits the current of the output transistors. Fig. 18 shows that the maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area (Fig. 2). This function can therefore be considered as being peak power limiting rather than simple current limiting.
It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

Fig. 18 - Maximum output current vs. voltage [V_{CEsat}] across each output transitor

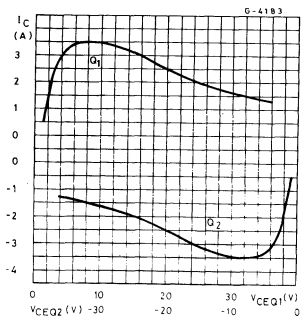
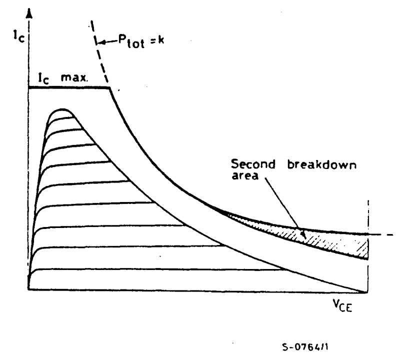


Fig. 19 - Safe operating area and collector characteristics of the protected power transistor



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1. An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2. The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation at the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 22 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 20 - Output power and drain current vs. case temperature ($R_L = 4\Omega$)

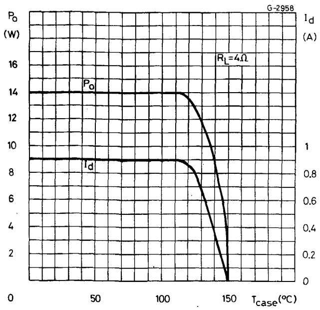


Fig. 21 - Output power and drain current vs. case temperature ($R_L = 8\Omega$)

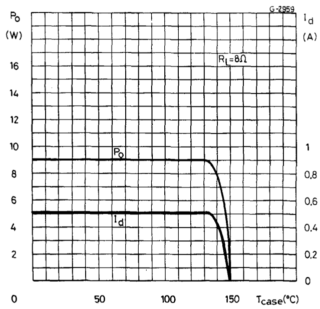


Fig. 22 - Maximum allowable power dissipation vs. ambient temperature

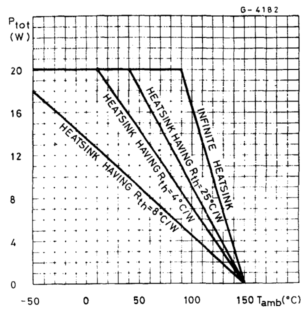
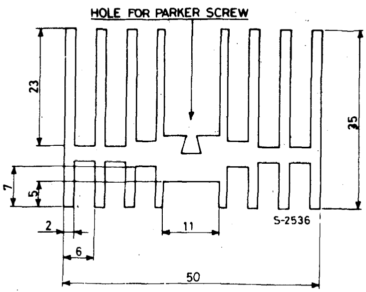


Fig. 23 - Example of heat-sink



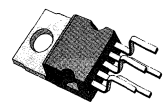
Dimension : suggestion.

The following table shows the length that the heatsink in fig. 23 must have for several values of P_{tot} and R_{th}.

P_{tot}(W)	12	8	6
Length of heatsink (mm)	60	40	30
R_{th} of heatsink (°C/W)	4.2	6.2	8.3

18W Hi-Fi AMPLIFIER AND 35W DRIVER

The TDA2030A is a monolithic IC in Pentawatt® package intended for use as low frequency class AB amplifier.
With $V_{s\,max}$ = 44V it is particularly suited for more reliable applications without regulated supply and for 35W driver circuits using low-cost complementary pairs.
The TDA2030A provides high output current and has very low harmonic and cross-over distortion.
Further the device incorporates a short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included



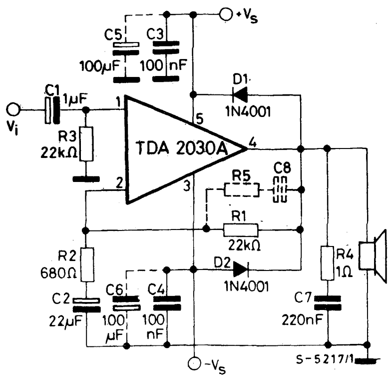
Pentawatt

ORDERING NUMBERS: TDA2030A
TDA2030AH

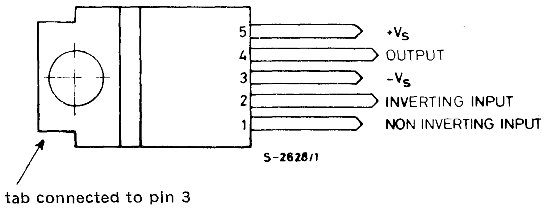
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 22	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Peak output current (internally limited)	3.5	A
P_{tot}	Total power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

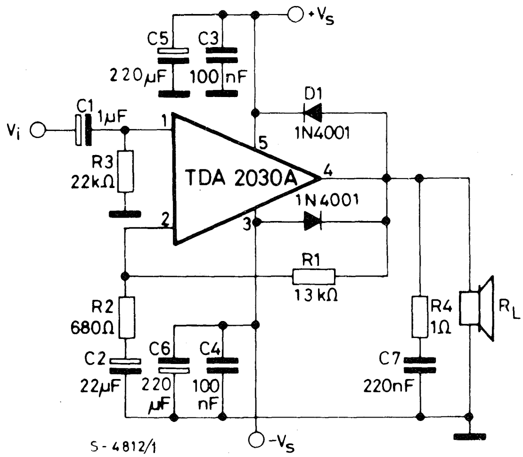
TYPICAL APPLICATION



CONNECTION DIAGRAM
(top view)



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_s= ±16V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			± 6		± 22	V
I_d	Quiescent drain current				50	80	mA
I_b	Input bias current	V_s = ± 22V			0.2	2	μA
V_{os}	Input offset voltage	V_s = ± 22V			± 2	± 20	mV
I_{os}	Input offset current				± 20	± 200	nA
P_o	Output power	d = 0.5% G_v = 26 dB f = 40 to 15000 Hz R_L= 4 Ω R_L= 8 Ω		 15 10	 18 12		W
		V_s = ± 19V	R_L= 8Ω	13	16		W
BW	Power bandwidth	P_o= 15W	R_L= 4 Ω		100		KHz
SR	Slew Rate				8		V/μsec
G_v	Open loop voltage gain	f = 1 KHz			80		dB
G_v	Closed loop voltage gain	f = 1 KHz		25.5	26	26.5	dB
d	Total harmonic distortion	P_o= 0.1 to 14W R_L= 4 Ω f = 40 to 15000 Hz f = 1 KHz			 0.08 0.03		%
		P_o = 0.1 to 9W R_L= 8 Ω f = 40 to 15000 Hz			0.05		%
d_2	Second order CCIF intermodulation distortion	P_o= 4W R_L= 4Ω	f_2-f_1 = 1 KHz		0.03		%
d_3.	Third order CCIF intermodulation distortion	f_1= 14 KHz f_2= 15 KHz	2 f_1-f_2= 13KHz		0.08		%
e_N	Input noise voltage	B = curve A			2		μV
		B = 22 Hz to 22 KHz			3	10	μV
i_N	Input noise current	B = curve A			50		pA
		B = 22 Hz to 22 KHz			80	200	pA
S/N	Signal to noise ratio	R_L= 4Ω R_g= 10 KΩ B = curve A	P_o = 15W		106		dB
			P_o = 1W		94		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
R_i	Input resistance (pin 1)	(open loop) f = 1 KHz	0.5	5		MΩ
SVR	Supply voltage rejection	R_L = 4 Ω G_v = 26 dB R_g = 22 KΩ f = 100 Hz		54		dB
T_j	Thermal shut-down junction temperature			145		°C

Fig. 1 - Single supply amplifier

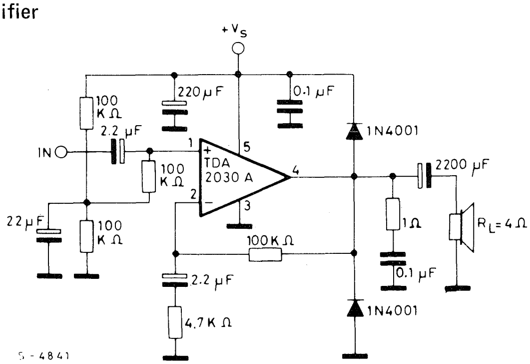


Fig. 2 - Open loop-frequency response

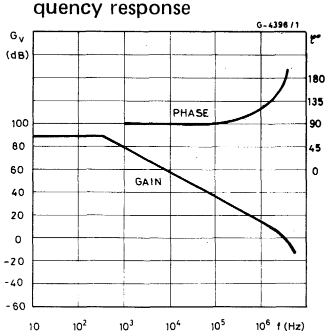


Fig. 3 - Output power vs. supply voltage

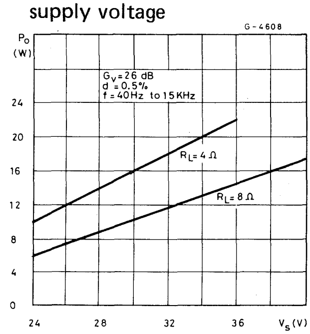
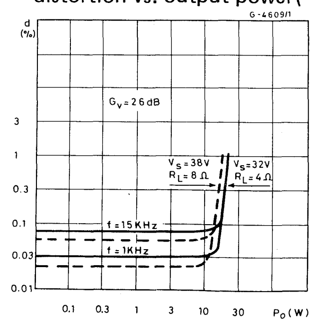


Fig. 4 - Total harmonic distortion vs. output power(*)



*) Test using noise filters.

Fig. 5 - Two tone CCIF intermodulation distortion

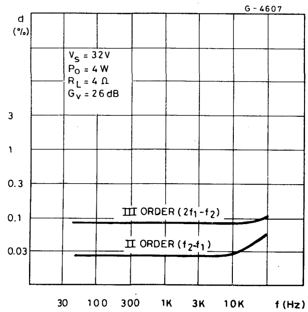


Fig. 6 - Large signal frequency response

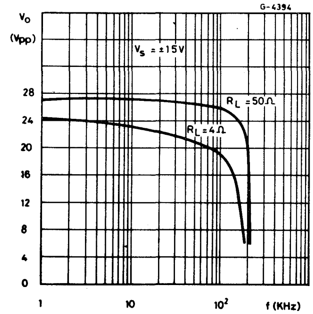


Fig. 7 - Maximum allowable power dissipation vs. ambient temperature

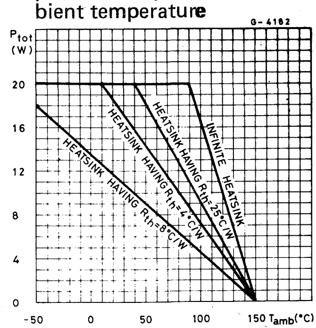


Fig. 8 - Single supply high power amplifier (TDA 2030A + BD907/BD908)

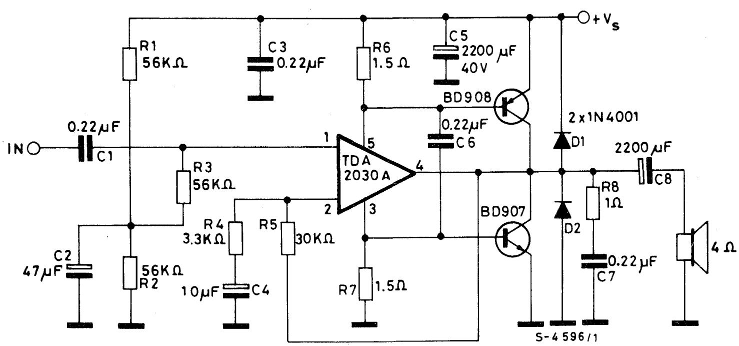
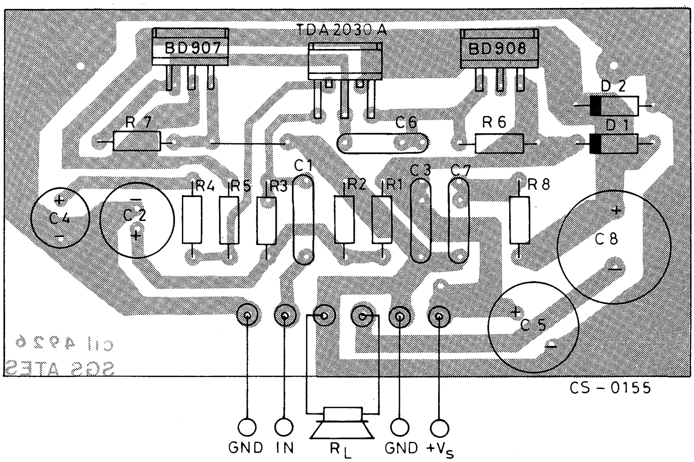


Fig. 9 - P.C. board and component layout for the circuit of fig. 8 (1:1 scale)



Typical performance of the circuit of fig. 8

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage				36	44	V
I_d	Quiescent drain current	V_s = 36V			50		mA
P_o	Output power	d = 0.5% R_L = 4Ω f = 40Hz to 15KHz	V_s = 39V		35		W
			V_s = 36V		28		
		d = 10%; f = 1KHz	V_s = 39V		44		W
		R_L = 4Ω	V_s = 36V		35		
G_v	Voltage gain	f = 1 KHz		19.5	20	20.5	dB
SR	Slew Rate				8		V/µsec
d	Total harmonic distortion		f = 1KHz		0.02		%
		P_o = 20W	f = 40 Hz to 15 KHz		0.05		
V_i	Input sensitivity	G_v = 20 dB P_o = 20W	f = 1 KHz R_L = 4Ω		890		mV
S/N	Signal to noise ratio	R_L = 4Ω R_g = 10 KΩ B = curve A	P_o = 25W		108		dB
			P_o = 4W		100		

Fig. 10 - Output power vs. supply voltage

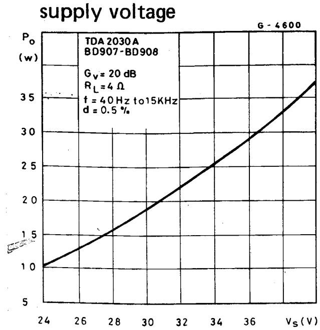


Fig. 11 - Total harmonic distortion vs. output power

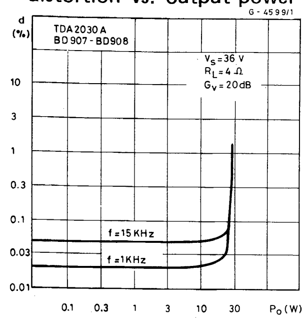


Fig. 12 - Output power vs. input level

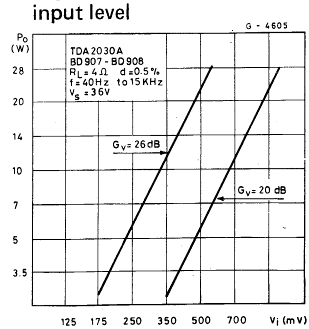


Fig. 13 - Power dissipation vs. output power

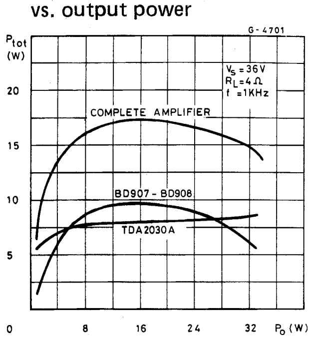


Fig. 14 - Typical amplifier whit split power supply

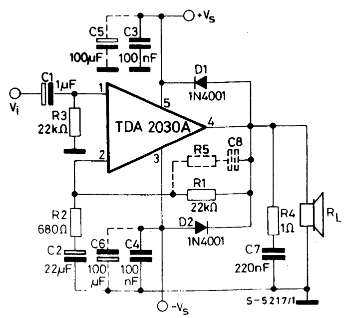


Fig. 15 - P.C. board and component layout for the circuit of fig. 14 (1 : 1 scale)

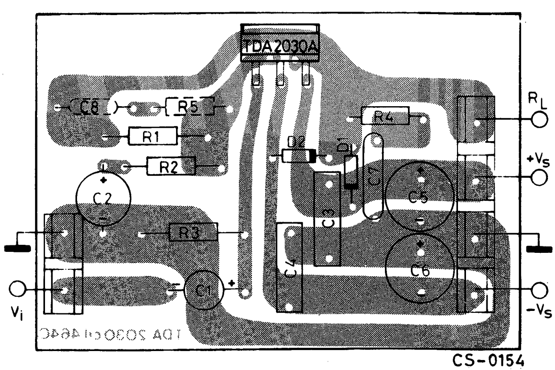


Fig. 16 - Bridge amplifier whit split power supply (P_o= 34W, V_s= ±16V)

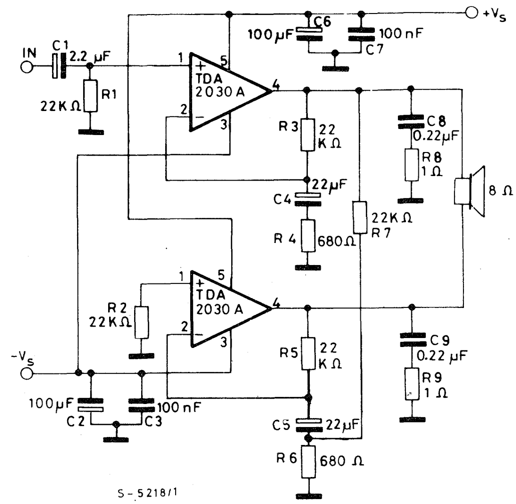
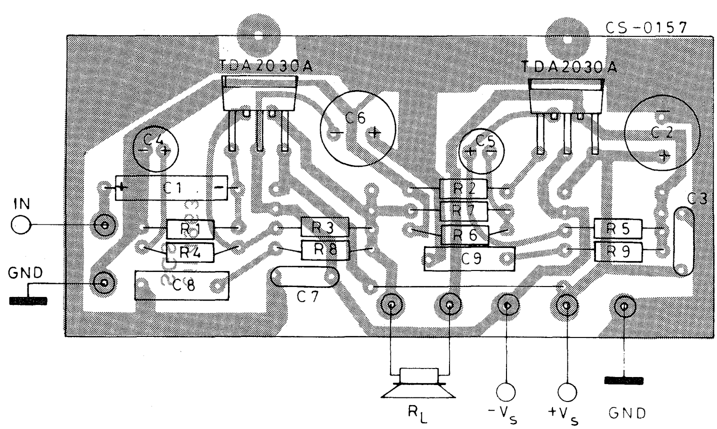


Fig. 17 - P.C. board and component layout for the circuit in fig. 16 (1:1 scale)



Multiway speaker systems and active boxes

Multiway loudspeaker systems provide the best possible acoustic performance since each loudspeaker is specially designed and optimized to handle a limited range of frequencies. Commonly, these loudspeaker systems divide the audio spectrum into two or three bands.
To maintain a flat frequency response over the Hi-Fi audio range the bands covered by each loudspeaker must overlap slightly. Imbalance between the loudspeakers produces unacceptable results therefore it is important to ensure that each unit generates the correct amount of acoustic energy for its segmento of the audio spectrum. In this respect it is also important to know the energy distribution of the music spectrum to determine the cutoff frequencies of the crossover filters (see Fig. 18). As an example, a 100W three-way system with crossover frequencies of 400Hz and 3KHz would require 50W for the woofer, 35W for the midrange unit and 15W for the tweeter.
Both active and passive filters can be used for crossovers but today active filters cost significantly less than a good passive filter using air-cored inductors and non-electrolytic capacitors. In addition, active filters do not suffer from the typical defects of passive filters:

- power less;
- increased impedance seen by the loudspeaker (lower damping)
- difficulty of precise design due to variable loudspeaker impedance.

Obviously, active crossovers can only be used if a power amplifier is provided for each drive unit. This makes it particularly interesting and economically sound to use monolithic power amplifiers.
In some applications, complex filters are not really necessary and simple RC low-pass and high-pass networks (6dB/octave) can be recommended.
The result obtained are excellent beceuse this is the best type of audio filter and the only one free from phase and transient distortion.
The rather poor out of band attenuation of single RC filters means that the loudspeaker must operate linearly well beyond the crossover frequency to avoid distortion.
A more effective solution, named "Active Power Filter" by SGS is shown in Fig. 19.
The proposed circuit can realize combined power amplifiers and 12dB/octave or 18dB/octave high-pass or low-pass filters.
In practice, at the input pins of the amplifier two equal and in-phase voltages are available, as required for the active filter operation.
The impedance at the pin (-) is of the order of 100Ω, while that of the pin (+) is very high, which is also what was wanted.

Fig. 19 - Active power filter

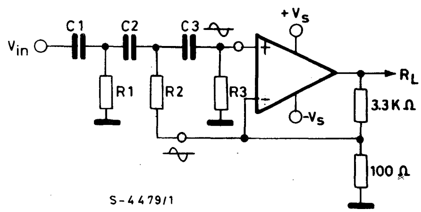
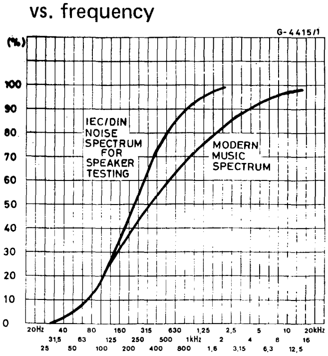


Fig. 18 - Power distribution vs. frequency



The component values calculated for $f_c = 900Hz$ using a Bessel 3rd order Sallen and Key structure are:

$C_1 = C_2 = C_3$	R_1	R_2	R_3
22nF	8.2KΩ	5.6KΩ	33KΩ

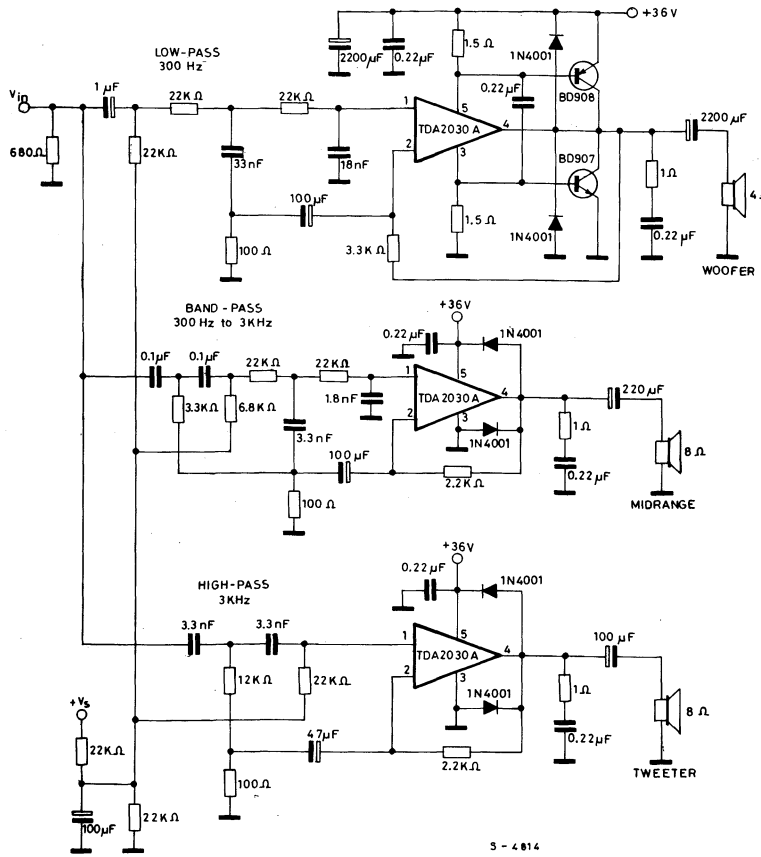
Using this type of crossover filter, a complete 3-way 60W active loudspeaker system is shown in Fig. 20.

It employs 2nd order Butttherworth filters with the crossover frequencies equal to 300Hz and 3KHz.

The midrange section consists of two filters, a high pass circuit followed by a low pass network. With $V_s = 36V$ the output power delivered to the woofer is 25W at d = 0.06% (30W at d = 0.5%). The power delivered to the midrange and the tweeter can be optimized in the design phase taking in account the loudspeaker efficiency and impedance (R_L = 4Ω to 8Ω).

It is quite common that midrange and tweeter speakers have an efficiency 3dB higher than woofers.

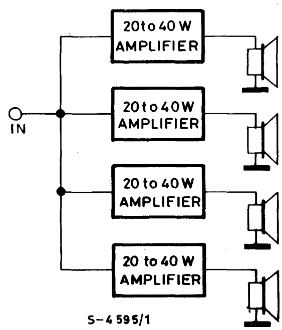
Fig. 20 - 3 way 60W active loudspeaker system ($V_s = 36V$)



Musical instruments amplifiers

Another important field of application for active systems is music.
In this area the use of several medium power amplifiers is more convenient than a single high power amplifier, and it is also more realiable. A typical example (see Fig. 21) consist of four amplifiers each driving a low-cost, 12 inch loud-speaker. This application can supply 80 to 160W rms.

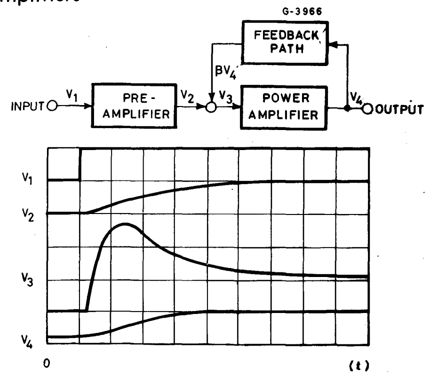
Fig. 21 - High power active box for musical instrument



Transient intermodulation distortion (TIM)

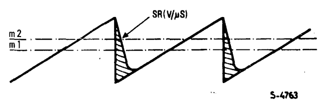
Transient intermodulation distortion is an unfortunate phenomen associated with negative-feedback amplifiers. When a feedback amplifier receives an input signal which rises very steeply, i.e. contains high-frequency components, the feedback can arrive too late so that the amplifiers overloads and a burst of intermodulation distortion will be produced as in Fig. 22. Since transients occur frequently in music this obviously a problem for the designer of audio amplifiers. Unfortunately, heavy negative feedback is frequency used to reduce the total harmonic distortion of an amplifier, which tends to aggravate the transient intermodulation (TIM situation. The best known method for the measurement of TIM consists of feeding sine waves superimposed onto square waves, into the amplifier under test. The output spectrum is then examined using a

Fig. 22 - Overshoot phenomenon in feedback amplifiers



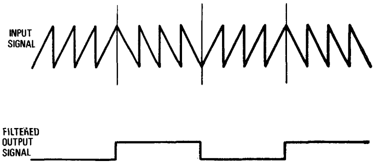
spectrum analyser and compared to the input. This method suffers from serious disadvantages: the accuracy is limited, the measurement is a rather delicate operation and an expensive spectrum analyser is essential. A new approach (see Technical Note 143) applied by SGS to monolithic amplifiers measurement is fast cheap-it requires nothing more sophisticated than an oscilloscope - and sensitive - and it can be used down to the values as low as 0.002% in high power amplifiers.
The "inverting-sawtooth" method of measurement is based on the response of an amplifier to a 20KHz sawtooth waveform. The amplifier has no difficulty following the slow ramp but it cannot follow the fast edge. The output will follow the upper line in Fig. 23 cutting of the shaded area and thus increasing the mean level. If this output signal is filtered to remove the sawtooth, direct voltage remains which indicates the amount of TIM distortion, although it is difficult to measure because it is indistinguishable from the DC offset of the amplifier. This problem is neatly avoided in the IS-TIM method

Fig. 23 - 20KHz sawtooth waveform



by periodically inverting the sawtooth waveform at a low audio frequency as shown in Fig. 24. In the case of the sawtooth in Fig. 25 the mean level was increased by the TIM distortion, for a sawtooth in the other direction the opposite is true.

Fig. 24 - Inverting sawtooth waveform

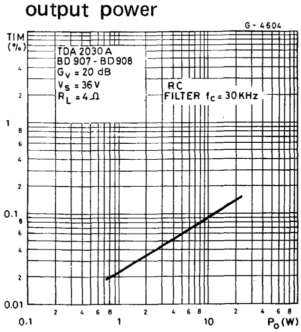


The result is an AC signal at the output whole peak-to-peak value is the TIM voltage, which can be measured easily with an oscilloscope. If the peak-to-peak value of the signal and the peak-to-peak of the inverting sawtooth are measured, the TIM can be found very simply from:

$$TIM = \frac{V_{out}}{V_{sawtooth}} \cdot 100$$

In Fig. 25 the experimental results are shown for the 30W amplifier using the TDA2030A as a driver and a low-cost complementary pair. A simple RC filter on the input of the amplifier to limit the maximum signal slope (SS) is an effective way to reduce TIM.

Fig. 25 - TIM distortion vs. output power



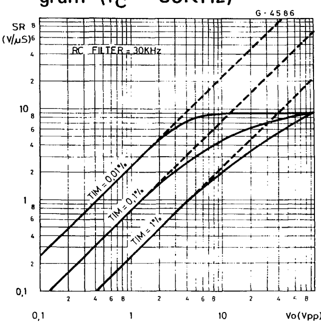
The diagram of Fig. 26 originated by SGS can be used to find the Slew-Rate (SR) required for a given output power or voltage and a TIM design target.

For example if an anti-TIM filter with a cutoff at 30KHz is used and the max. peak-to-peak output voltage is 20V then, referring to the diagram, a Slew-Rate of 6V/µs is necessary for 0.1% TIM.

As shown Slew-Rates of above 10V/µs do not contribute to a further reduction in TIM.

Slew-Rates of 100/µs are not only useless but also a disadvantage in Hi-Fi audio amplifiers because they tend to turn the amplifier into a radio receiver.

Fig. 26 - TIM design diagram (f_C = 30KHz)



Power supply

Using monolithic audio amplifier with non-regulated supply voltage it is important to design the power supply correctly. In any working case it must provide a supply voltage less than the maximum value fixed by the IC breakdown voltage.

It is essential to take into account all the working conditions, in particular mains fluctuations and supply voltage variations with and without load. The TDA2030A ($V_{s\,max}$ = 44V) is particularly suitable for substitution of the standard IC power amplifiers (with $V_{s\,max}$ = 36V) for more reliable applications.

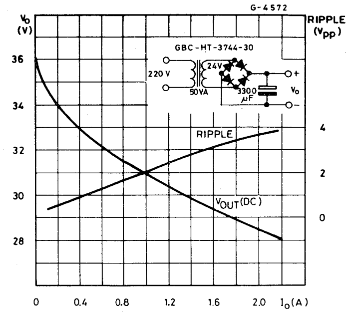
An example, using a simple full-wave rectifier followed by a capacitor filter, is shown in the table and in the diagram of Fig. 27.

A regulated supply is not usually used for the power output stages because of its dimensioning must be done taking into account the power to supply in the signal peaks. They are only a small percentage of the total music signal, with consequently large overdimensioning of the circuit.

Even if with a regulated supply higher output power can be obtained (V_s is constant in all working conditions), the additional cost and power dissipation do not usually justify its use. Using non-regulated supplies, there are fewer designe restriction. In fact, when signal peaks are present, the capacitor filter acts as a flywheel supplying the required energy.

In average conditions, the continuous power supplied is lower. The music power/continuous power ratio is greater in this case than for the case of regulated supplied, with space saving and cost reduction.

Fig. 27 - DC characteristics of 50W non-regulated supply



Mains (220V)	Secondary voltage	DC output voltage (V_O)		
		I_O = 0	I_O = 0.1A	I_O = 1A
+20%	28.8V	43.2V	42V	37.5V
+15%	27.6V	41.4V	40.3V	35.8V
+10%	26.4V	39.6V	38.5V	34.2V
–	24V	36.2V	35V	31V
-10%	21.6V	32.4V	31.5V	27.8V
-15%	20.4V	30.6V	29.8V	26V
-20%	19.2V	28.8V	28V	24.3V

Application suggestion

The recommended values of the components are those shown on application circuit of Fig. 14. Different values can be used. The following table can help the designer.

Component	Recommended value	Purpose	Larger than recommended value	Smeller than recommended value
R1	22KΩ	Closed loop gain setting.	Increase of gain.	Decrease of gain. *
R2	680Ω	Closed loop gain setting.	Decrease of gain. *	Increase of gain.
R3	22KΩ	Non inverting input biasing.	Increase of input impedance.	Decrease of input impedance.
R4	1Ω	Frequency stability.	Danger of oscillation at high frequencies with inductive loads.	
R5	≅ 3 R2	Upper frequency cutoff.	Poor high frequencies attenuation.	Danger of oscillation.
C1	1μF	Input DC decoupling.		Increase of low frequencies cutoff.
C2	22μF	Inverting DC decoupling.		Increase of low frequencies cutoff.
C3, C4	0.1μF	Supply voltage bypass.		Danger of oscillation.
C5, C6	100μF	Supply voltage bypass.		Danger of oscillation.
C7	0.22μF	Frequency stability.		Larger bandwidth.
C8	$\cong \frac{1}{2\pi\ B\ R1}$	Upper frequency cutoff.	Smaller bandwidth.	Larger bandwidth.
D1, D2	1N4001	To protect the device against output voltage spikes.		

* The value of closed loop gain must be higher than 24dB.

SHORT CIRCUIT PROTECTION

The TDA2030A has an original circuit which limits the current of the output transistors. This function can be considered as being peak power limiting rather than simple current limiting. It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

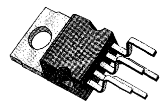
1. An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2. The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

SGS-THOMSON MICROELECTRONICS

TDA2040

20W Hi-Fi AUDIO POWER AMPLIFIER

The TDA2040 is a monolithic integrated circuit in Pentawatt® package, intended for use as an audio class AB amplifier. Typically it provides 22W output power (d = 0.5%) at $V_s = 32V/4\Omega$. The TDA2040 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates a patented short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A thermal shut-down system is also included.



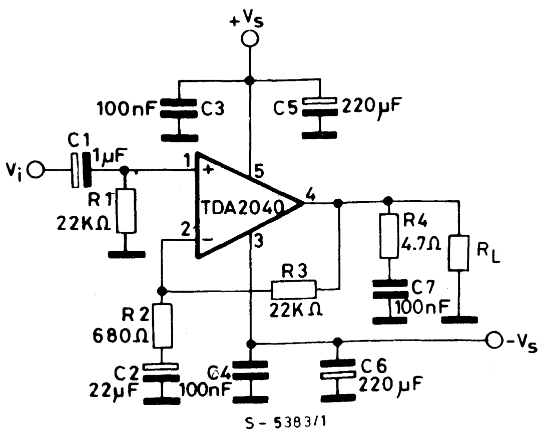
Pentawatt

ORDERING NUMBER: TDA2040V
TDA2040H

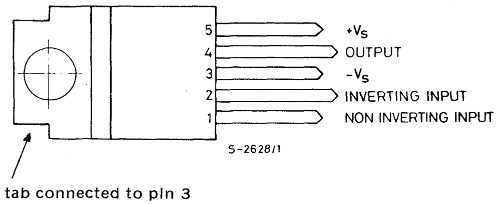
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 20	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o.	Output peak current (internally limited)	4	A
P_{tot}	Power dissipation at $T_{case} = 75°C$	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

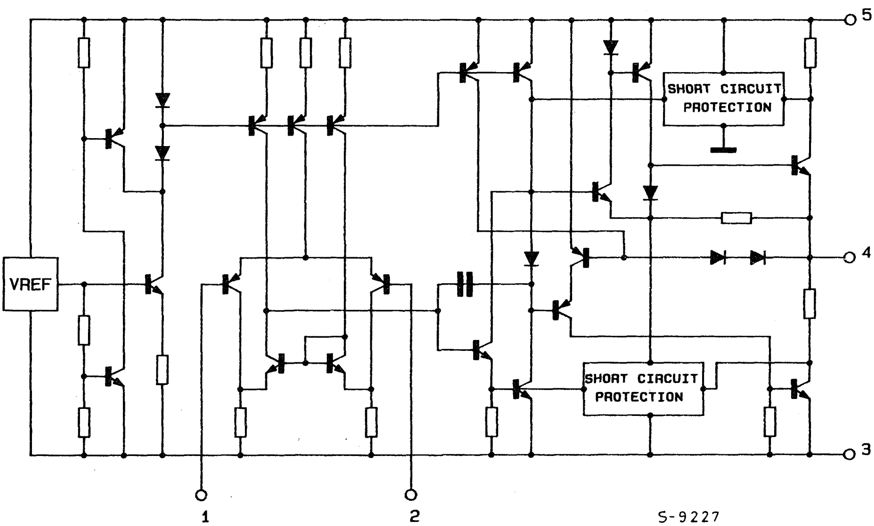
TEST CIRCUIT



CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_s = ±16V, T_{amb} = 25°C unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 2.5		± 20	V
I_d	Quiescent drain current	V_s = ± 4.5V			30	mA
		V_s = ± 20V		45	100	mA
I_b	Input bias current	V_s = ± 20V		0.3	1	μA
V_{os}	Input offset voltage	V_s = ± 20V		± 2	± 20	mV
I_{os}	Input offset current				±200	nA
P_o	Output power	d = 0.5% T_{case} = 60°C f = 1 KHz R_L = 4Ω R_L = 8Ω	20	22 12		W
		f = 15 KHz R_L = 4Ω	15	18		W
BW	Power bandwidth	P_o = 1W R_L = 4Ω		100		KHz
G_v	Open loop voltage gain	f = 1 KHz		80		dB
G_v	Closed loop voltage gain	f = 1 KHz	29.5	30	30.5	dB
d	Total harmonic distortion	P_o = 0.1 to 10W R_L = 4Ω f = 40 to 15000Hz f = 1 KHz		0.08 0.03		%
e_N	Input noise voltage	B = curve A		2		μV
		B = 22 Hz to 22 KHz		3	10	μV
i_N	Input noise current	B = curve A		50		pA
		B = 22 Hz to 22 KHz		80	200	pA
R_i	Input resistance (pin 1)		0.5	5		MΩ
SVR	Supply voltage rejection	R_L = 4Ω G_v = 30 dB R_g = 22 KΩ f = 100 Hz V_{ripple} = 0.5 V_{rms}	40	50		dB
η	Efficiency	f = 1 KHz P_o = 12W R_L = 8Ω P_o = 22W R_L = 4Ω		66 63		%
T_j	Thermal shut-down junction temperature			145		°C

Fig. 1 - Output power vs. supply voltage

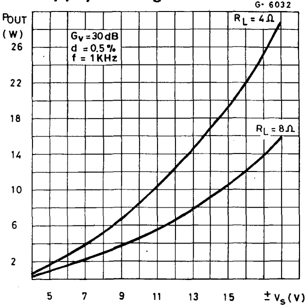


Fig. 2 - Output power vs. supply voltage

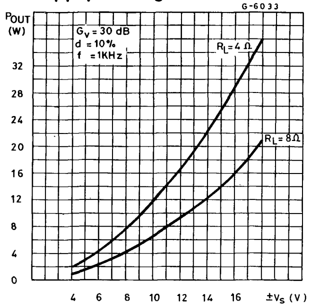


Fig. 3 - Output power vs. supply voltage

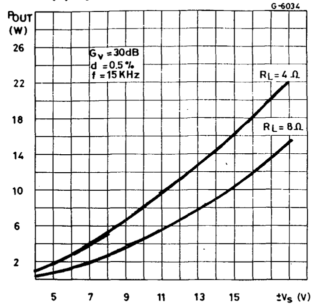


Fig. 4 - Distortion vs. frequency

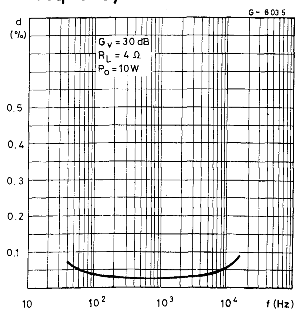


Fig. 5 - Supply voltage rejection vs. frequency

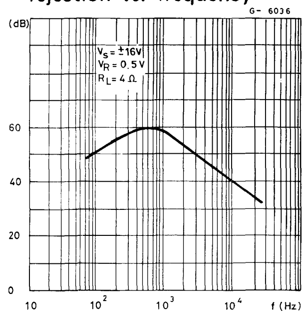


Fig. 6 - Supply voltage rejection vs. voltage gain

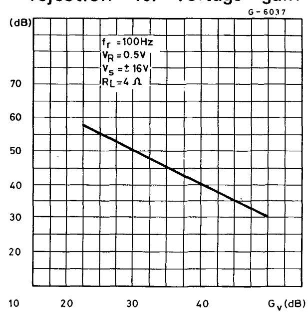


Fig. 7 - Quiescent drain current vs. supply voltage

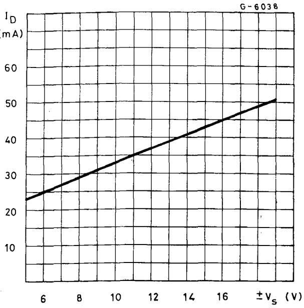


Fig. 8 - Open loop gain vs. frequency

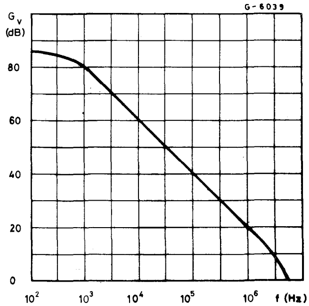
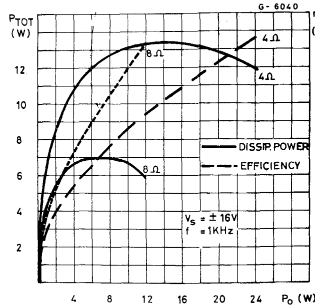


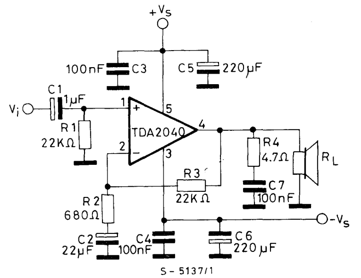
Fig. 9 - Power dissipation vs. output power



SGS-THOMSON MICROELECTRONICS

APPLICATION INFORMATION

Fig. 10 - Amplifier with split power supply (*)



$V_s = \pm 16V$
$R_L = 4\Omega$
$P_o \geqslant 15W$ (d = 0.5%)

Fig. 11 - P.C. board and components layout of the circuit of fig. 10 (1:1 scale)

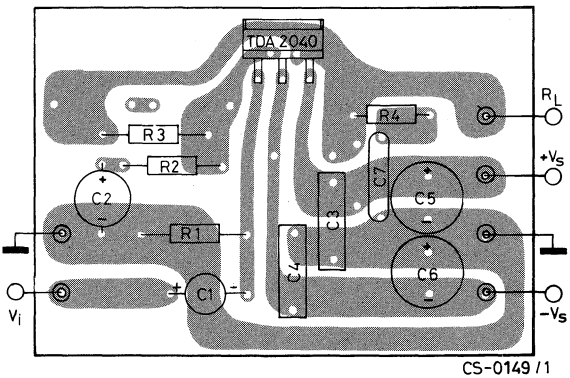


Fig. 12 - Amplifier with single supply (*)

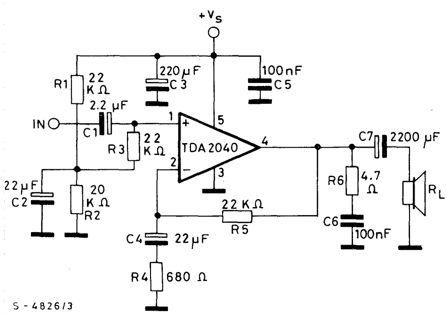
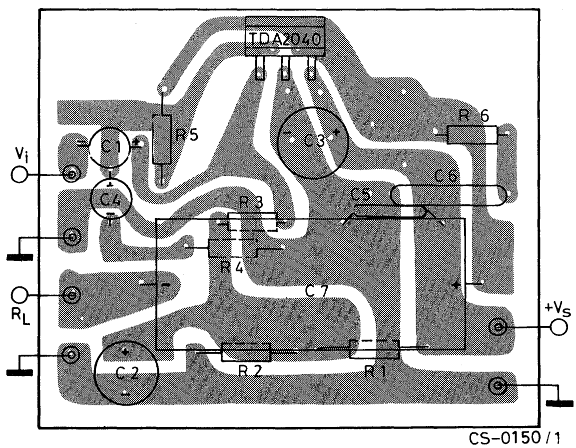


Fig. 13 - P.C. board and components layout of the circuit of fig. 12 (1:1 scale)



* In the case of highly inductive loads protection diodes may be necessary.

APPLICATION INFORMATION (continued)

Fig. 14 - 30W Bridge amplifier with split power supply

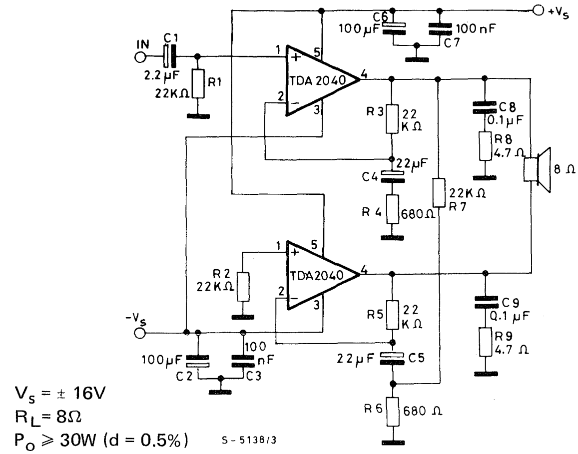
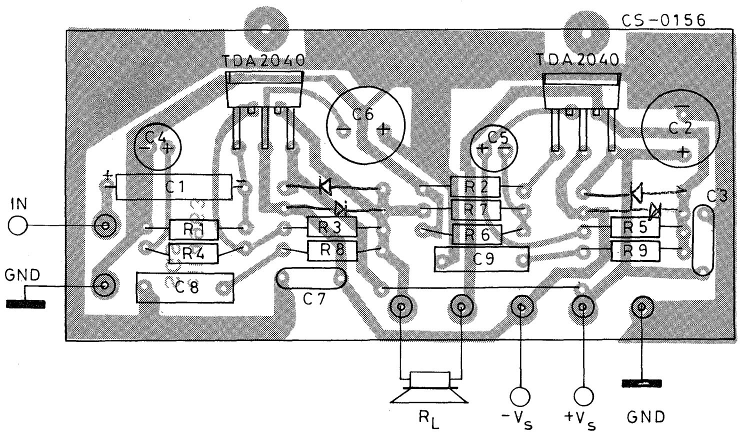


Fig. 15 - P.C. board and components layout for the circuit of fig. 14 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 16 - Two way Hi-Fi system with active crossover

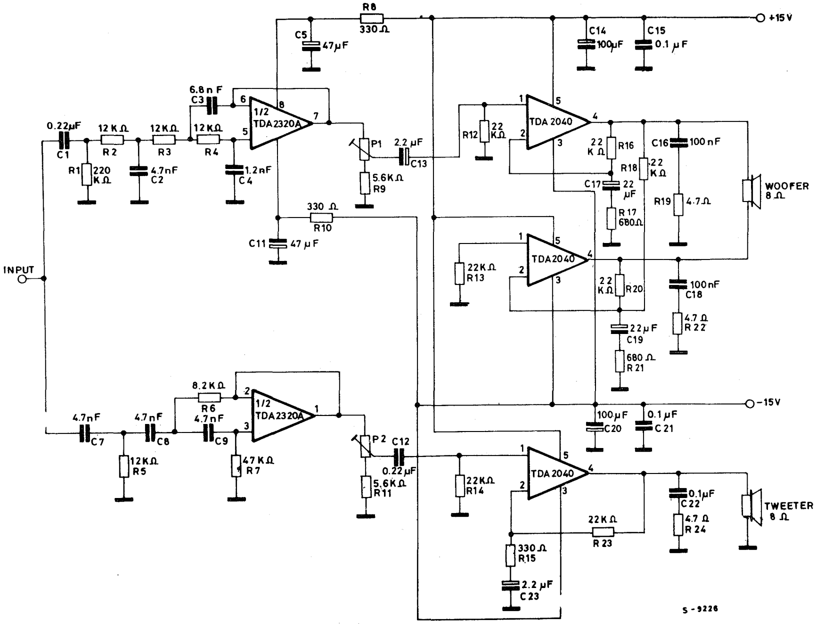
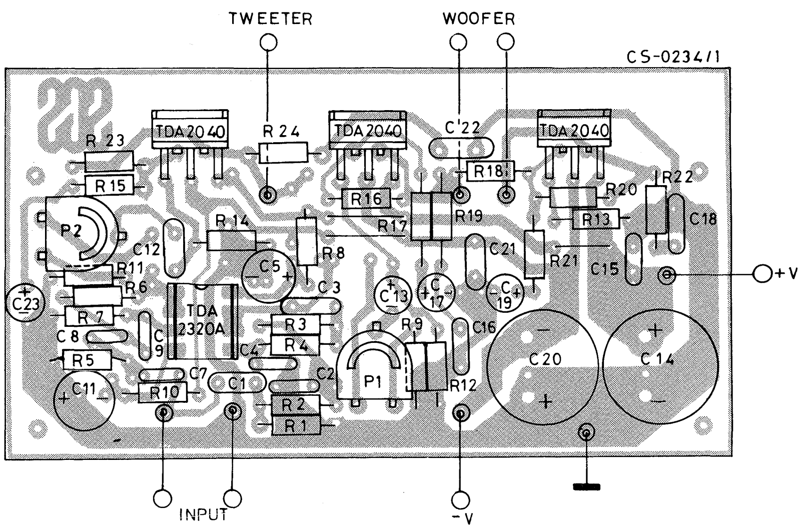


Fig. 17 - P.C. board and component layout of the circuit of fig. 16 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 18 - Frequency response

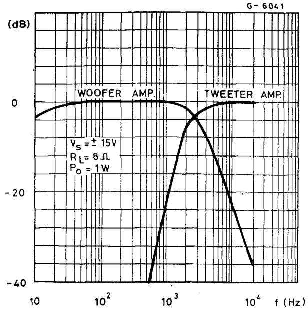
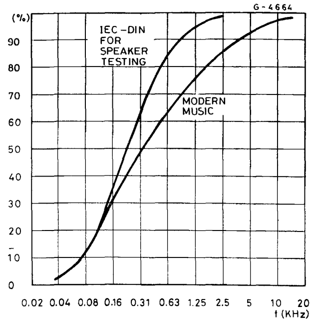


Fig. 19 - Power distribution vs. frequency



Multiway speaker systems and active boxes

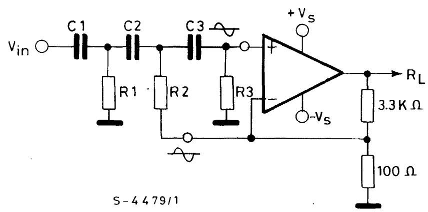
Multiway loudspeaker systems provide the best possible acoustic performance since each loudspeaker is specially designed and optimized to handle a limited range of frequencies. Commonly, these loudspeaker systems divide the audio spectrum into two, three or four bands.

To maintain a flat frequency response over the Hi-Fi audio range the bands covered by each loudspeaker must overlap slightly. Imbalance between the loudspeakers produces unacceptable results therefore it is important to ensure that each unit generates the correct amount of acoustic energy for its segment of the audio spectrum. In this respect it is also important to know the energy distribution of the music spectrum determine the cutoff frequencies of the crossover filters (see Fig. 19). As an example, a 100W three-way system with crossover frequencies of 400Hz and 3KHz would require 50W for the woofer, 35W for the midrange unit and 15W for the tweeter.

Both active and passive filters can be used for crossovers but today active filters cost significantly less than a good passive filter using air-cored inductors and non-electrolytic capacitors. In addition, active filters do not suffer from the typical defects of passive filters:

- power loss
- increased impedance seen by the loudspeaker (lower damping)
- difficulty of precise design due to variable loudspeaker impedance

Fig. 20 - Active power filter



Obviously, active crossovers can only be used if a power amplifier is provided for each drive unit. This makes it particularly interesting and economically sound to use monolithic power amplifiers. In some applications, complex filters are not really necessary and simple RC low-pass and high-pass networks (6dB/octave) can be recommended.

The results obtained are excellent because this is the best type of audio filter and the only one free from phase and transient distortion.

The rather poor out of band attenuation of single RC filters means that the loudspeaker must operate linearly well beyond the crossover frequency to avoid distortion.

A more effective solution, named "Active Power Filter" by SGS is shown in Fig. 20.

The proposed circuit can realize combined power amplifiers and 12dB/octave or 18dB/octave high-pass or low-pass filters.

APPLICATION INFORMATION (continued)

In practice, at the input pins of the amplifier two equal and in-phase voltages are available, as required for the active filter operation.
The impedance at the pin (-) is of the order of 100Ω, while that of the pin (+) is very high, which is also what was wanted.

The component values calculated for $f_c = 900Hz$ using a Bessel 3rd order Sallen and Key structure are:

C1 = C2 = C3	R1	R2	R3
22nF	8.2KΩ	5.6KΩ	33KΩ

In the block diagram of Fig. 21 is represented an active loudspeaker system completely realized using power integrated circuit, rather than the traditional discrete transistors on hybrids, very high quality is obtained by driving the audio spectrum into three bands using active crossovers (TDA2320A) and a separate amplifier and loudspeakers for each band.
A modern subwoofer/midrange/tweeter solution is used.

SHORT CIRCUIT PROTECTION

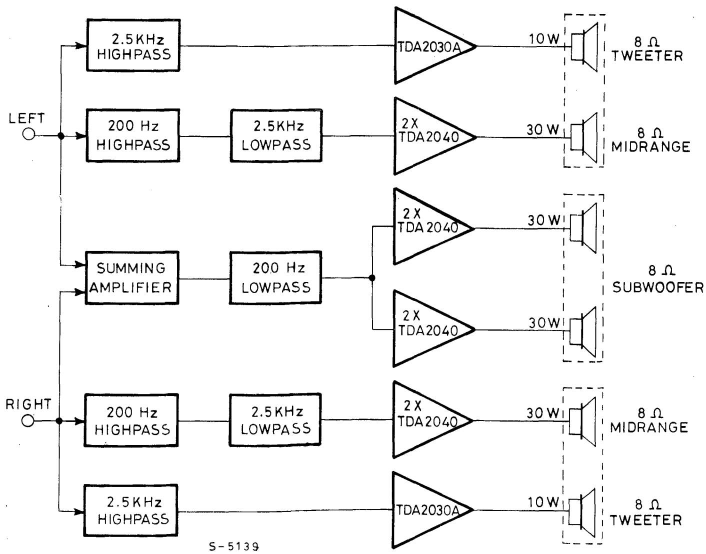
The TDA2040 has an original circuit which limits the current of the output transistors. This function can be considered as being peak power limiting rather than simple current limiting. The TDA2030A is thus protected against temporary overloads or short circuit. Should the short circuit exist for a longer time the thermal shut down protection keeps the junction temperature within safe limits.

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increase up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

Fig. 21 - High power active loudspeaker system using TDA2030A and TDA2040



PRACTICAL CONSIDERATION

Printed circuit board

The layout shown in Fig. 11 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the gorund return of the output in which a high current flows.

Assembly suggestion

No electrical isolation is needed between the package and the heatsink with single supply voltage configuration.

Application suggestions

The recommended values of the components are those shown on application circuit of Fig. 10. Different values can be used. The following table can help the designer.

Component	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22KΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R2	680Ω	Closed loop gain setting	Decrease of gain (*)	Increase of gain
R3	22KΩ	Closed loop gain setting	Increase of gain	Decrease of gain (*)
R4	4.7Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
C1	1μF	Input DC decoupling		Increase of low frequencies cutoff
C2	22μF	Inverting DC decoupling		Increase of low frequencies cutoff
C3, C4	0.1μF	Supply voltage bypass		Danger of oscillation
C5, C6	220μF	Supply voltage bypass		Danger of oscillation
C7	0.1μF	Frequency stability		Danger of oscillation

(*) The value of closed loop gain must be higher than 24dB.

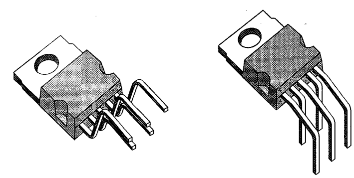
SGS-THOMSON MICROELECTRONICS

TDA2050

32W Hi-Fi AUDIO POWER AMPLIFIER

PRELIMINARY DATA

- HIGH OUTPUT POWER (50W MUSIC POWER IEC 268.3 RULES)
- HIGH OPERATING SUPPLY VOLTAGE (50V)
- SINGLE OR SPLIT SUPPLY OPERATIONS
- VERY LOW DISTORTION
- SHORT CIRCUIT PROTECTION (OUT TO GND)
- THERMAL SHUTDOWN



Pentawatt V **Pentawatt H**

ORDERING NUMBERS:
TDA2050V TDA2050H

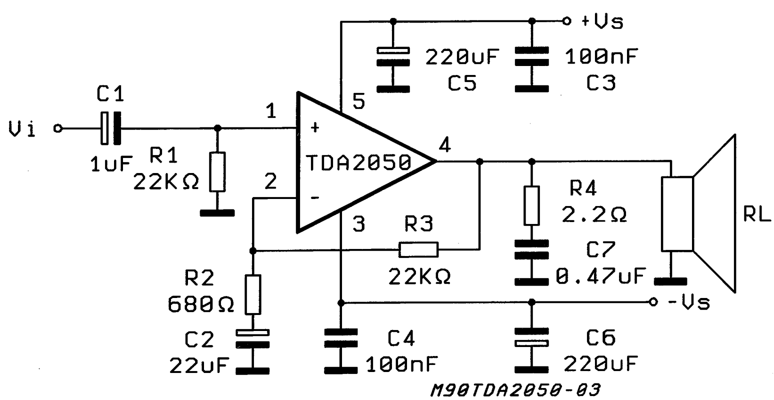
DESCRIPTION

The TDA 2050 is a monolithic integrated circuit in Pentawatt package, intended for use as an audio class AB audio amplifier. Thanks to its high power capability the TDA2050 is able to provide up to 35W true rms power into 4 ohm load @ THD = 10%, V_S = ±18V, f = 1KHz and up to 32W into 8ohm load @ THD = 10%, V_S = ±22V, f = 1KHz.

Moreover, the TDA 2050 delivers typically 50W music power into 4 ohm load over 1 sec at V_S= 22.5V, f = 1KHz.

The high power and very low harmonic and cross-over distortion (THD = 0.05% typ, @ V_S = ±22V, P_O = 0.1 to 15W, R_L=8ohm, f = 100Hz to 15KHz) make the device most suitable for both HiFi and high class TV sets.

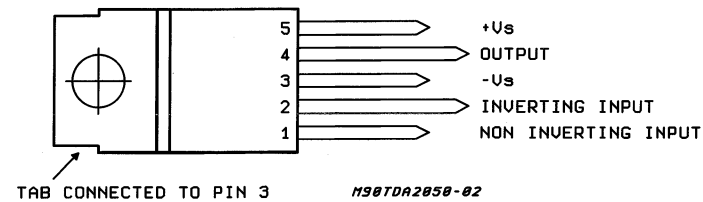
TEST AND APPLICATION CIRCUIT



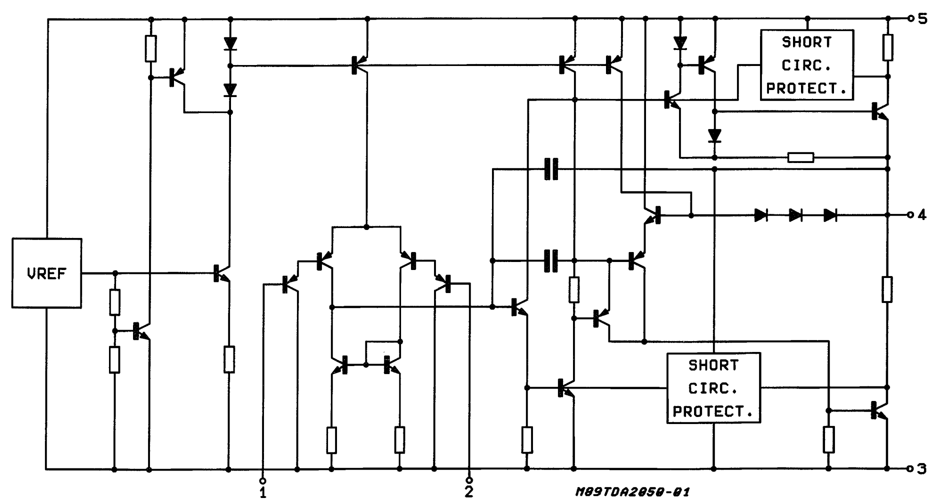
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	±25	V
V_i	Input Voltage	V_S	
V_i	Differential Input Voltage	±15	V
I_O	Output Peak Current (internally limited)	5	A
P_{tot}	Power Dissipation T_{CASE} = 75°C	25	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance junction-case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the Test Circuit, V_S = ±18V, T_{amb} = 25°C, f = 1 kHz; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range		±4.5		±25	V
I_d	Quiescent Drain Current	V_S = ±4.5V V_S = ±25V		30 55	50 90	mA mA
I_b	Input Bias Current	V_S = ±22V		0.1	0.5	µA
V_{OS}	Input Offset Voltage	V_S = ±22V			±15	mV
I_{OS}	Input Offset Current	V_S = ±22V			±200	nA
P_O	RMS Output Power	d = 0.5% R_L = 4Ω R_L = 8Ω V_S = ±22V R_L = 8Ω	 24 22	 28 18 25		 W W W
		d = 10% R_L = 4Ω R_L = 8Ω V_S = ±22V R_L = 8Ω		 35 22 32		 W W W
	Music Power IEC268.3 RULES	d = 10%; T = 1s V_S = ±22.5V; R_L = 4Ω		 50		 W
d	Total Harmonic Distortion	R_L = 4Ω f = 1kHz, P_O = 0.1 to 24W f = 100Hz to 10kHz, P_O = 0.1 to 18W		 0.03	 0.5 0.5	 % %
		V_S = ±22V R_L = 8Ω f = 1kHz, P_O = 0.1 to 20W f = 100Hz to 10kHz, P_O = 0.1 to 15W		 0.02	 0.5	 % %
SR	Slew Rate		5	8		V/µs
G_V	Open Loop Voltage Gain			80		dB
G_V	Closed Loop Voltage Gain		30	30.5	31	dB
BW	Power Bandwidth (-3dB)	R_L = 4Ω V_i = 200mV	20 to 80,000			Hz
e_N	Total Input Noise	curve A B = 22Hz to 22kHz		4 5	 10	µV µV
R_i	Input Resistance (pin 1)		500			kΩ
SVR	Supply Voltage Rejection	R_s = 22kΩ; f = 100Hz; V_{ripple} = 0.5Vrms		 45		 dB
η	Efficiency	P_O = 28W; R_L = 4Ω		65		%
		P_O = 25W; R_L = 8Ω; V_S = ±22V		 67		 %
T_{sd-j}	Thermal Shut-down Junction Temperature			150		°C

Figure 1: Split Supply Typical Application Circuit

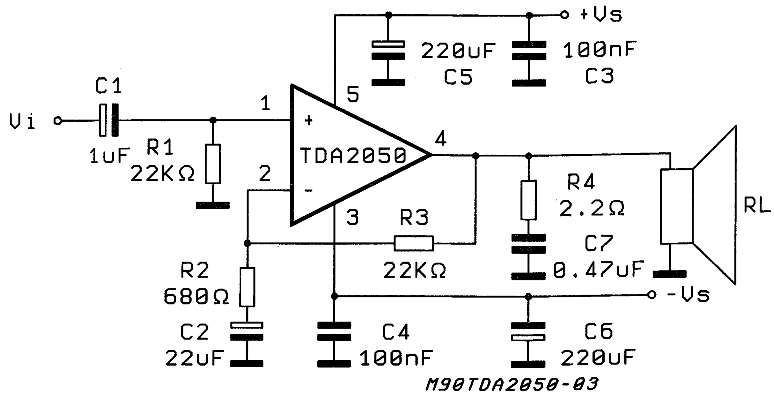
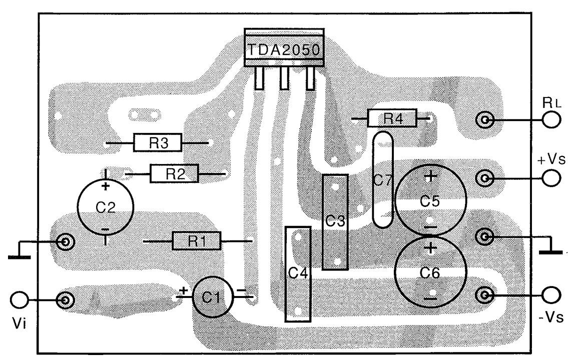


Figure 2: P.C. Board and Components Layout of the Circuit of Fig. 1 (1:1)



SPLIT SUPPLY APPLICATION SUGGESTIONS

The recommended values of the external components are those shown on the application circuit of fig. 2. Different values can be used. The following table can help the designer.

Component	Recommended Value	Purpose	Larger than Recommended Value	Smaller than Recommended Value
R1	22kΩ	Input Impedance	Increase of Input Impedance	Decrease of Input Impedance
R2	680Ω	Feedback Resistor	Decrease of Gain (*)	Increase of Gain
R3	22kΩ		Increase of Gain	Decrease of Gain (*)
R4	2.2Ω	Frequency Stability	Danger of Oscillations	
C1	1µF	Input Decoupling DC		Higher Low-frequency cut-off
C2	22µF	Inverting Input DC Decoupling	Increase of Switch ON/OFF Noise	Higher Low-frequency cut-off
C3 C4	100nF	Supply Voltage Bypass		Danger of Oscillations
C5 C6	220µF	Supply Voltage Bypass		Danger of Oscillations
C7	0.47µF	Frequency Stability		Danger of Oscillations

(*) The gain must be higher than 24dB

PRINTED CIRCUIT BOARD

The layout shown in fig. 2 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

Figure 3: Single Supply Typical Application Circuit

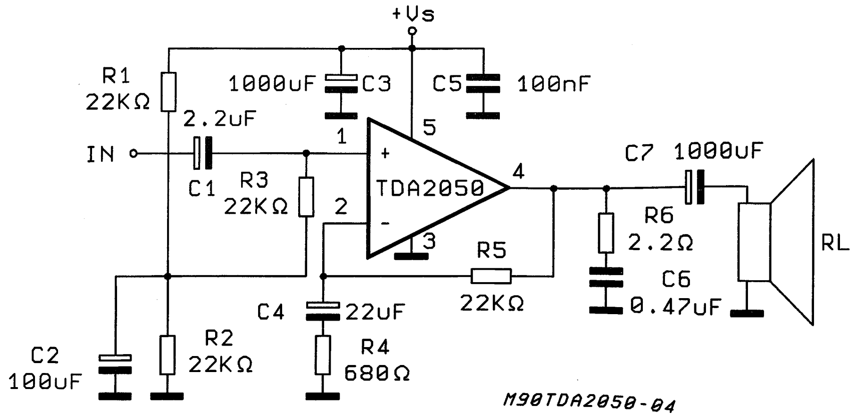
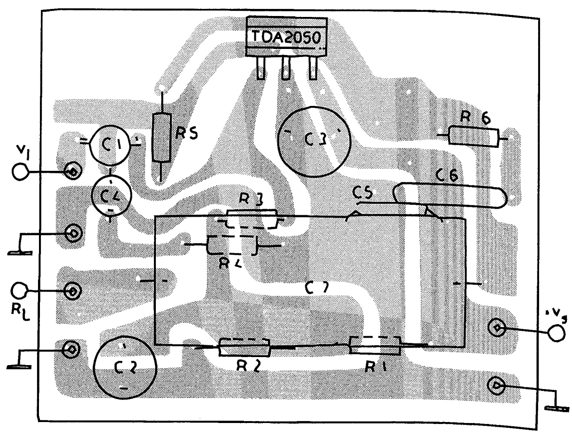


Figure 4: P.C. Board and Components Layout of the Circuit of Fig. 3 (1:1)



SINGLE SUPPLY APPLICATION SUGGESTIONS

The recommended values of the external components are those shown on the application circuit of fig. 3. Different values can be used. The following table can help the designer.

Component	Recommended Value	Purpose	Larger than Recommended Value	Smaller than Recommended Value
R1, R2, R3	22kΩ	Biasing Resistor		
R4	22kΩ	Feedback Resistors	Increase of Gain	Decrease of Gain (*)
R5	680Ω		Decrease of Gain (*)	Increase of Gain
R6	2.2Ω	Frequency Stability	Danger of Oscillations	
C1	2.2µF	Input Decoupling DC		Higher Low-frequency cut-off
C2	100µF	Supply Voltage Rejection	Worse Turn-off Transient Worse Turn-on Delay	
C3	1000µF	Supply Voltage Bypass		Danger of Oscillations Worse of Turn-off Transient
C4	22µF	Inverting Input DC Decoupling	Increase of Switching ON/OFF	Higher Low-frequency cut-off
C5	100nF	Supply Voltage Bypass		Danger of Oscillations
C6	0.47µF	Frequency Stability		Danger of Oscillations
C7	1000µF	Output DC Decoupling		Higher Low-frequency cut-off

(*) The gain must be higher than 24dB

NOTE
If the supply voltage is lower than 40V and the load is 8ohm (or more) a lower value of C2 can be used (i.e. 22µF).

C7 can be larger than 1000uF only if the supply voltage does not exceed 40V.

TYPICAL CHARACTERISTICS (Split Supply Test Circuit unless otherwise specified)

Figure 5: Output Power vs. Supply Voltage

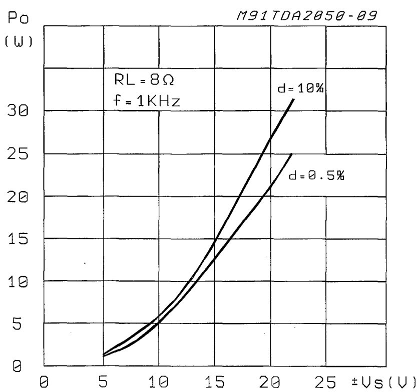


Figure 6: Distortion vs. Output Power

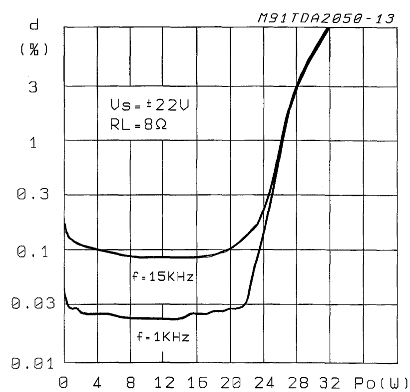


Figure 7: Output Power vs. Supply Voltage

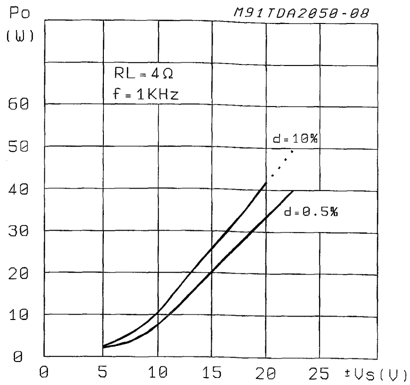


Figure 8: Distortion vs. Output Power

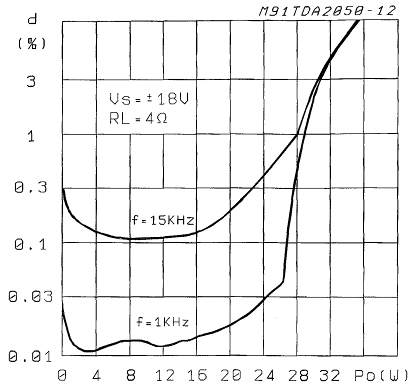


Figure. 9: Distortion vs. Frequency

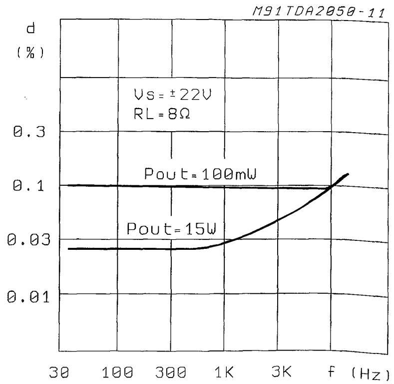


Figure 10: Distortion vs. Frequency

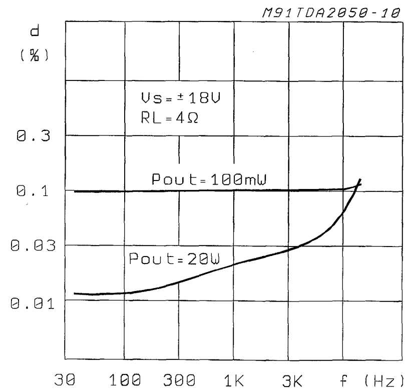


Figure 11: Quiescent Current vs. Supply Voltage

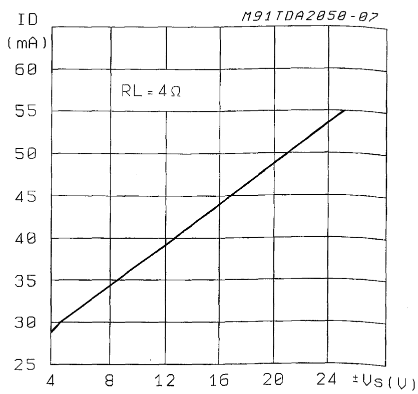


Figure 12: Supply Voltage Rejection vs. Frequency

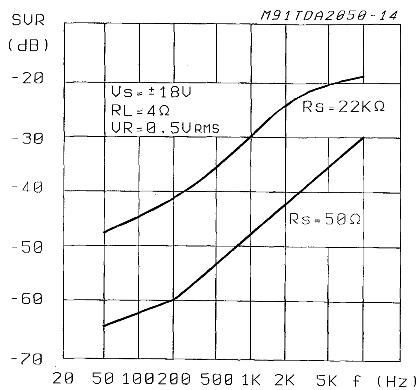


Figure 13: Supply Voltage Rejection vs. Frequency (Single supply) for Different values of C2 (circuit of fig. 3)

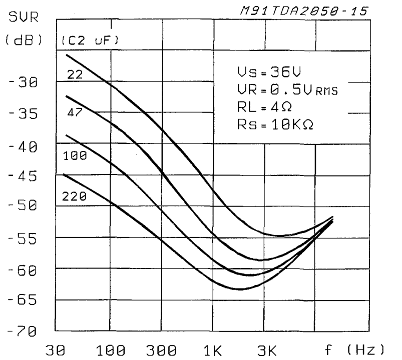


Figure 14: Supply Voltage Rejection vs. Frequency (Single supply) for Different values of C2 (circuit of fig. 3)

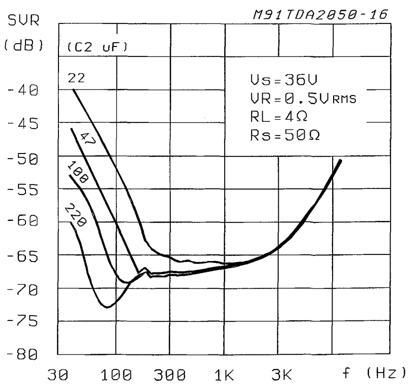


Figure 15: Total Power Dissipation and Efficiency vs. Output Power

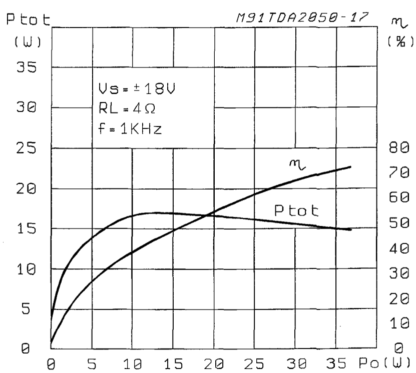
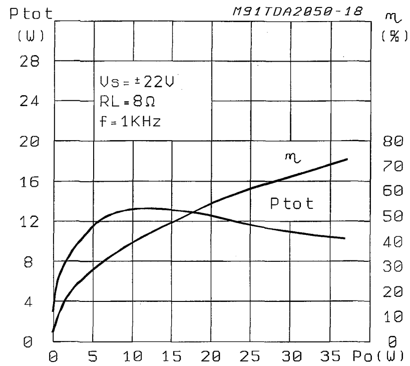


Figure 16: Total Power Dissipation and Efficiency vs. Output Power



SHORT CIRCUIT PROTECTION

The TDA 2050 has an original circuit which limits the current of the output transistors. The maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area. This function can therefore be considered as being peak power limiting rather than simple current limiting.

It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

THERMAL SHUTDOWN

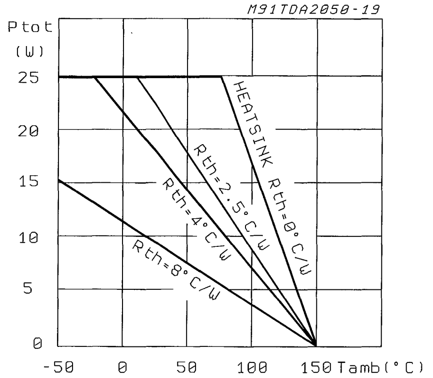
The presence of a thermal limiting circuit offers the following advantages:

1)An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily tolerated since the Tj cannot be higher than 150°C.

2)The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150°C, the thermal shutdown simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the thermal resistance junction-ambient. Fig. 17 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Figure 17: Maximum Allowable Power Dissipation vs. Ambient Temperature



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

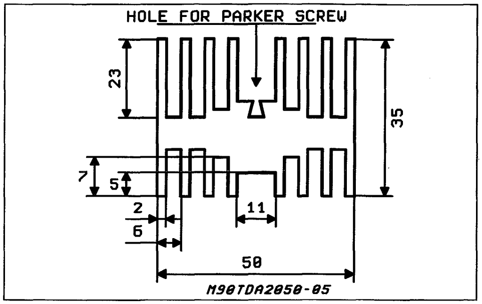
Thanks to the PENTAWATT package, the heatsink mounting operation is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces. Fig. 18 shows an example of heatsink.

Dimension suggestion

The following table shows the length that the heatsink in fig. 18 must have for several values of Ptot and Rth.

P_{tot} (W)	12	8	6
Lenght of heatsink (mm)	60	40	30
R_{th} of heatsink (°C/W)	4.2	6.2	8.3

Figure 18: Example of heat-sink



APPENDIX A

A.1 - MUSIC POWER CONCEPT

MUSIC POWER is (according to the IEC clauses n.268-3 of Jan 83) the maximum power which the amplifier is capable of producing across the rated load resistance (regardless of non linearity) 1 sec after the application of a sinusoidal input signal of frequency 1 KHz.

According to this definition our method of measurement comprises the following steps:

- Set the voltage supply at the maximum operating value;
- Apply a input signal in the form of a 1KHz tone burst of 1 sec duration: the repetition period of the signal pulses is 60 sec;
- The output voltage is measured 1 sec from the start of the pulse;
- Increase the input voltage until the output signal shows a THD=10%;
- The music power is then V^2_{out} /RL, where Vout is the output voltage measured in the condition of point 4 and RL is the rated load impedance;

The target of this method is to avoid excessive dissipation in the amplifier.

A.2 - INSTANTANEOUS POWER

Another power measurement (MAXIMUM INSTANTANEOUS OUTPUT POWER) was proposed by IEC in 1988 (IEC publication 268-3 subclause 19.A).

We give here only a brief extract of the concept, and a circuit useful for the measurement.

The supply voltage is set at the maximum operating value.

The test signal consists of a sinusoidal signal whose frequency is 20 Hz, to which are added alternate positive and negative pulses of 50 µs duration and 500 Hz repetition rate. The amplitude of the 20 Hz signal is chosen to drive the amplifier to its voltage clipping limits, while the amplitude of the pulses takes the amplifier alternately into its current-overload limits.

A circuit for generating the test signal is given in fig. 19.

The load network consists of a 40 µF capacitor, in series with a 1 ohm resistor. The capacitor limits the current due to the 20 Hz signal to a low value, whereas for he short pulses the effective load impedance is of the order of 1 ohm, and a high output current is produced.

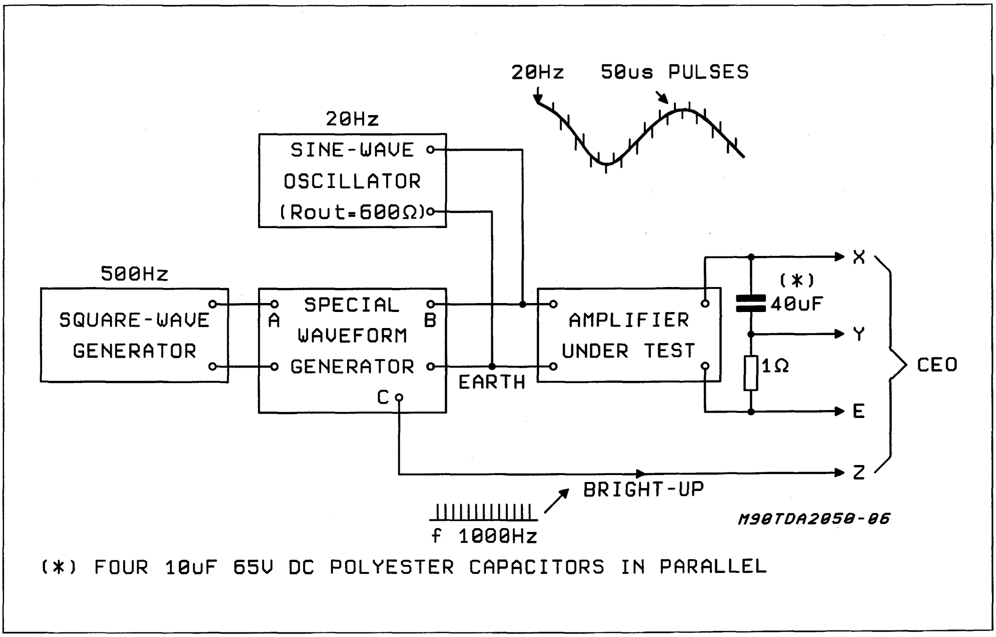
Using this signal and load network the measurement may be made without causing excessive dissipation in the amplifier. The dissipation in the 1 ohm resistor is much lower than a rated output power of the amplifier, because the duty-cycle of the high output current is low.

By feeding the amplifier output voltage to the X-plates of an oscilloscope, and the voltage across the 1 ohm resistor (representing the output current) to the Y=plates, it is possible to read on the display the value of the maximum instantaneous output power.

The result of this test applied at the TDA 2050 is:

PEAK POWER = 100W typ

Figure 19: Test circuit for peak power measurement



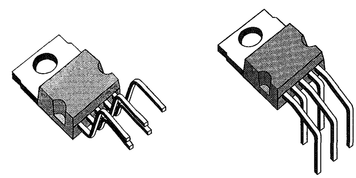
SGS-THOMSON MICROELECTRONICS

TDA2051

40W Hi-Fi AUDIO POWER AMPLIFIER

PRODUCT PREVIEW

- HIGH OUTPUT POWER (60W/4Ω MUSIC POWER IEC 268.3 RULES)
- HIGH OPERATING SUPPLY VOLTAGE (±25V)
- SINGLE OR SPLIT SUPPLY OPERATIONS
- VERY LOW DISTORTION
- SHORT CIRCUIT PROTECTION (OUT TO GND)
- THERMAL SHUTDOWN



Pentawatt V	Pentawatt H
ORDERING NUMBERS:	
TDA2051V	TDA2051H

DESCRIPTION

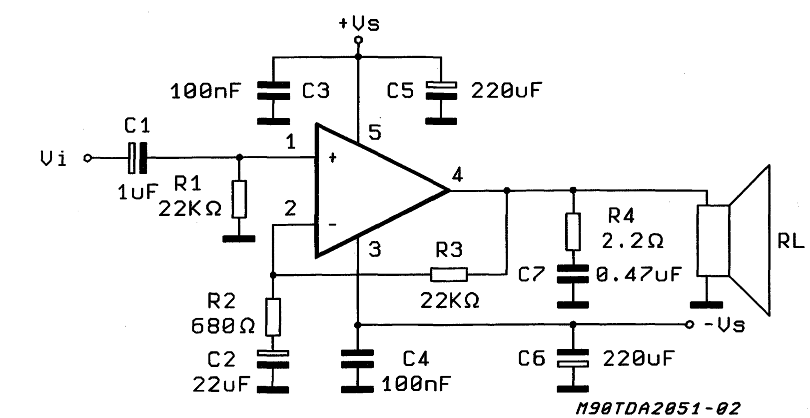
The TDA 2051 is a monolithic integrated circuit in Pentawatt package, intended for use as an audio class AB amplifier. Thanks to its high power capability the TDA2051 is able to provide up to 40W typ. into 4 ohm load @ THD = 10%, V_S = ±18V, f = 1KHz and up to 33W into 8ohm load @ THD = 10%, V_S = ±22V, f = 1KHz.

Moreover, the TDA 2051 delivers typically 60W music power into 4 ohm load over 1 sec at V_S= 22.5V, f = 1KHz.

The very low harmonic and crossover distortion performances make the device the most suitable for Hi-Fi field application.

The low external component count and the good power dissipation capability of the Pentawatt Package allowes stereo sets reduced in cost/space due to both, low number of external parts and reduced heatsink area due to optimized heatsink efficiency.

TEST AND APPLICATION CIRCUIT

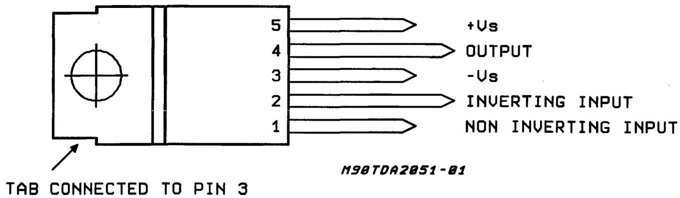


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

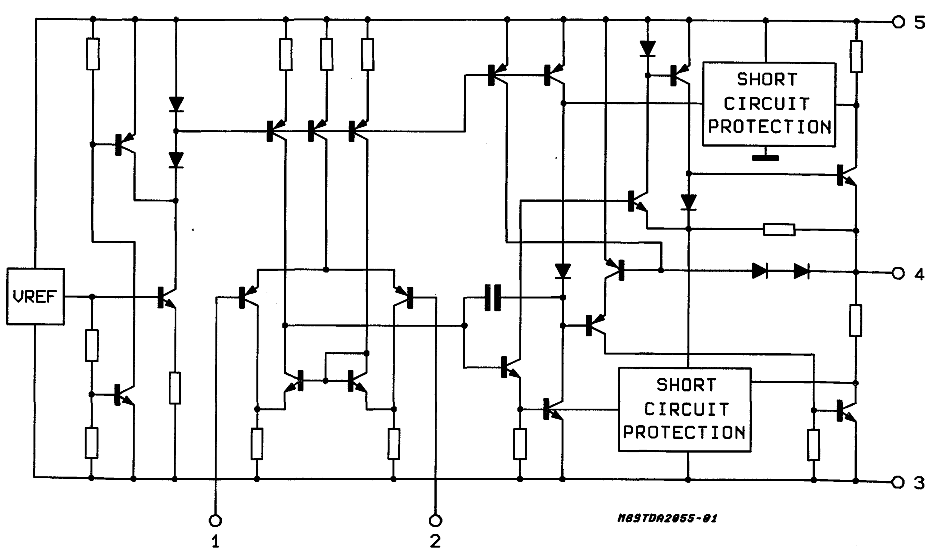
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	±25	V
V_i	Input Voltage	V_S	
V_i	Differential Input Voltage	±15	V
I_O	Output Peak Current (internally limited)	6	A
P_{tot}	Power Dissipation T_{CASE} = 70°C	36	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance junction-case	Max	2.5	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the Test Circuit, V_S = ±18V, T_{amb} = 25°C, f = 1 kHz; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range		±5		±25	V
I_d	Quiescent Drain Current	V_S = ±4.5V V_S = ±25V		50 100		mA mA
I_b	Input Bias Current	V_S = ±22V		0.3		µA
V_{OS}	Input Offset Voltage	V_S = ±22V			±20	mV
I_{OS}	Input Offset Current	V_S = ±22V			±200	nA
P_O	RMS Output Power	d = 10%; rms values R_L = 4Ω R_L = 8Ω V_S = ±22V R_L = 8Ω		 40 22 33		 W W W
		d = 1%; rms values R_L = 4Ω R_L = 8Ω V_S = ±22V R_L = 8Ω		 30 17 25		 W W W
	Music Power IEC268.3 RULES	d = 10%; T = 1s V_S = ±22.5V; R_L = 4Ω		 60		 W
d	Total Harmonic Distortion	R_L = 4Ω; P_O = 0.1 to 20W f = 1kHz, f = 40Hz to 15kHz		 0.02 0.1		 % %
		V_S = ±22V R_L = 8Ω; P_O = 0.1 to 20W f = 1kHz f = 40Hz to 15kHz		 0.02 0.1		 % %
SR	Slew Rate			6		V/µs
G_V	Open Loop Voltage Gain			80		dB
G_V	Closed Loop Voltage Gain		30	30.5	31	dB
e_N	Total Input Noise	B = curve A B = 22Hz to 22kHz		4 5	 10	µV µV
R_i	Input Resistance (pin 1)		500			kΩ
SVR	Supply Voltage Rejection	R_L = 4Ω G_V = 30dB R_s = 22kΩ; f = 100Hz; V_{ripple} = 0.5Vrms		 45		 dB
η	Efficiency	P_O = 30W; R_L = 4Ω		65		%
		P_O = 25W; R_L = 8Ω; V_S = ±22V		 67		 %
T_{sd-j}	Thermal Shut-down Junction Temperature			160		°C

Figure 1: Split Supply Typical Application Circuit

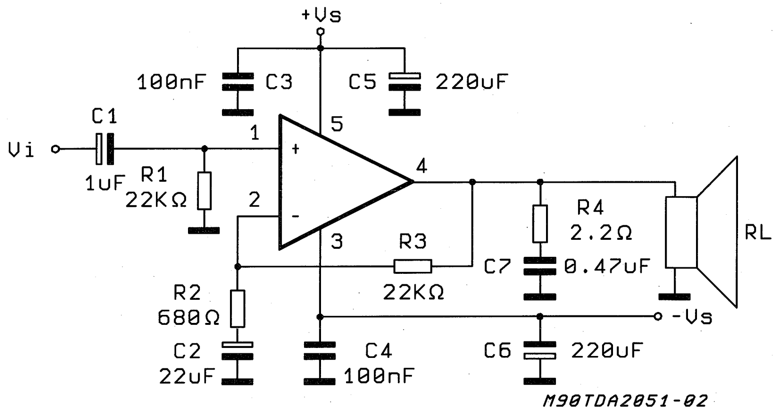
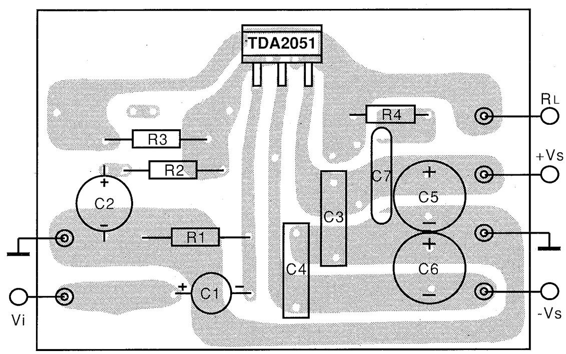


Figure 2: P.C. Board and Components Layout of the Circuit of Fig. 1 (1:1)



SPLIT SUPPLY APPLICATION SUGGESTIONS

The recommended values of the external components are those shown on the application circuit of fig. 2. Different values can be used. The following table can help the designer.

Component	Recommended Value	Purpose	Larger than Recommended Value	Smaller than Recommended Value
R1	22kΩ	Input Impedance	Increase of Input Impedance	Decrease of Input Impedance
R2	680Ω	Feedback Resistor	Decrease of Gain (*)	Increase of Gain
R3	22kΩ		Increase of Gain	Decrease of Gain (*)
R4	2.2Ω	Frequency Stability	Danger of Oscillations	
C1	1µF	Input Decoupling DC		Higher Low-frequency cut-off
C2	22µF	Inverting Input DC Decoupling	Increase of Switch ON/OFF Noise	Higher Low-frequency cut-off
C3 C4	100nF	Supply Voltage Bypass		Danger of Oscillations
C5 C6	220µF	Supply Voltage Bypass		Danger of Oscillations
C7	0.47µF	Frequency Stability		Danger of Oscillations

(*) The gain must be higher than 24dB

PRINTED CIRCUIT BOARD

The layout shown in fig. 2 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

TYPICAL CHARACTERISTICS (Split Supply Test Circuit unless otherwise specified)

Figure 3: Output Power vs. Supply Voltage

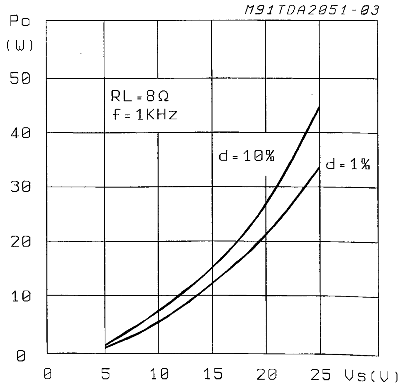


Figure 4: Distortion vs. Output Power

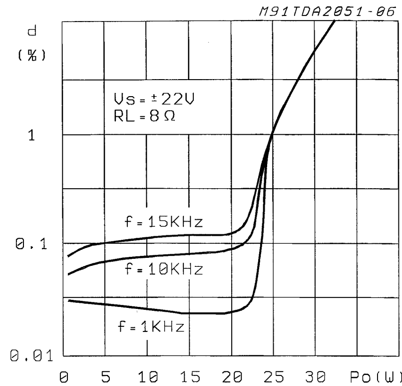


Figure 5: Output Power vs. Supply Voltage

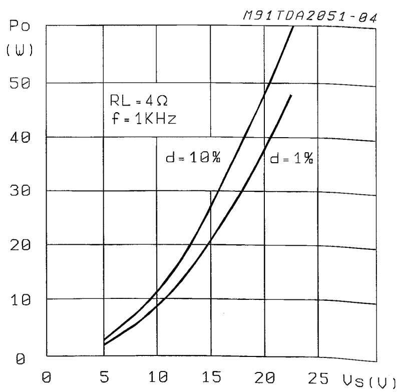


Figure 6: Distortion vs. Output Power

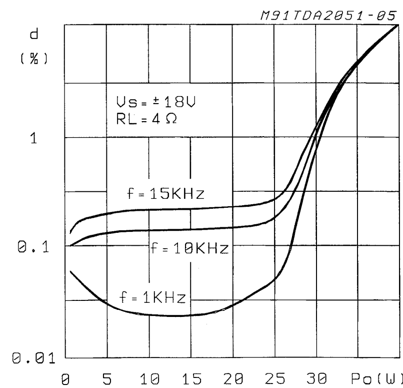


Figure 7: Total Power Dissipation and Efficiency vs. Output Power

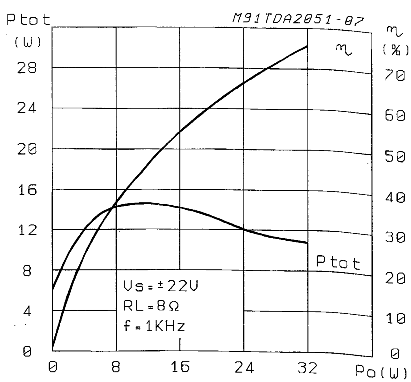
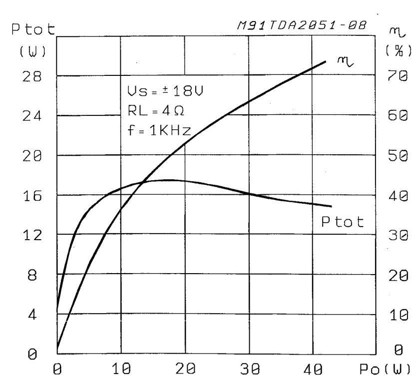


Figure 8: Total Power Dissipation and Efficiency vs. Output Power



SHORT CIRCUIT PROTECTION

The TDA 2051 has an original circuit which limits the current of the output transistors. The maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area. This function can therefore be considered as being peak power limiting rather than simple current limiting.

It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

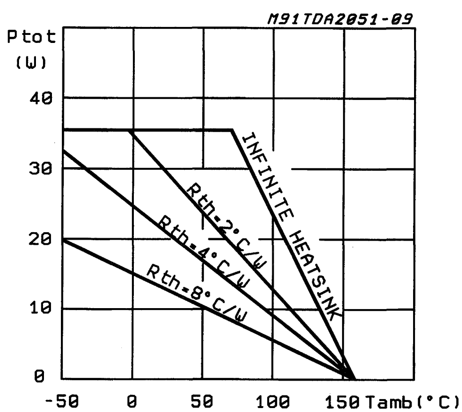
THERMAL SHUTDOWN

The presence of a thermal limiting circuit offers the following advantages:

1)An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily tolerated since the Tj cannot be higher than 160°C.

2)The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 160°C, the thermal shutdown simply reduces the power dissipation and the current consumption.

Figure 9: Maximum Allowable Power Dissipation vs. Ambient Temperature



The maximum allowable power dissipation depends upon the thermal resistance junction-ambient. Fig. 9 shows this dissipable power as a function of ambient temperature for different thermal resistance.

MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

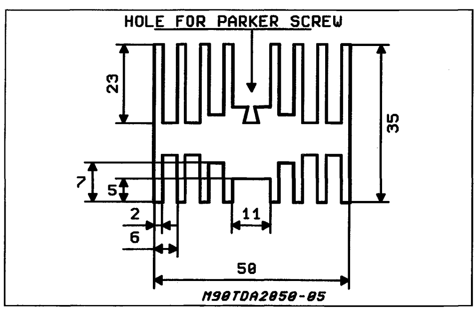
Thanks to the PENTAWATT package, the heatsink mounting operation is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces. Fig. 18 shows an example of heatsink.

Dimension suggestion

The following table shows the length that the heatsink in fig. 10 must have for several values of Ptot and Rth.

P_{tot} (W)	12	8	6
Lenght of heatsink (mm)	60	40	30
R_{th} of heatsink (°C/W)	4.2	6.2	8.3

Figure 10: Example of heat-sink



APPENDIX A

A.1 - MUSIC POWER CONCEPT

MUSIC POWER is (according to the IEC clauses n.268-3 of Jan 83) the maximum power which the amplifier is capable of producing across the rated load resistance (regardless of non linearity) 1 sec after the application of a sinusoidal input signal of frequency 1 KHz.

According to this definition our method of measurement comprises the following steps:

- Set the voltage supply at the maximum operating value -10%;
- Apply a input signal in the form of a 1KHz tone burst of 1 sec duration: the repetition period of the signal pulses is 60 sec;
- The output voltage is measured 1 sec from the start of the pulse;
- Increase the input voltage until the output signal shows a THD=10%;
- The music power is then V^2_{out} /RL, where Vout is the output voltage measured in the condition of point 4 and RL is the rated load impedance;

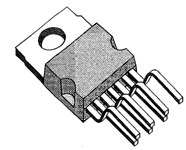
The target of this method is to avoid excessive dissipation in the amplifier.

TDA2052

60W Hi-Fi AUDIO POWER AMPLIFIER WITH MUTE / STAND-BY

PRODUCT PREVIEW

- SUPPLY VOLTAGE RANGE UP TO ±25V
- SPLIT SUPPLY OPERATION
- HIGH OUTPUT POWER (UP TO 60W MUSIC POWER)
- LOW DISTORTION
- MUTE/STAND-BY FUNCTION
- NO SWITCH ON/OFF NOISE
- AC SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN



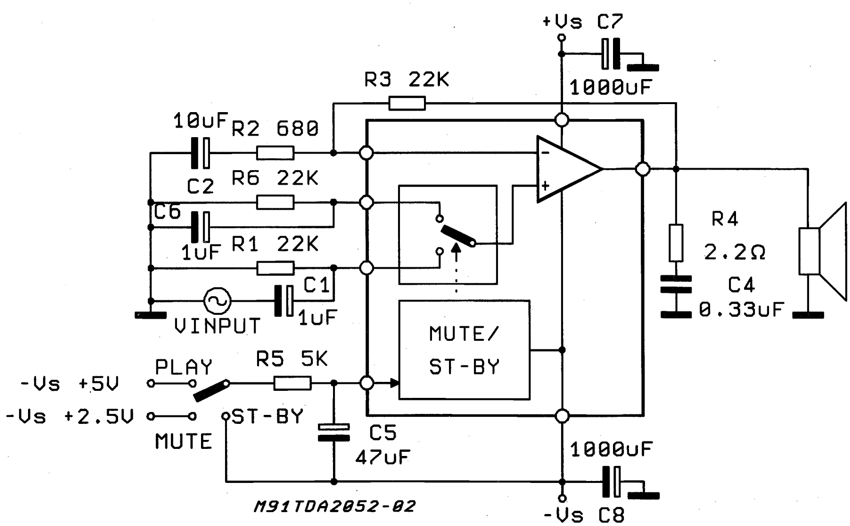
Heptawatt
ORDERING NUMBER: TDA2052

DESCRIPTION

The TDA2052 is a monolithic integrated circuit in Heptawatt package, intended for use as audio class AB amplifier in TV or Hi-Fi field application. Thanks to the wide voltage range and to the high out current capability it's able to supply the highest power into booth 4Ω and 8Ω loads even in presence of poor supply regulation.

The built in muting/Stand-by function simplifies the remote operations avoiding also switching on-off noises.

TEST AND APPLICATION CIRCUIT

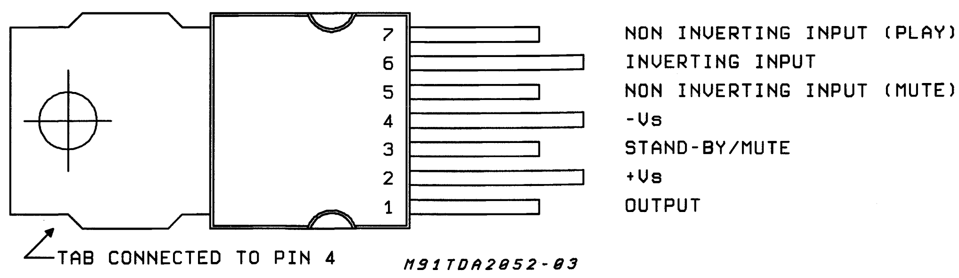


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

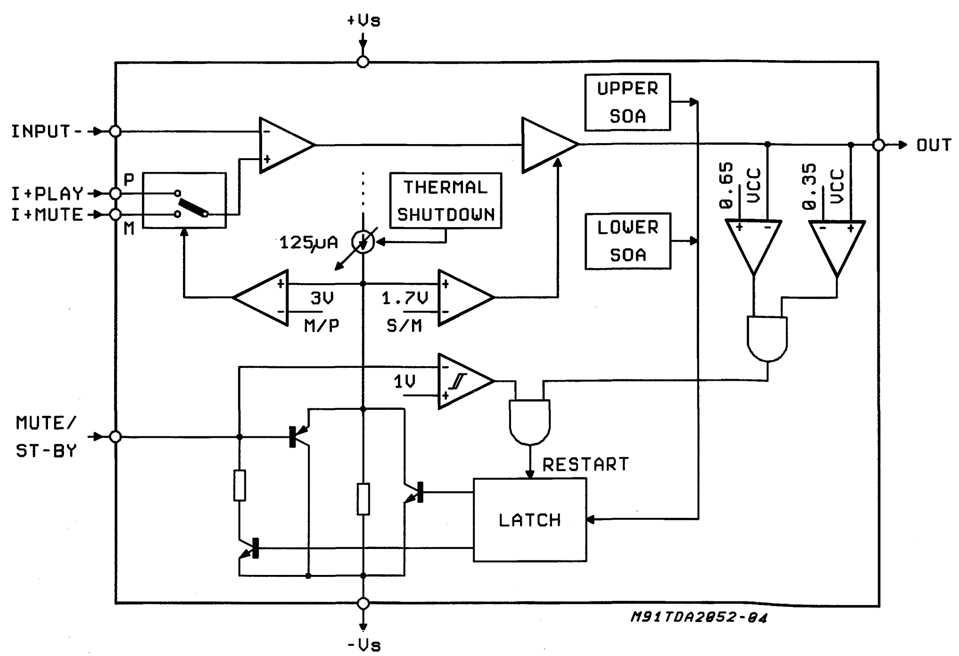
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	±25	V
I_O	Output Peak Current (internally limited)	6	A
P_{tot}	Power Dissipation T_{case} = 70°C	30	W
T_{op}	Operating Temperature Range	0 to +70	°C
T_{stg}, T_j	Storage and Junction Temperature	-40 to +150	°C

PIN CONNECTION (Top view)



BLOCK DIAGRAM



THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	2.5	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_S \pm 18V$; f = 1KHz; T_{amb} = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Range		±6		±25	V
I_d	Total Quiescent Drain Current	V_S = ±25V		50	100	mA
I_b	Input Bias Current			0.3		μA
V_{IS}	Input Offset Voltage				±20	mV
I_{IS}	Input Offset Current				±200	nA
P_O	Music Output Power	IEC2683 Rules (t = 1s) V_S = ± 22.5, R_L = 4Ω, d = 10%		60		W
P_O	Output Power	d = 10% RL = 4Ω R_L = 8Ω V_S = ±22V, R_L = 8Ω		 40 22 30		 W W W
		d = 1% R_L = 4Ω R_L = 8Ω V_S = ±22V, R_L = 8Ω		 30 17 24		 W W W
d	Total Harmonic Distortion	P_O = 0.1 to 20W; R_L = 4Ω f = 40Hz to 15KHz P_O = 0.1 to 12W; R_L = 4Ω f = 40Hz to 15KHz		 0.1 0.1		 % %
SR	Slew Rate			6		V/μs
G_V	Open Loop Voltage Gain			80		dB
G_V	Closed Loop Voltage Gain			30		dB
e_N	Total Input Noise	A Curve f = 20Hz to 20KHz		5	 10	μV μV
R_i	Input Resistance		500			KΩ
SVR	Supply Voltage Rejection	f = 100Hz		50		dB
T_S	Thermal Shutdown			150		°C

MUTE/STAND-BY FUNCTION

$VT_{ST\text{-}BY}$	Stand-by - Mute Threshold			1.7		V
VT_{MUTE}	Mute Threshold			3		V
$Id_{ST\text{-}BY}$	Quiescent Current @ Stand-by			1	3	mA
$ATT_{ST\text{-}BY}$	Stand-by Attenuation			90		dB
ATT_{MUTE}	Mute Attenuation		60	70		dB

SGS-THOMSON MICROELECTRONICS

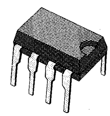
TDA2320A

MINIDIP STEREO PREAMPLIFIER

- WIDE SUPPLY VOLTAGE RANGE (3 TO 36V)
- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW CURRENT CONSUMPTION (0.8mA)
- VERY LOW DISTORTION
- NO POP-NOISE
- SHORT CIRCUIT PROTECTION

The TDA2320A is a stereo class A preamplifier intended for application in portable cassette players and high quality audio systems.

The TDA2320A is a monolithic integrated circuit a 8 lead minidip.



Minidip Plastic

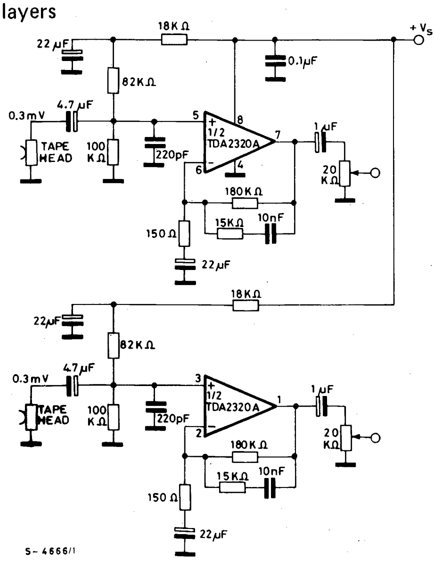
ORDERING NUMBER: TDA 2320A

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	36	V
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	400	mW
$T_{stg, j}$	Storage and junction temperature	-40 to 150	°C

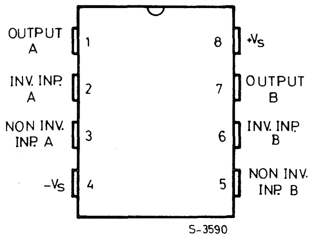
TYPICAL APPLICATION:

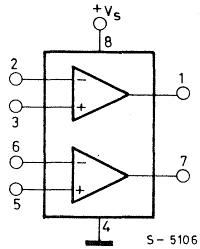
Stereo preamplifier for cassette players



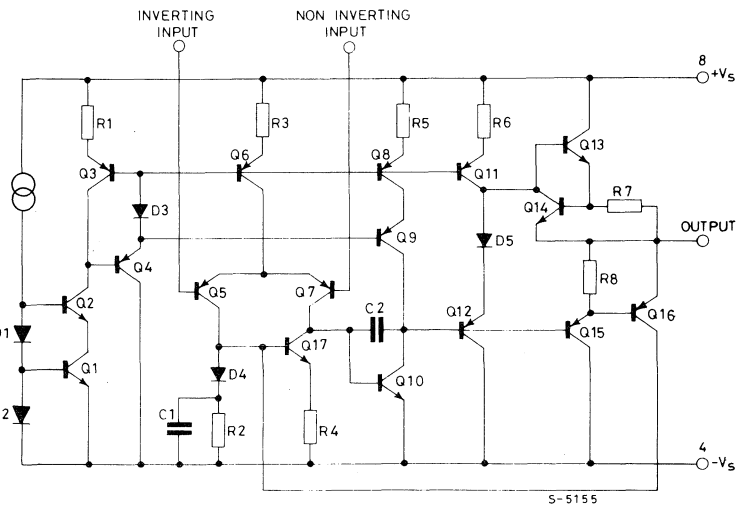
June 1988

CONNECTION AND BLOCK DIAGRAM
(top view)



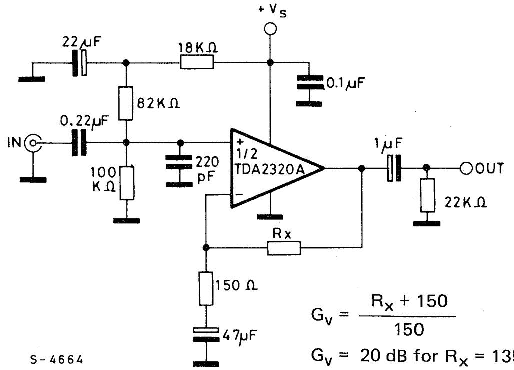


SCHEMATIC DIAGRAM
(one section)



TEST CIRCUITS

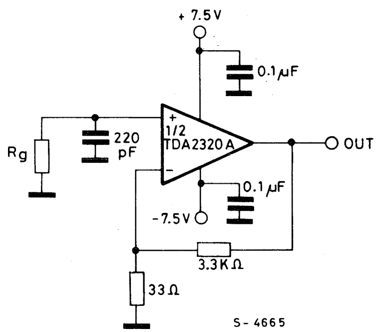
Fig. 1



$$G_v = \frac{R_x + 150}{150}$$

G_v = 20 dB for R_x = 1350Ω

Fig. 2



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, $V_s = 15V$, $T_{amb} = 25°C$, unless otherwise specified)

	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage (*)			3		36	V
I_s	Supply current (*)				0.8	2	mA
I_b	Input bias current				150	500	nA
V_{os}	Input offset voltage	$R_g < 10\ K\Omega$			1	5	mV
I_{os}	Input offset current				10	50	nA
G_v	Open loop voltage gain	$V_s = 15V$	f = 333 Hz		80		dB
			f = 1 KHz		70		
			f = 10 KHz		50		
		$V_s = 4.5V$	f = 1 KHz		70		
V_o	Output voltage swing (*)	f = 1 KHz	$V_s = 15V$		13		Vpp
		$R_L = 600\Omega$	$V_s = 4.5V$		2.5		
B	Gain-bandwidth product	f = 20 KHz		1.5	2.5		MHz
BW	Power bandwidth (*)	$V_o = 5$ Vpp d = 1%		40	70		KHz
SR	Slew rate (*)			1	1.6		V/µS
d	Distortion (*)	$V_o = 2V$	f = 1 KHz		0.03		%
		$G_v = 20$ dB	f = 10 KHz		0.08		
e_N	Total input noise voltage (**)	Curve A	$R_g = 50\Omega$		1		µV
			$R_g = 600\Omega$		1.1	1.4	
			$R_g = 5\ K\Omega$		1.5		
		B = 22 Hz to 22 KHz	$R_g = 50\Omega$		1.3		µV
			$R_g = 600\Omega$		1.5		
			$R_g = 5\ K\Omega$		2		
		f = 1 KHz	$R_g = 600\Omega$		9		$nV/\sqrt{Hz}$
Cs	Channel separation (**)		f = 1 KHz		100		dB
SVR	Supply voltage (**) rejection		f = 100 Hz		80		dB

(*) Test circuit of fig. 1.
(**) Test circuit of fig. 2.

Fig. 3 - Supply current vs. supply voltage

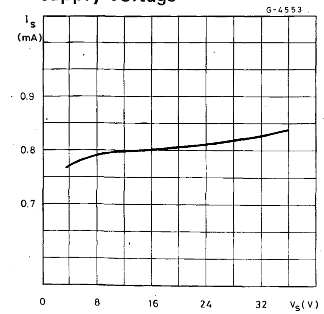


Fig. 4 - Supply current vs. ambient temperature

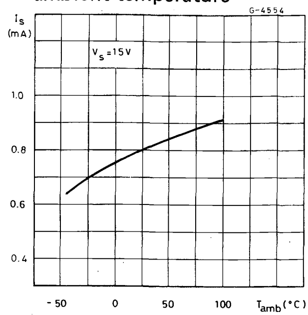


Fig. 5 - Output voltage swing vs. load resistance

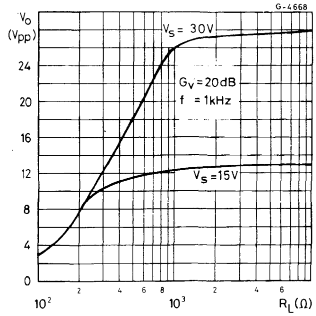


Fig. 6 - Power bandwidth

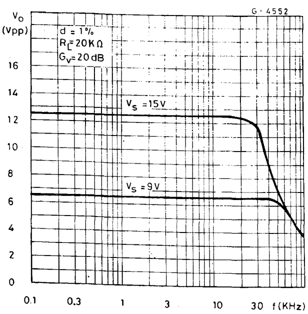


Fig. 7 - Total harmonic distortion vs. output voltage

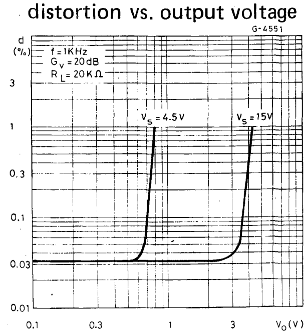


Fig. 8 - Total input noise vs. source resistance

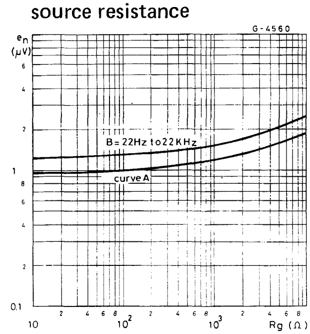


Fig. 9 - Noise density vs. frequency

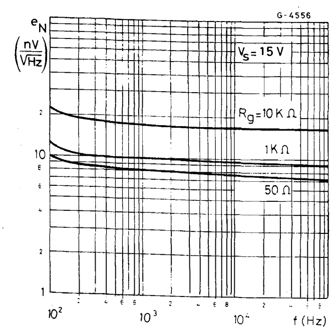


Fig. 10 - RIAA preamplifier response (circuit of fig. 12)

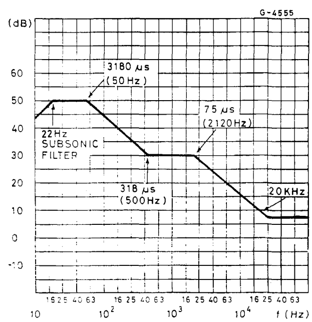
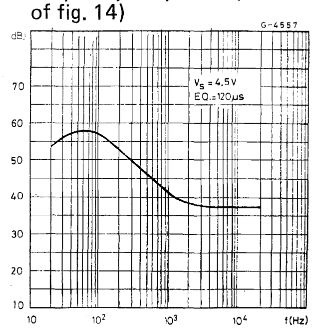


Fig. 11 - Tape preamplifier frequency response (circuit of fig. 14)



APPLICATION INFORMATION

Fig. 12 - Stereo RIAA preamplifier

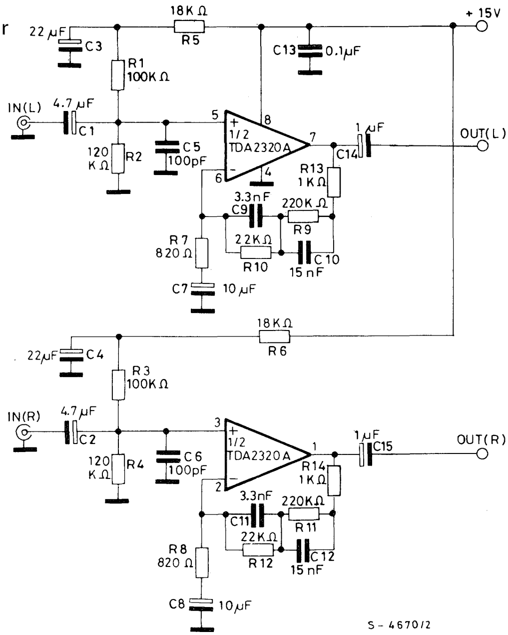
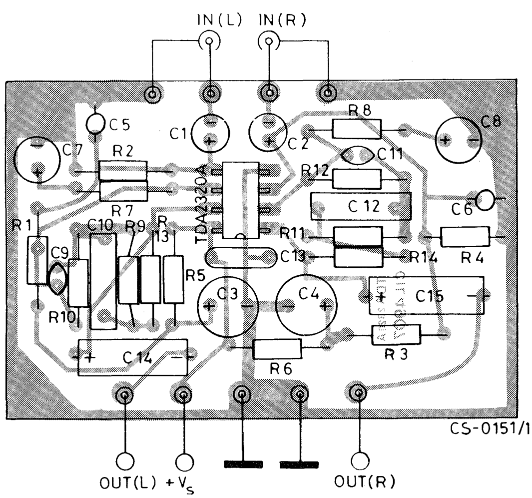


Fig. 13 - P.C. board and components layout of the circuit of fig. 12



APPLICATION INFORMATION (continued)

Fig. 14 - Stereo preamplifier for Walkman cassette players

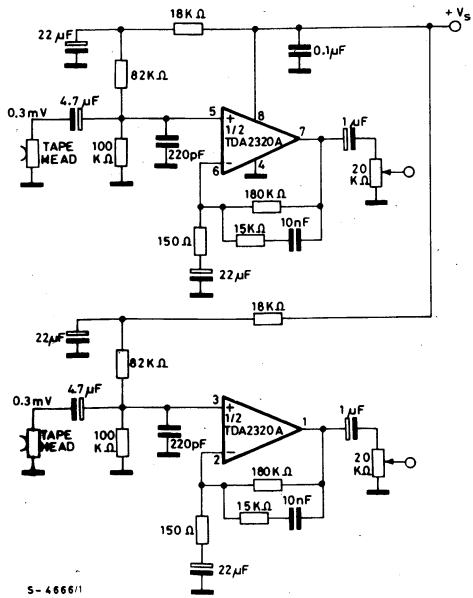


Fig. 15 - Second order 2 KHz Butterworth crossover filter for Hi-Fi active boxes

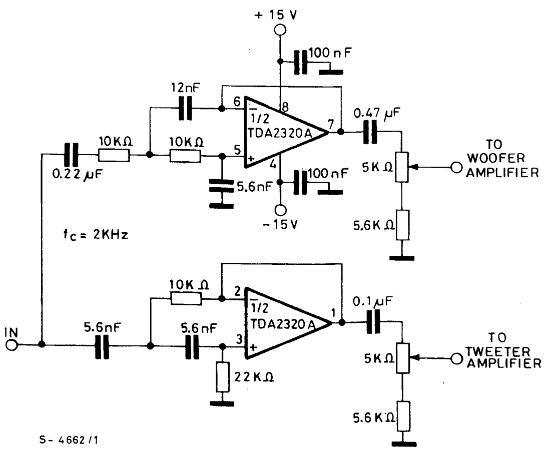
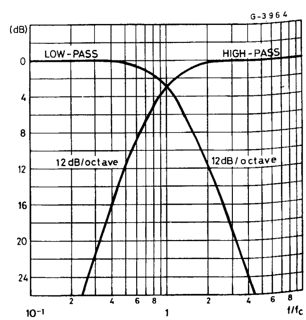


Fig. 16 - Frequency response (circuit of fig. 15)



APPLICATION INFORMATION (continued)

Fig. 17 - Third order 2.8 KHz Bessel crossover filter for Hi-Fi active boxes

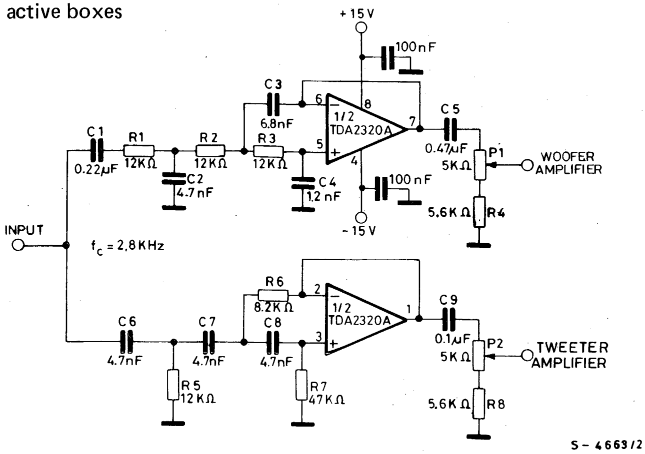


Fig. 18 - Frequency response (circuit of fig. 17)

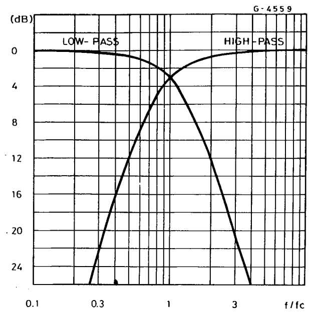


Fig. 19 - 200 Hz to 2 KHz Active Bandpass Filter for midrange speakers

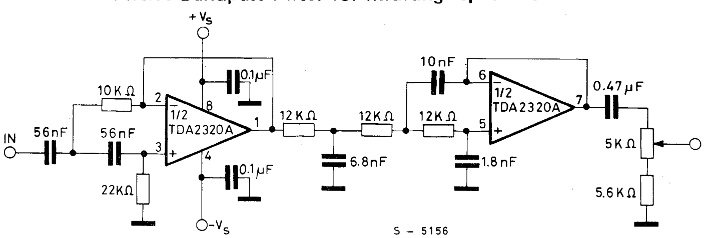
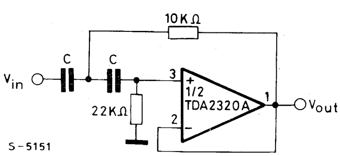
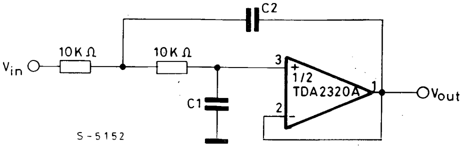


Fig. 20 - Subsonic filter



f_c (Hz)	C (μF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

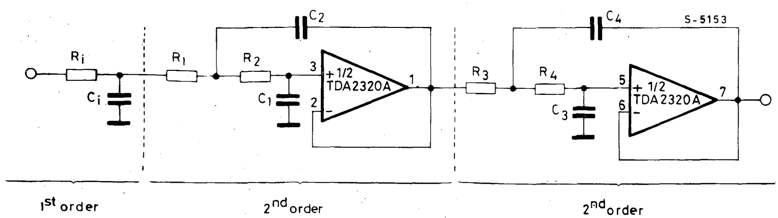
Fig. 21 - High-cut filter



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

APPLICATION INFORMATION (continued)

Fig. 22 - Fifth order 3.4 KHz low-pass Butterworth filter



For f_c = 3.4 KHz and R_i = R1 = R2 = R3 = R4 = 10 KΩ, we obtain:

$$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33 \text{ nF}$$

$$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97 \text{ nF}$$

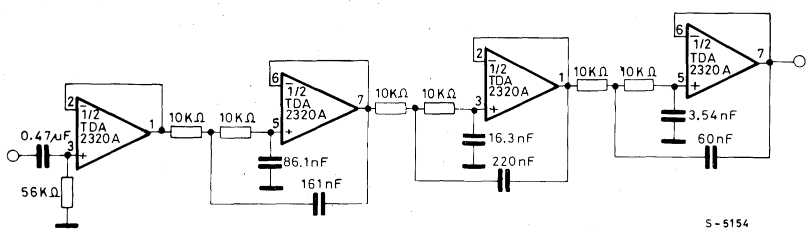
$$C2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20 \text{ nF}$$

$$C3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45 \text{ nF}$$

$$C4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2,\pi f_c} = 15.14 \text{ nF}$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Fig. 23 - Sixth-pole 355 Hz low-pass filter (Chebychev type)



This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 1/2 dB at 0.9 fc.

APPLICATION INFORMATION (continued)

Fig. 24 - Three band tone control

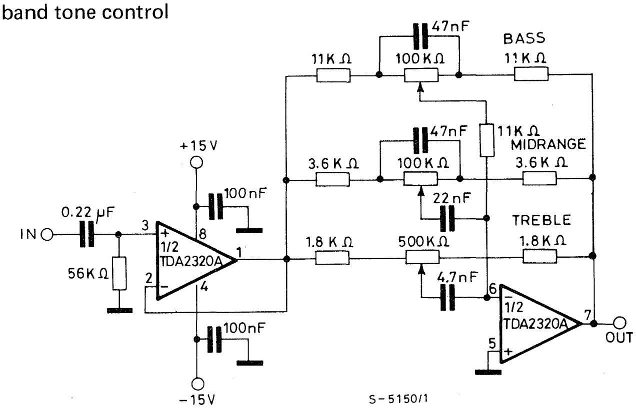
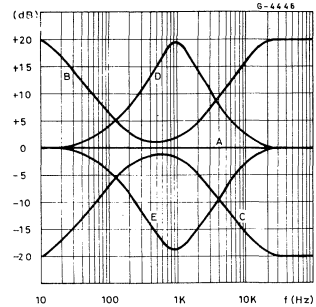


Fig. 25 - Frequency response of the circuit of fig. 24.

A : all controls flat
B : bass & treble boost, mid flat
C : bass & treble cut, mid flat
D : mid boost, bass & treble flat
E : mid cut, bass & treble flat



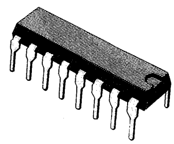
SGS-THOMSON MICROELECTRONICS

TDA2822

DUAL POWER AMPLIFIER

- SUPPLY VOLTAGE DOWN TO 3V
- LOW CROSSOVER DISTORTION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION

The TDA2822 is a monolithic integrated circuit in 12+2+2 powerdip, intended for use as dual audio power amplifier in portable radios and TV sets.



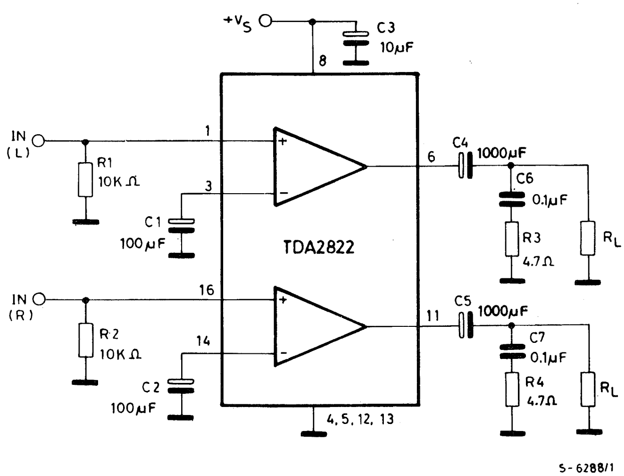
Powerdip Plastic (12+2+2)

ORDERING NUMBER: TDA2822

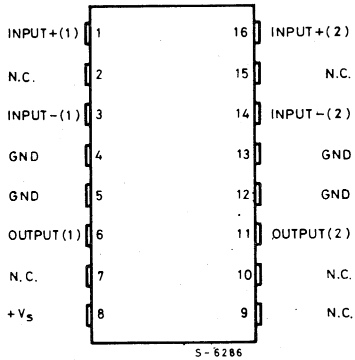
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	15	V
I_o	Output peak current	1.5	A
P_{tot}	Total power dissipation at $T_{amb} = 50°C$	1.25	W
	at $T_{case} = 70°C$	4	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

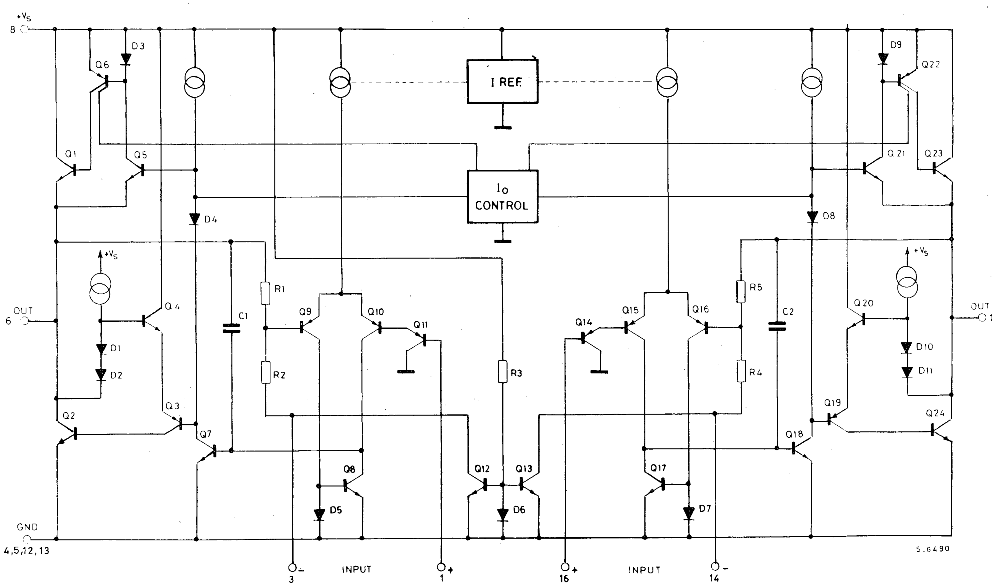
TYPICAL APPLICATION CIRCUIT (STEREO)



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max 80	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max 20	°C/W

ELECTRICAL CHARACTERISTICS ($V_s = 6V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
STEREO (Test circuit of Fig. 1)						
V_s	Supply voltage		3		15	V
V_c	Quiescent output voltage	V_s = 9V V_s = 6V		4 2.7		V V
I_d	Quiescent drain current			6	12	mA
I_b	Input bias current			100		nA
P_o	Output power (each channel)	d = 10% f = 1KHz V_s = 9V R_L = 4Ω V_s = 6V R_L = 4Ω V_s = 4.5V R_L = 4Ω	 1.3 0.45 	 1.7 0.65 0.32		 W W W
G_v	Closed loop voltage gain	f = 1KHz	36	39	41	dB
R_i	Input resistance	f = 1KHz	100			KΩ
e_N	Total input noise	R_s = 10KΩ, B = 22Hz to 22KHz		2.5		μV
		R_s = 10KΩ, Curve A		2		μV
SVR	Supply voltage rejection	f = 100Hz	24	30		dB
CS	Channel separation	R_g = 10KΩ f = 1KHz		50		dB
BRIDGE (Test circuit of Fig. 2)						
V_s	Supply voltage		3		15	V
I_d	Quiescent drain current	R_L = ∞		6	12	mA
V_{os}	Output offset voltage	R_L = 8Ω		10	60	mV
I_b	Input bias current			100		nA
P_o	Output power	d = 10% f = 1KHz V_s = 9V R_L = 8Ω V_s = 6V R_L = 8Ω V_s = 4.5V R_L = 4Ω	 2.7 0.9 	 3.2 1.35 1		 W W W
d	Distortion (f = 1KHz)	R_L = 8Ω P_o = 0.5W		0.2		%
G_v	Closed loop voltage gain	f = 1KHz		39		dB
R_i	Input resistance	f = 1KHz	100			KΩ
e_N	Total input noise	R_s = 10KΩ, B = 22Hz to 22KHz		3		μV
		R_s = 10KΩ, curve A		2.5		μV
SVR	Supply voltage rejection	f = 100Hz		40		dB

Fig. 1 - Test circuit (STEREO)

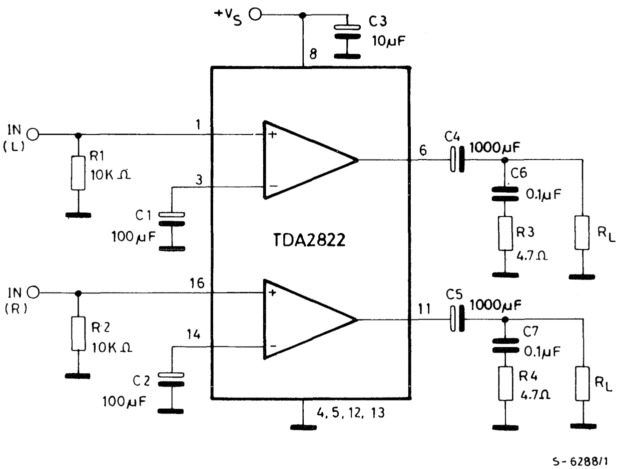


Fig. 2 - P.C. board and components layout of the circuit of Fig. 1 (1 : 1 scale)

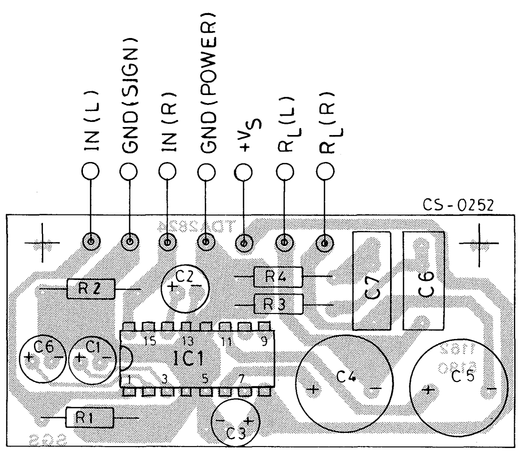


Fig. 3 - Test circuit (BRIDGE)

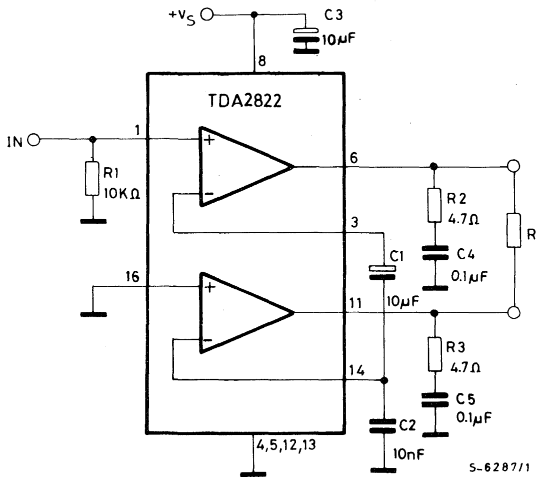


Fig. 4 - P.C. board and components layout of the circuit of Fig. 3 (1 : 1 scale)

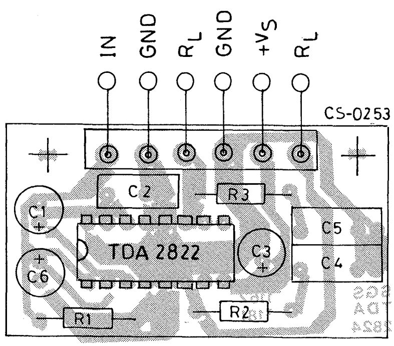


Fig. 5 - Output power vs. supply voltage (Stereo)

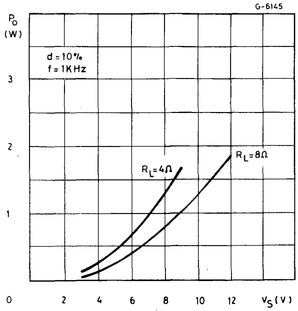


Fig. 6 - Output power vs. supply voltage (Bridge)

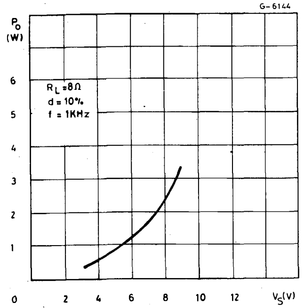


Fig. 7 - Distortion vs. output power (Bridge)

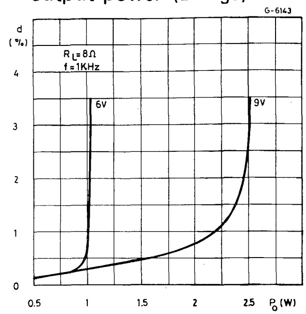


Fig. 8 - Distortion vs. output power (Bridge)

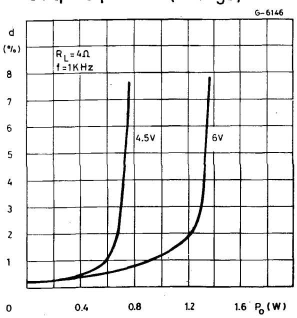


Fig. 9 - Supply voltage rejection vs. frequency

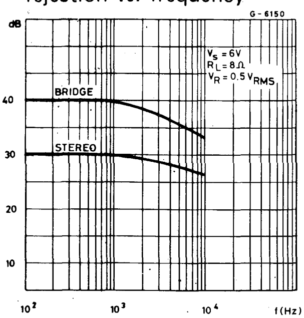


Fig. 10 - Quiescent current vs. supply voltage

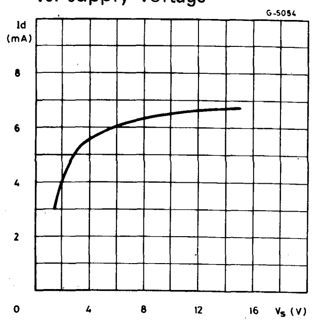


Fig. 11 - Total power dissipation vs. output power (Stereo)

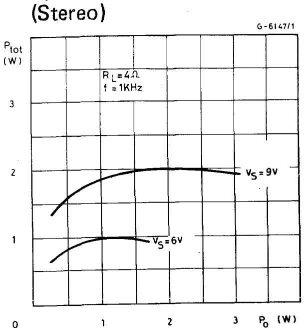


Fig. 12 - Total power dissipation vs. output power (Bridge)

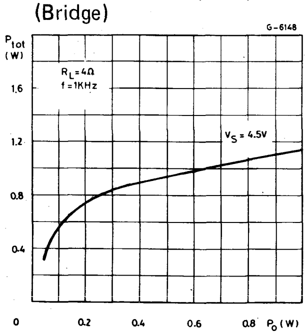


Fig. 13 - Total power dissipation vs. output power (Bridge)

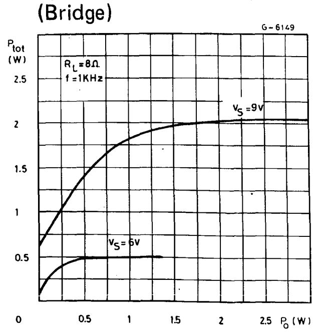
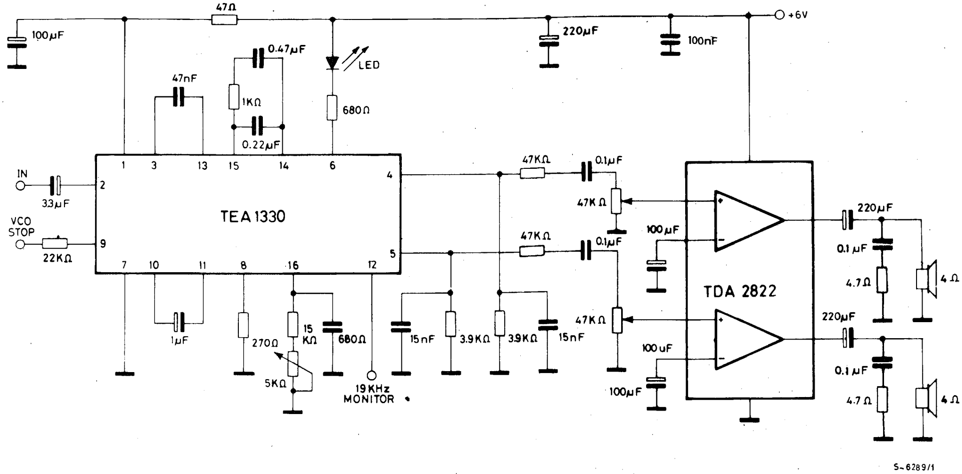


Fig. 14 - Application circuit for portable radios



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the TDA2822 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 15 or to an external heatsink (Fig. 16).

The diagram of figure 17 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4mils).

During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 15 - Example of P.C. board copper area which is used as heatsink.

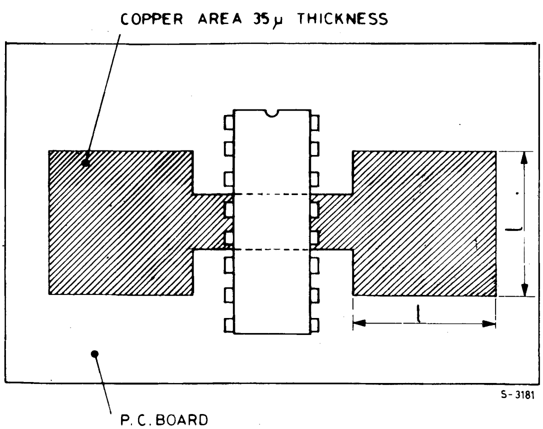
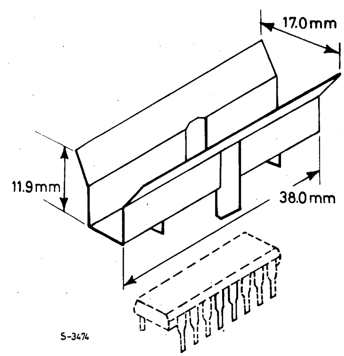


Fig. 16 - External heatsink mounting example



MOUNTING INSTRUCTION (continued)

Fig. 6 – Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

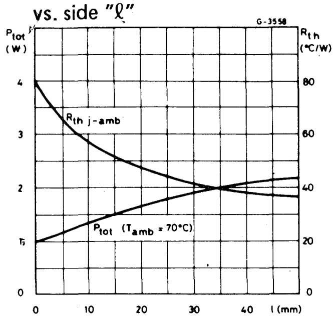
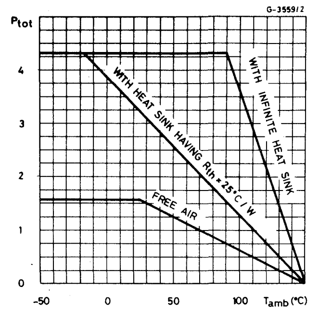


Fig. 7 – Maximum allowable power dissipation vs. ambient temperature

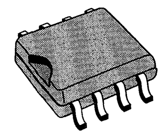


TDA2822D

DUAL LOW-VOLTAGE POWER AMPLIFIER

ADVANCE DATA

- SUPPLY VOLTAGE DOWN TO 1.8V
- LOWCROSSOVER DISTORTION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION



SO8

ORDERING NUMBER: TDA2822D

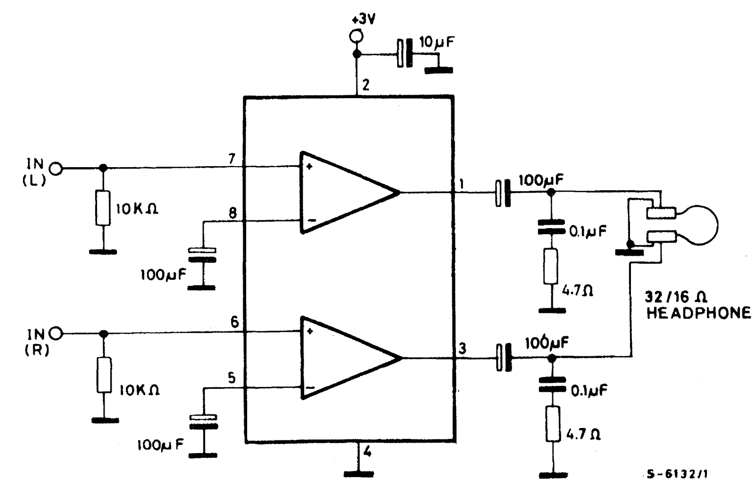
DESCRIPTION

The TDA2822D is a monolithic integrated circuit in 8 lead (SO-8) package. It is intended for use as dual audio power amplifier in portable cassette players, radios and CD players

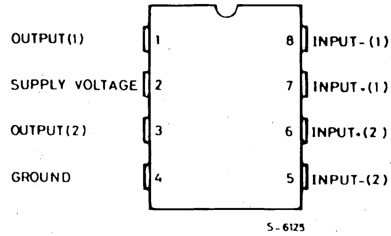
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	15	V
I_O	Peak Output	1	A
P_{tot}	Total Power Dissipation T_{amb} = 50°C	0.5	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

APPLICATION CIRCUIT



PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	200	°C/W

Figure 1: Stereo Application and Test Circuit

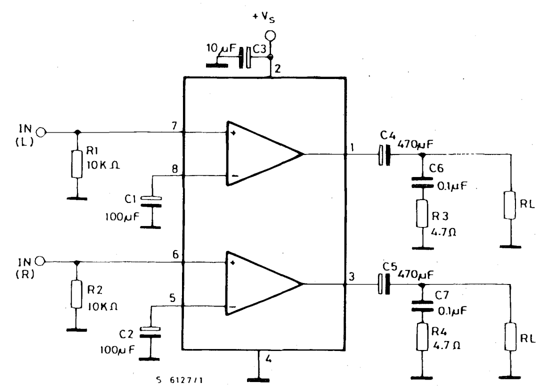
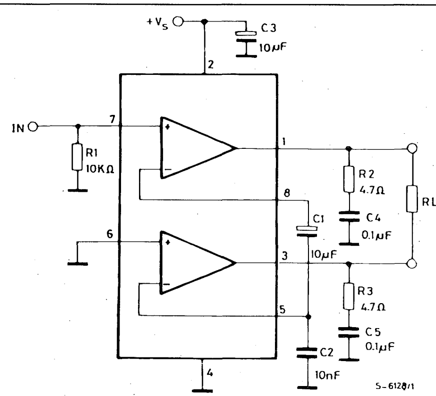


Figure 2: Bridge Application and Test Circuit



ELECTRICAL CHARACTERISTICS (V_S = 6V; T_{amb} = 25°C, unless otherwise specified.
STEREO (Test circuit of fig. 1).

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_S	Supply Voltage			1.8		15	V
I_d	Total Quiescent Drain Current					15	mA
V_O	Quiescent Output Voltage				2.7		V
		V_S = 3V			1.2		V
I_b	Input Bias Current				100		nA
P_O	Output Power (each channel) (f = 1KHz, d = 10%)	R_L = 32Ω	V_S = 9V V_S = 6V V_S = 4.5V V_S = 3V V_S = 2V		300 120 60 20 5		mW
		R_L = 16Ω	V_S = 6V	170	220		mW
		R_L = 8Ω	V_S = 6V	300	380		mW
		R_L = 4Ω	V_S = 4.5V V_S = 3V		320 110		mW mW
d	Distortion	R_L = 32Ω	P_O = 40mW		0.2		%
		R_L = 16Ω	P_O = 75mW		0.2		%
		R_L = 8Ω	P_O = 150mW		0.2		%
G_V	Closed Loop Voltage Gain	f = 1KHz		36	39	41	dB
ΔG_V	Channel Balance					±1	dB
R_i	Input Resistance	f = 1KHz		100			KΩ
e_N	Total Input Noise	R_s = 10kΩ B = Curve A			2		μV
		R_s = 10kΩ B = 22Hz to 22KHz			2.5		μV
SVR	Supply Voltage Rejection	f = 100Hz C1 = C2 = 100μF		24	30		dB
C_s	Channel Separation	f = 1KHz			50		dB

BRIDGE (Test circuit of fig.2)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_S	Supply Voltage			1.8		15	V
I_d	Total Quiescent Drain Current	R_L = ∞				15	mA
V_{os}	Output Offset Voltage (between the outputs)	R_L = 8Ω				±80	mV
I_b	Input Bias Current				100		nA
P_O	Output Power (f = 1KHz, d = 10%)	R_L = 32Ω	V_S = 9V V_S = 6V V_S = 4.5V V_S = 3V V_S = 2V	 320 50 	1000 400 200 65 8		mW
		R_L = 16Ω	V_S = 6V V_S = 3V		800 120		mW mW
		R_L = 8Ω	V_S = 4.5V V_S = 3V		700 220		mW mW
		R_L = 4Ω	V_S = 3V V_S = 2V		350 80		mW mW
d	Distortion	R_L = 8Ω P_O = 0.5W f = 1KHz			0.2		%
G_V	Closed Loop Voltage Gain	f = 1KHz			39		dB
R_i	Input Resistance	f = 1KHz		100			KΩ
e_N	Total Input Noise	R_s = 10kΩ B = Curve A			2.5		μV
		R_s = 10kΩ B = 22Hz to 22KHz			3		μV
SVR	Supply Voltage Rejection	f = 100Hz			40		dB
B	Power Bandwidth (-3dB)	R_L = 8Ω P_O = 1W			120		KHz

Figure 3: Supply Voltage Rejection vs. Frequency

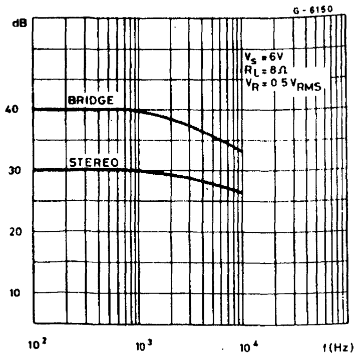


Figure 4: Output Power vs. Supply Voltage (THD = 10%, f = 1KHz Stereo)

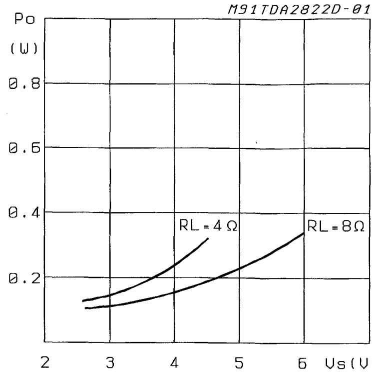


Figure 5: Total Power Dissipation vs. Output Power (Bridge)

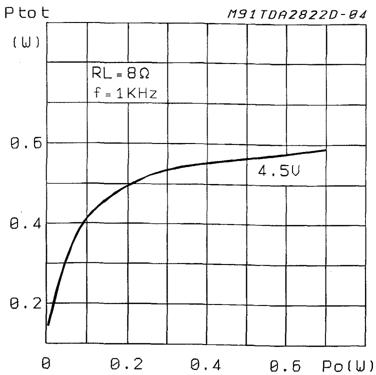
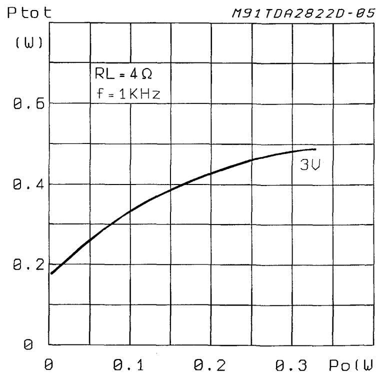


Figure 6: Total Power Dissipation vs. Output Power (Bridge)



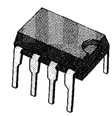
SGS-THOMSON MICROELECTRONICS

TDA2822M

DUAL LOW-VOLTAGE POWER AMPLIFIER

- SUPPLY VOLTAGE DOWN TO 1.8V
- LOW CROSSOVER DISTORTION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION

The TDA2822M is a monolithic integrated circuit in 8 lead Minidip package. It is intended for use as dual audio power amplifier in portable cassette players and radios.



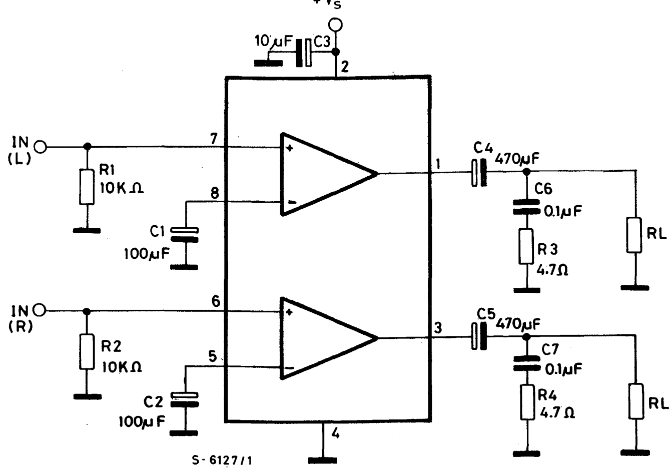
Minidip Plastic

ORDERING NUMBER: TDA2822M

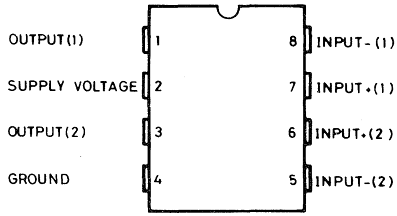
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	15	V
I_o	Peak output current	1	A
P_{tot}	Total power dissipation at $T_{amb} = 50°C$	1	W
	at $T_{case} = 50°C$	1.4	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST CIRCUIT

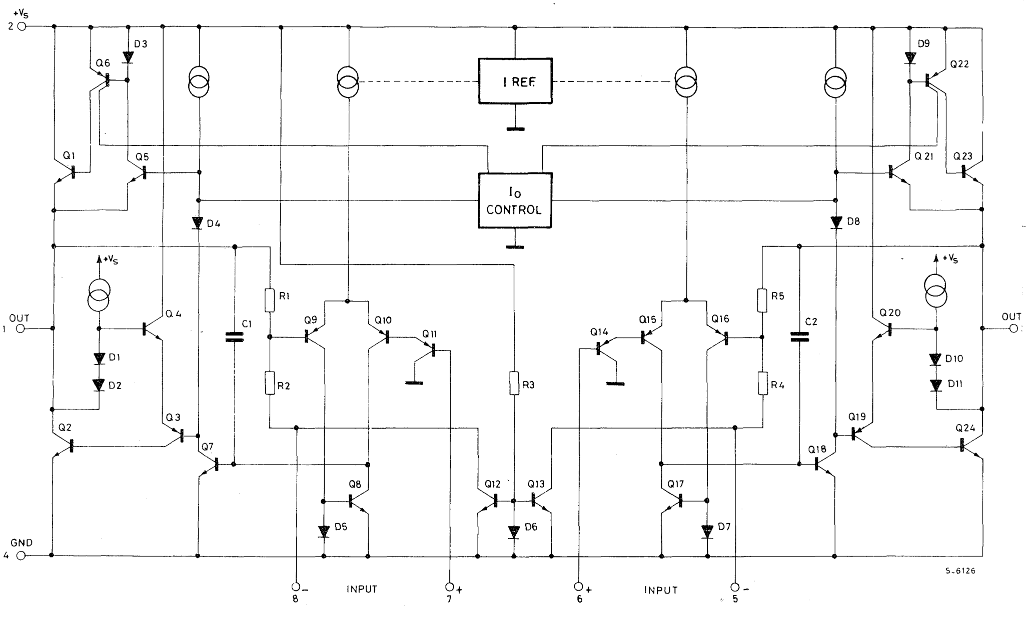


CONNECTION DIAGRAM
(Top view)



S-6125

SCHEMATIC DIAGRAM



S-6126

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-pin (4)	max	70	°C/W

STEREO APPLICATION

Fig. 1 – Test circuit

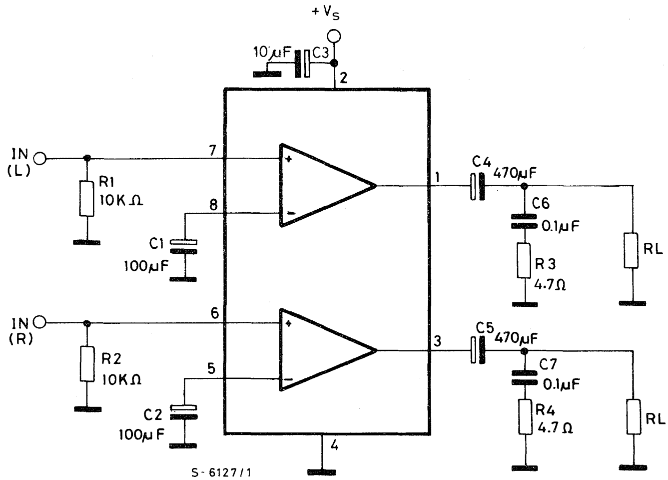
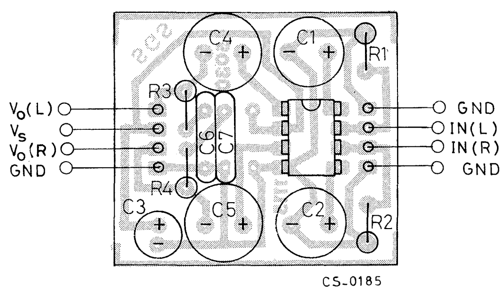


Fig. 2 – P.C. board and component layout of the circuit of Fig. 1 (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_s = 6V, T_{amb} = 25°C, unless otherwise specified)

STEREO (Test circuit of Fig. 1)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			1.8		15	V
V_o	Quiescent output voltage				2.7		V
		V_s = 3V			1.2		V
I_d	Quiescent drain current				6	9	mA
I_b	Input bias current				100		nA
P_o	Output power (each channel) (f = 1KHz, d = 10%)	R_L = 32Ω	V_s = 9V		300		mW
			V_s = 6V	90	120		
			V_s = 4.5V		60		
			V_s = 3V	15	20		
			V_s = 2V		5		
		R_L = 16Ω	V_s = 6V	170	220		mW
		R_L = 8Ω	V_s = 9V		1000		mW
			V_s = 6V	300	380		
		R_L = 4Ω	V_s = 6V	450	650		mW
			V_s = 4.5V		320		
			V_s = 3V		110		
d	Distortion (f = 1KHz)	R_L = 32Ω	P_o = 40mW		0.2		%
		R_L = 16Ω	P_o = 75mW		0.2		%
		R_L = 8Ω	P_o = 150mW		0.2		%
G_v	Closed loop voltage gain	f = 1KHz		36	39	41	dB
ΔG_v	Channel balance					± 1	dB
R_i	Input resistance	f = 1KHz		100			KΩ
e_N	Total input noise	R_s = 10KΩ	B = Curve A		2		μV
			B = 22Hz to KHz		2.5		
SVR	Supply voltage rejection	f = 100Hz	C1 = C2 = 100μF	24	30		dB
C_s	Channel separation	f = 1KHz			50		dB

BRIDGE APPLICATION

Fig. 3 - Test circuit

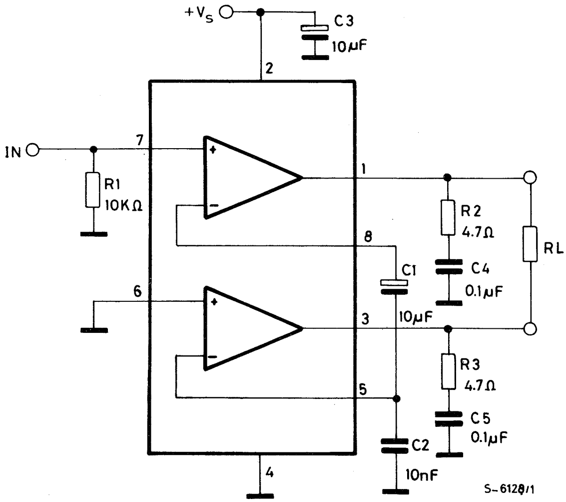
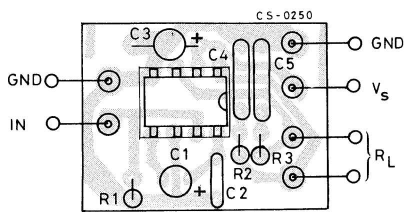


Fig. 4 - P.C. board and components layout of the circuit of Fig. 3 (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_s = 6V, T_{amb} = 25°C unless otherwise specified)

BRIDGE (Test circuit of Fig. 3)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			1.8		15	V
I_d	Quiescent drain current	$R_L = \infty$			6	9	mA
V_{os}	Output offset voltage (between the outputs)	$R_L = 8\Omega$				± 50	mV
I_b	Input bias current				100		nA
P_o	Output power (f = 1KHz, d = 10%)	$R_L = 32\Omega$	V_s = 9V V_s = 6V V_s = 4.5V V_s = 3V V_s = 2V	 320 50 	1000 400 200 65 8		mW
		$R_L = 16\Omega$	V_s = 9V V_s = 6V V_s = 3V		2000 800 120		mW
		$R_L = 8\Omega$	V_s = 6V V_s = 4.5V V_s = 3V	900	1350 700 220		mW
		$R_L = 4\Omega$	V_s = 4.5V V_s = 3V V_s = 2V	 200 	1000 350 80		mW
d	Distortion	P_o = 0.5W, f = 1KHz	$R_L = 8\Omega$		0.2		%
G_v	Closed loop voltage gain	f = 1KHz			39		dB
R_i	Input resistance	f = 1KHz		100			KΩ
e_N	Total input noise	$R_s = 10K\Omega$	B = Curve A		2.5		µV
			B = 22Hz to 22KHz		3		µV
SVR	Supply voltage rejection	f = 100Hz			40		dB
B	Power bandwidth (-3dB)	$R_L = 8\Omega$	P_o = 1W		120		KHz

Fig. 5 - Quiescent current vs. supply voltage

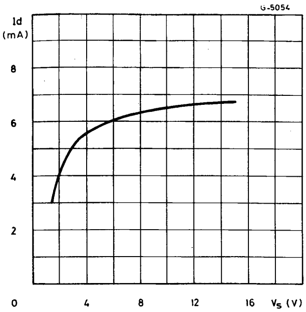


Fig. 6 - Supply voltage rejection vs. frequency

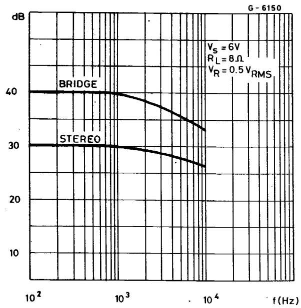


Fig. 7 - Output power vs. supply voltage (THD= 10%, f = 1KHz Stereo)

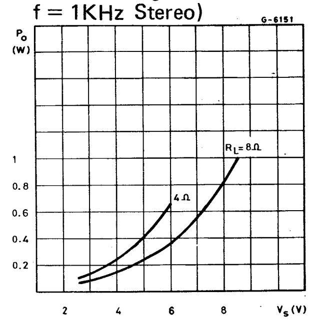


Fig. 8 - Distortion vs. output power (Stereo)

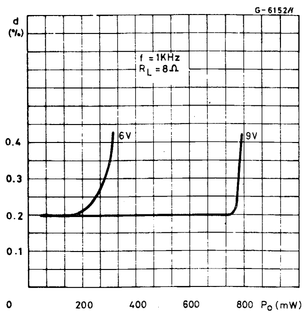


Fig. 9 - Distortion vs. output power (Stereo)

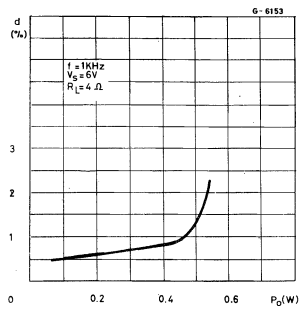


Fig. 10 - Output power vs. supply voltage (Bridge)

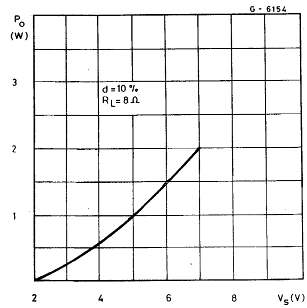


Fig. 11 - Distortion vs. output power (Bridge)

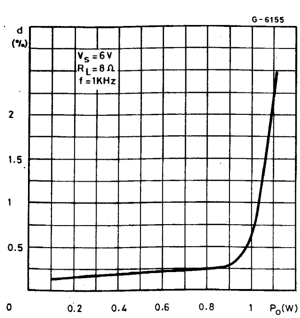


Fig. 12 - Total power dissipation vs. output power (Bridge)

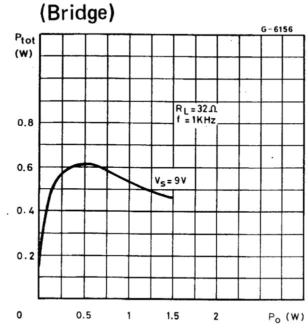


Fig. 13 - Total power dissipation vs. output power (Bridge)

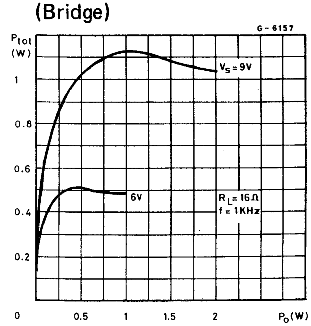


Fig. 14 - Total power dissipation vs. output power (Bridge)

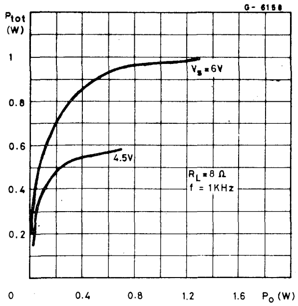


Fig. 15 - Total power dissipation vs. output power (Bridge)

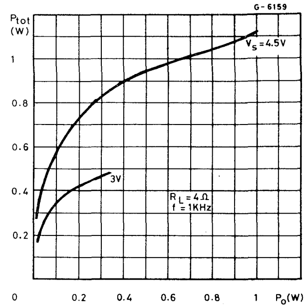
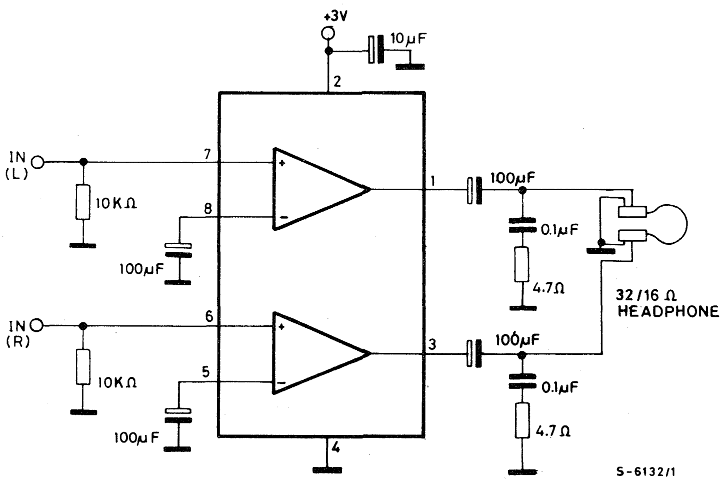


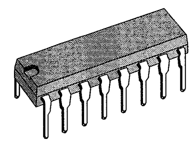
Fig. 16 - Typical application in portable players



DUAL POWER AMPLIFIER

ADVANCE DATA

- SUPPLY VOLTAGE DOWN TO 3 V
- HIGH SVR
- LOW CROSSOVER DISTORTION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION



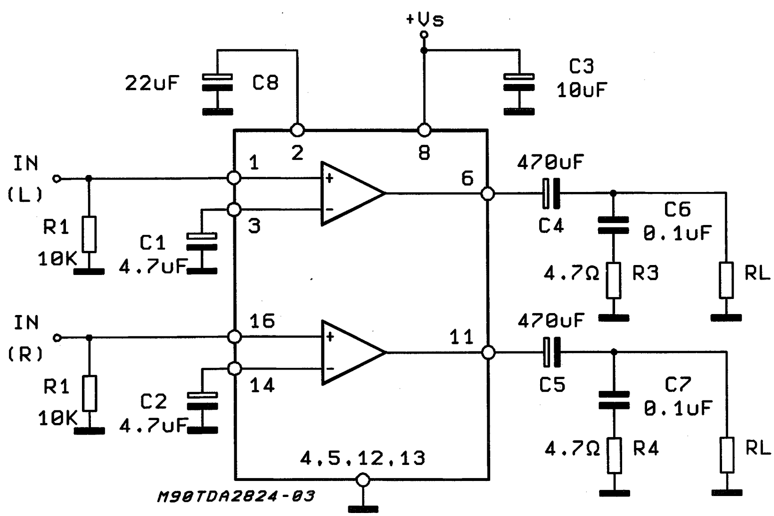
Powerdip (12+2+2)

ORDERING NUMBER : TDA2824

DESCRIPTION

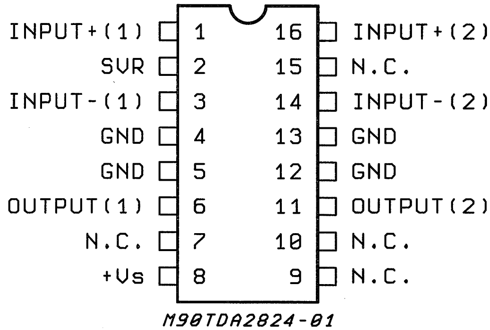
The TDA2824 is a monolithic integrated circuit in 12+2+2 powerdip, intended for use as dual audio power amplifier in portable radios and TV sets.

TYPICAL APPLICATION CIRCUIT (Stereo)

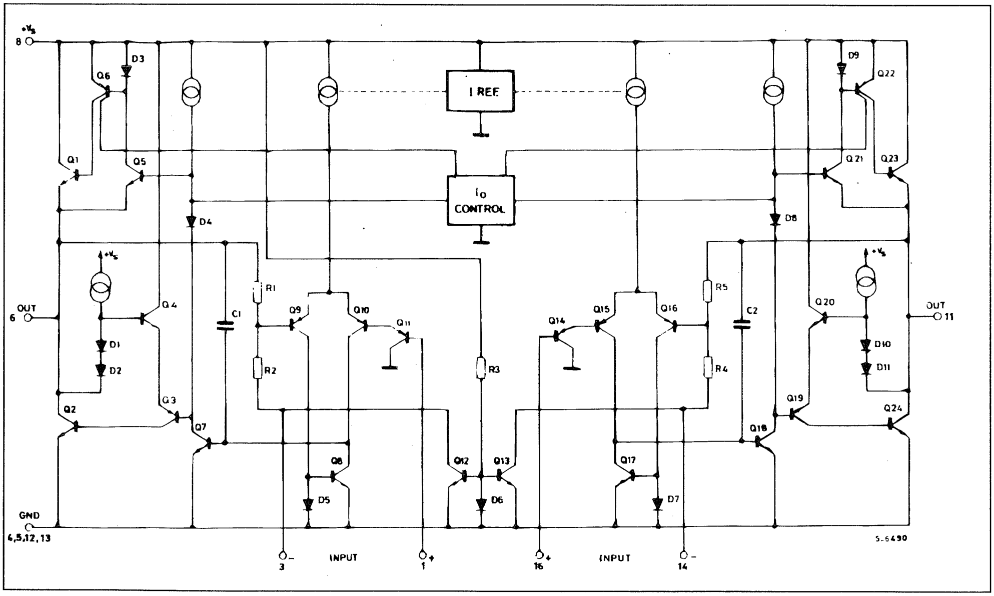


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	16	V
I_o	Output Peak Current	1.5	A
P_{tot}	Total Power Dissipation at T_{amb} = 50 °C at T_{case} = 70 °C	1.25 4	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-pins	Max	20	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 6V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
STEREO (test circuit of fig. 1)						
V_S	Supply Voltage		3		15	V
V_O	Quiescent Output Voltage	V_S = 9V V_S = 9V		4 2.7		V V
I_d	Quiescent Drain Current			6	12	mA
I_b	Input Bias Current			100		nA
P_O	Output Power (each channel)	d = 10% f = 1KHz V_S = 9V R_L = 4Ω V_S = 6V R_L = 4Ω V_S = 4.5V R_L = 4Ω	 1.3 0.45 	 1.7 0.65 0.32		 W W W
d	Distortion	V_S = 9V, f = 1KHz R_L = 8Ω, P_O = 0.5W		0.2		%
G_V	Closed Loop Voltage Gain	f = 1KHz	36	39	41	dB
R_i	Input Resistance	f = 1KHz	100			KΩ
e_N	Total Input Noise	R_S = 10KΩ B = 22Hz to 22KHz		2.5		µV
		R_S = 10KΩ Curve A		2		µV
SVR	Supply Voltage Rejection	f = 100Hz	40	50		dB
CS	Channel Separation	R_S = 10KΩ f = 1KHz		50		dB
BRIDGE (test circuit of fig. 2)						
V_S	Supply Voltage		3		15	V
V_{OS}	Output Offset Voltage	R_L = 8Ω			60	mV
I_b	Imput Bias Current			100		nA
P_O	Output Power	d = 10% f = 1KHz V_S = 9V R_L = 8Ω V_S = 6V R_L = 8Ω V_S = 4.5V R_L = 4Ω	 2.5 0.9 	 3.2 1.35 1		 W W W
d	Distortion (f = 1KHz)	R_L = 8Ω P_O = 0.5W		0.2		%
G_V	Closed Loop Voltage Gain	f = 1KHz		39		dB
e_N	Total Input Noise	R_S = 10KΩ B = 22Hz to 22KHz		3		mV
		R_S = 10KΩ Curve A		2.5		µV
SVR	Supply Voltage Rejection	f = 100Hz	48	60		dB

Figure 1 : Test Circuit (stereo).

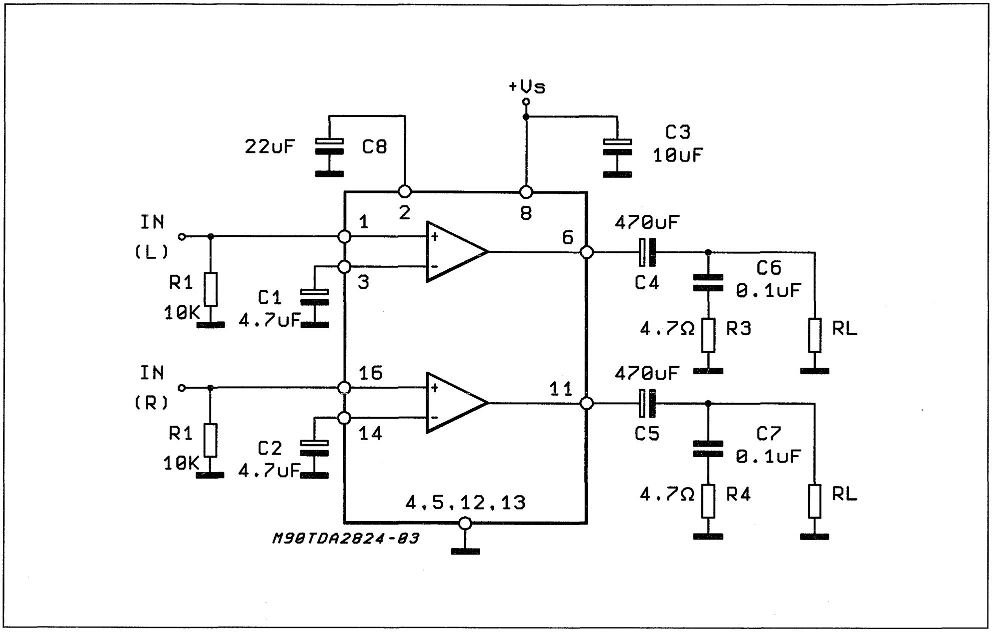


Figure 2: P.C. Board and Component Layout of the Circuit of Figure 1. (1:1 scale)

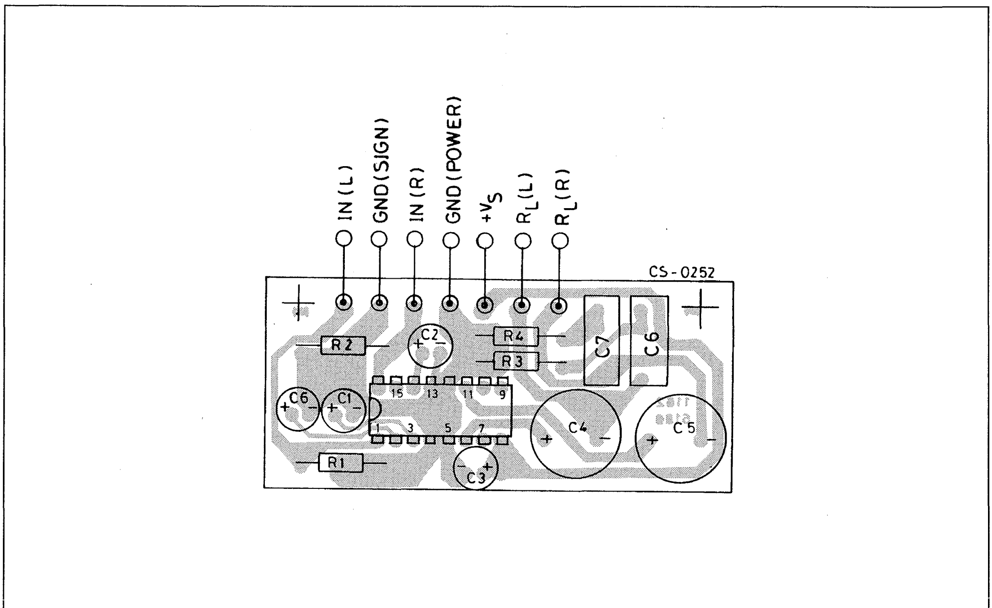


Figure 3 : Test Circuit (bridge).

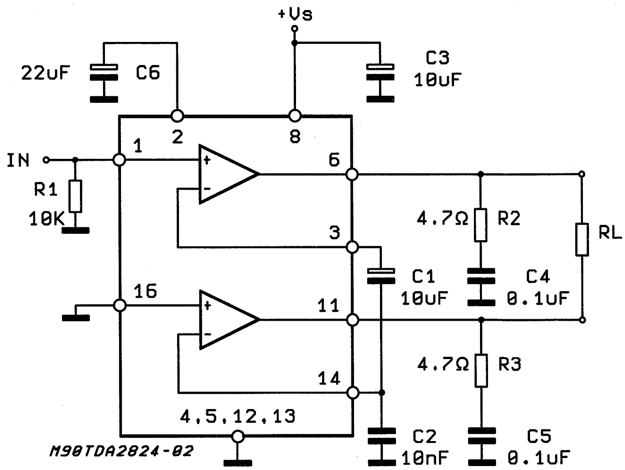


Figure 4: P.C. Board and Component Layout of the Circuit of Figure 3. (1:1 scale)

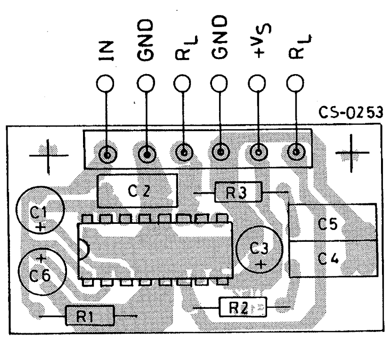


Figure 3 : Output Power vs. Supply Voltage (Stereo).

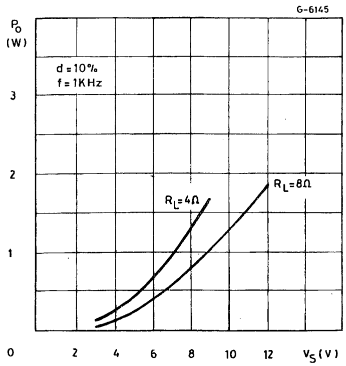


Figure 4 : Output Power vs. Supply Voltage (Bridge).

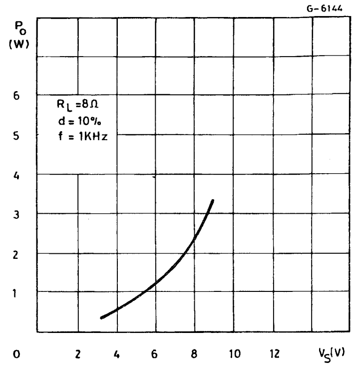


Figure 5 : Distortion vs. Output Power (Bridge).

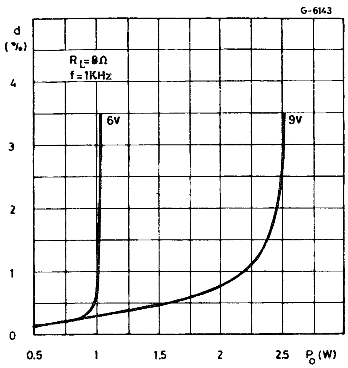


Figure 6 : Distortion vs. Output Power (Bridge).

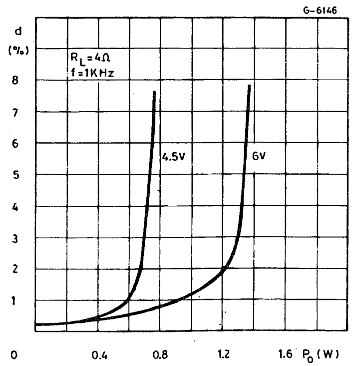


Figure 7 : Supply Voltage Rejection vs. Frequency (Stereo)

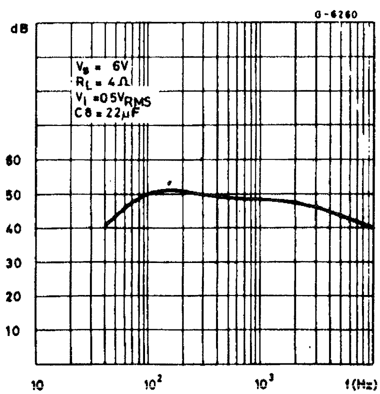


Figure 8 : Quiescent Current vs. Supply Voltage.

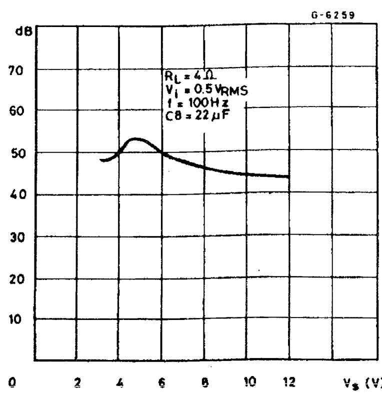


Figure 9 : Quiescent Current vs. Supply Voltage.

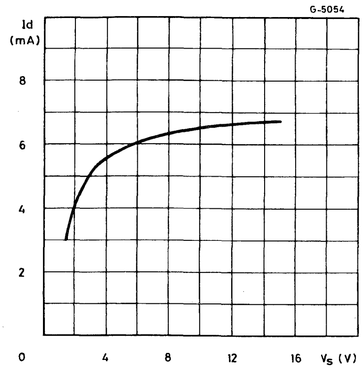


Figure 10 : Total Power Dissipation vs. Output Power (Stereo).

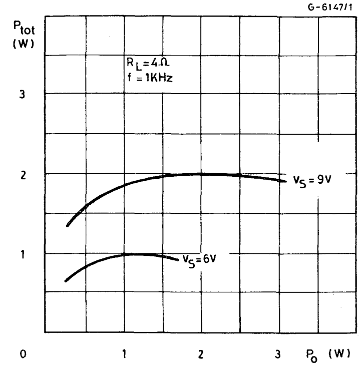


Figure 11 : Total Power Dissipation vs. Output Power (Bridge).

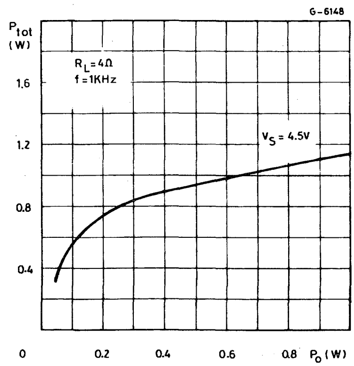
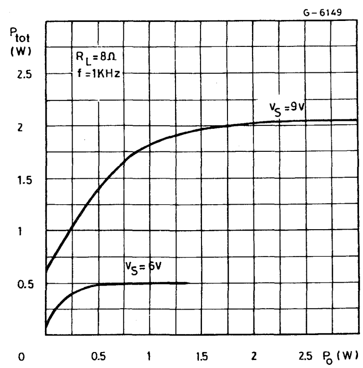


Figure 12 : Total Power Dissipation vs. Output Power (Bridge).



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the TDA2824 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Figure 13) or to an external heatsink (Figure 14).

The diagram of Figure 15 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "∂" of two equal square copper areas having a thickness of 35 µ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 13 : Example of P.C. Board Copper Area which is used as Heatsink.

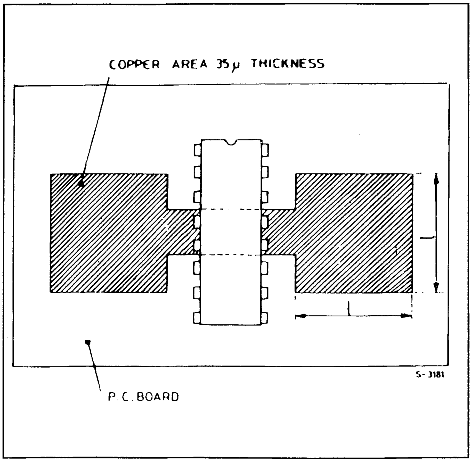


Figure 14 : External Heatsink Mounting Example.

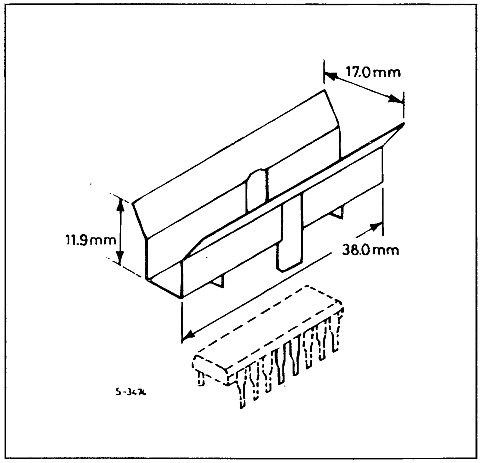


Figure 15 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "∂".

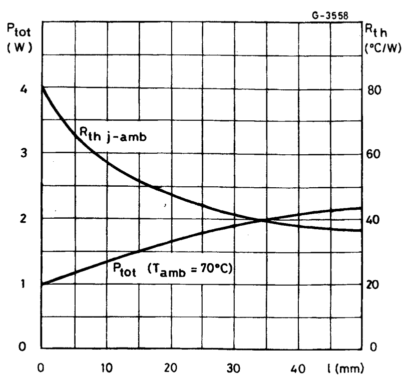
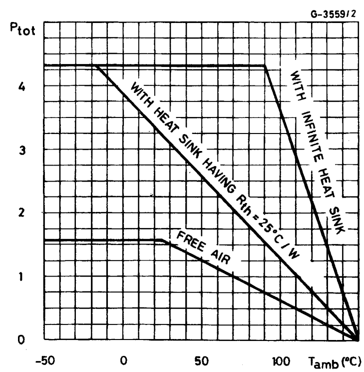


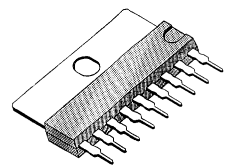
Figure 16 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



DUAL POWER AMPLIFIER

- SUPPLY VOLTAGE DOWN TO 3V
- HIGH SVR
- LOW CROSSOVER DISTORTION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION

The TDA2824S is a monolithic integrated circuit assembled in single line 9 pins package (SIP. 9), intended for use as dual audio power amplifier in portable radios and TV sets.



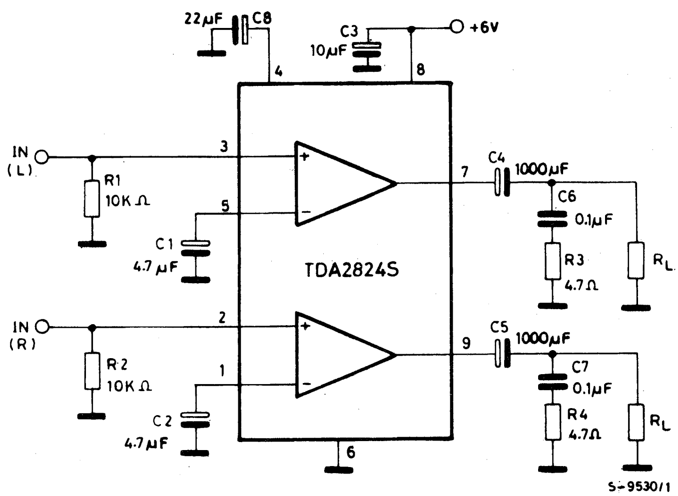
SIP. 9

ORDERING NUMBER: TDA2824S

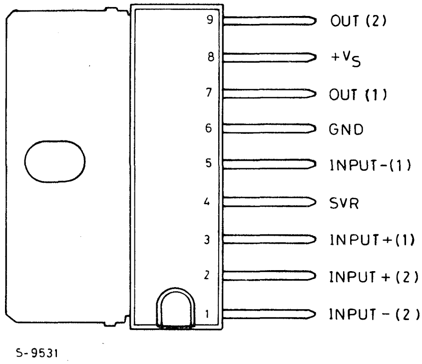
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
I_o	Output peak current	1.5	A
P_{tot}	Total power dissipation at $T_{amb} = 60°C$	1.3	W
	at $T_{case} = 70°C$	8	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

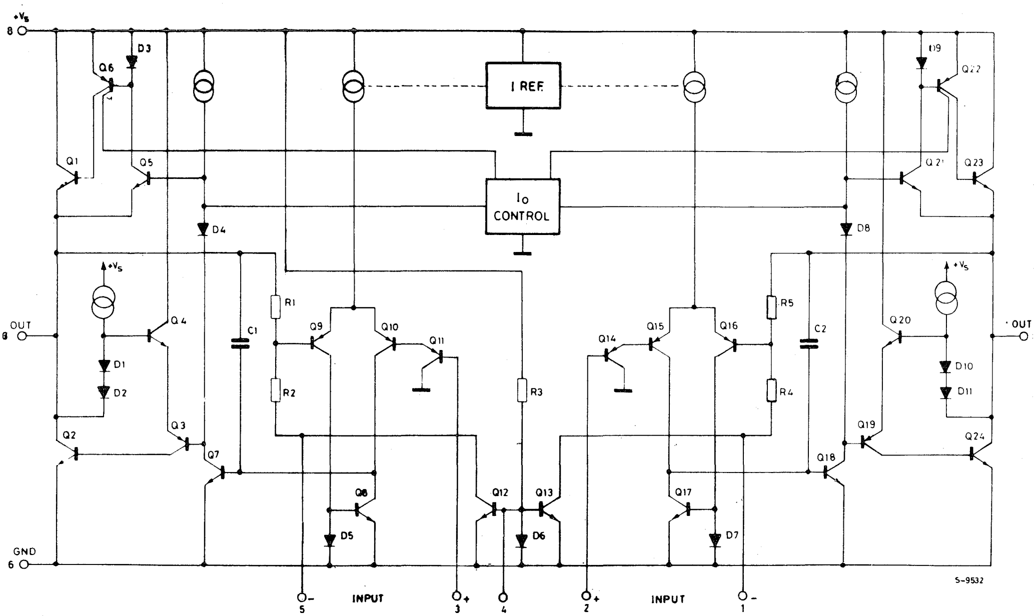
TYPICAL APPLICATION CIRCUIT (Stereo)



CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	10	°C/W

ELECTRICAL CHARACTERISTICS ($V_s = 6V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
STEREO (Test circuit of Fig. 1)						
V_s	Supply voltage		3		15	V
V_c	Quiescent output voltage	V_s = 9V V_s = 6V		4 2.7		V V
I_d	Quiescent drain current			6	12	mA
I_b	Input bias current			100		nA
P_o	Output power (each channel)	d = 10% f = 1KHz V_s = 9V R_L = 4Ω V_s = 6V R_L = 4Ω V_s = 4.5V R_L = 4Ω	 1.3 0.45 	 1.7 0.65 0.32		 W W W
G_v	Closed loop voltage gain	f = 1KHz	36	39	41	dB
R_i	Input resistance	f = 1KHz	100			KΩ
e_N	Total input noise	R_g = 10KΩ, B = 22Hz to 22KHz		2.5		μV
		R_g = 10KΩ, Curve A		2		μV
SVR	Supply voltage rejection	f = 100Hz	40	50		dB
CS	Channel separation	R_g = 10KΩ f = 1KHz		50		dB
BRIDGE (Test circuit of Fig. 3)						
V_s	Supply voltage		3		15	V
I_d	Quiescent drain current	R_L = ∞		6	12	mA
V_{os}	Output offset voltage	R_L = 8Ω		10	60	mV
I_b	Input bias current			100		nA
P_o	Output power	d = 10% f = 1KHz V_s = 9V R_L = 8Ω V_s = 6V R_L = 8Ω V_s = 4.5V R_L = 4Ω	 2.5 0.9 	 3.2 1.35 1		 W W W
d	Distortion	f = 1KHz; R_L = 8Ω; P_o = 0.5W		0.2		%
G_v	Closed loop voltage gain	f = 1KHz		39		dB
R_i	Input resistance	f = 1KHz	100			KΩ
e_N	Total input noise	R_g = 10KΩ, B = 22Hz to 22KHz		3		μV
		R_g = 10KΩ, Curve A		2.5		μV
SVR	Supply voltage rejection	f = 100Hz	48	60		dB

Fig. 1 - Test circuit (STEREO)

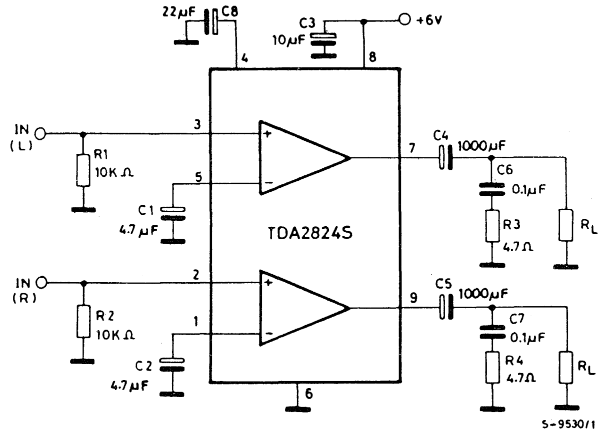


Fig. 2 - P.C. board and components layout of the circuit of Fig. 1 (1 : 1 scale)

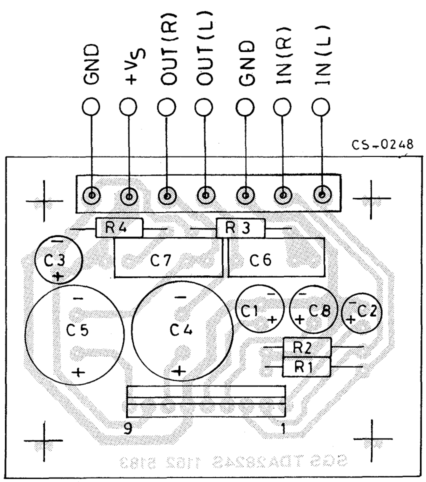


Fig. 3 - Test circuit (BRIDGE)

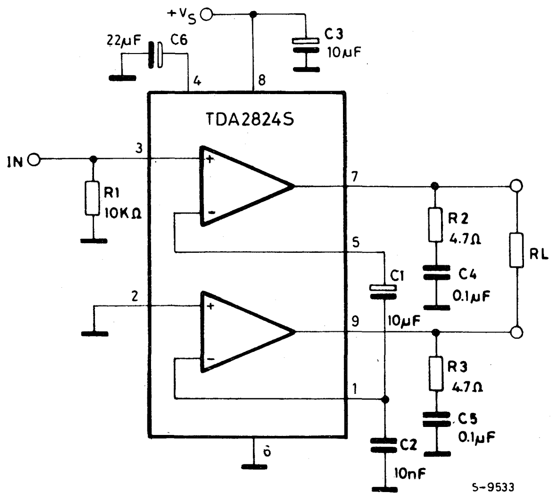


Fig. 4 - P.C. board and components layout of the circuit of the Fig. 3 (1 : 1 scale)

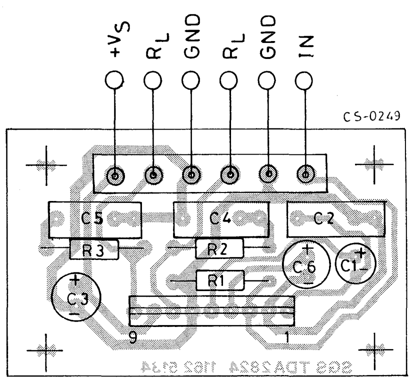


Fig. 5 - Output power vs. supply voltage (Stereo)

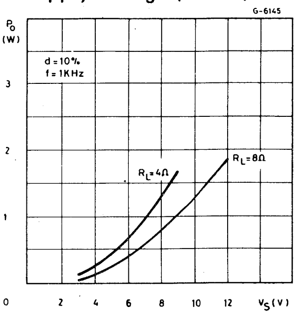


Fig. 6 - Output power vs. supply voltage (Bridge)

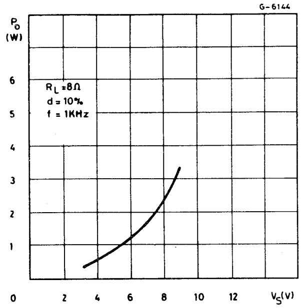


Fig. 7 - Distortion vs. output power (Bridge)

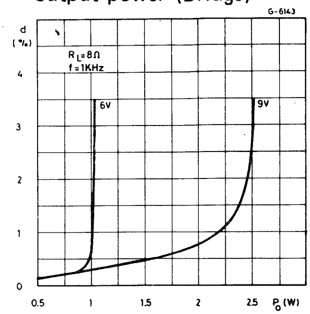


Fig. 8 - Distortion vs. output power (Bridge)

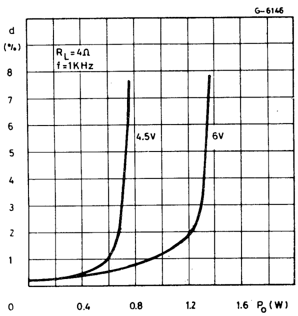


Fig. 9 - Supply voltage rejection vs. supply voltage (Stereo)

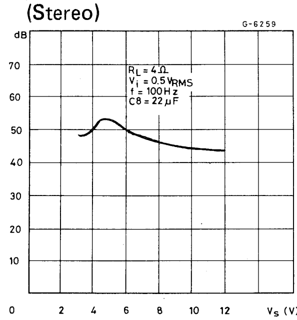


Fig. 10 - Supply voltage rejection vs. frequency (Stereo)

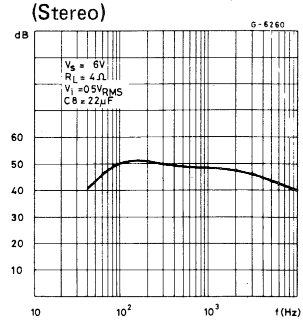


Fig. 11 - Quiescent current vs. supply voltage

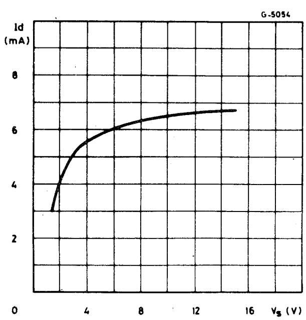


Fig. 12 - Total power dissipation vs. output power (Stereo)

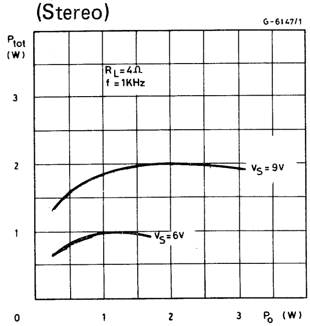
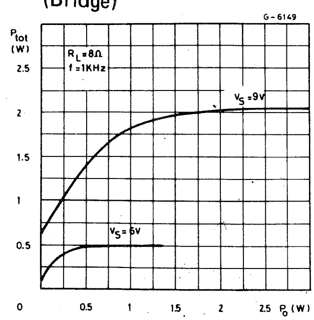


Fig. 13 - Total power dissipation vs. output power (Bridge)



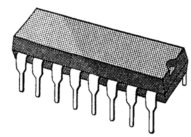
SGS-THOMSON
MICROELECTRONICS

TDA3190

COMPLETE TV SOUND CHANNEL

The TDA3190 is a monolithic integrated circuit in a 16-lead dual in-line plastic package. It performs all the functions needed for the TV sound channel :

- IF LIMITER AMPLIFIER
- ACTIVE LOW-PASS FILTER
- FM DETECTOR
- DC VOLUME CONTROL
- AF PREAMPLIFIER
- AF OUTPUT STAGE



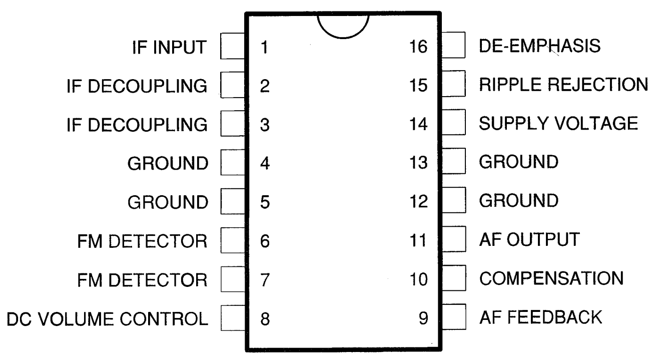
DIP16
(Plastic Package)

ORDER CODE : TDA3190

DESCRIPTION

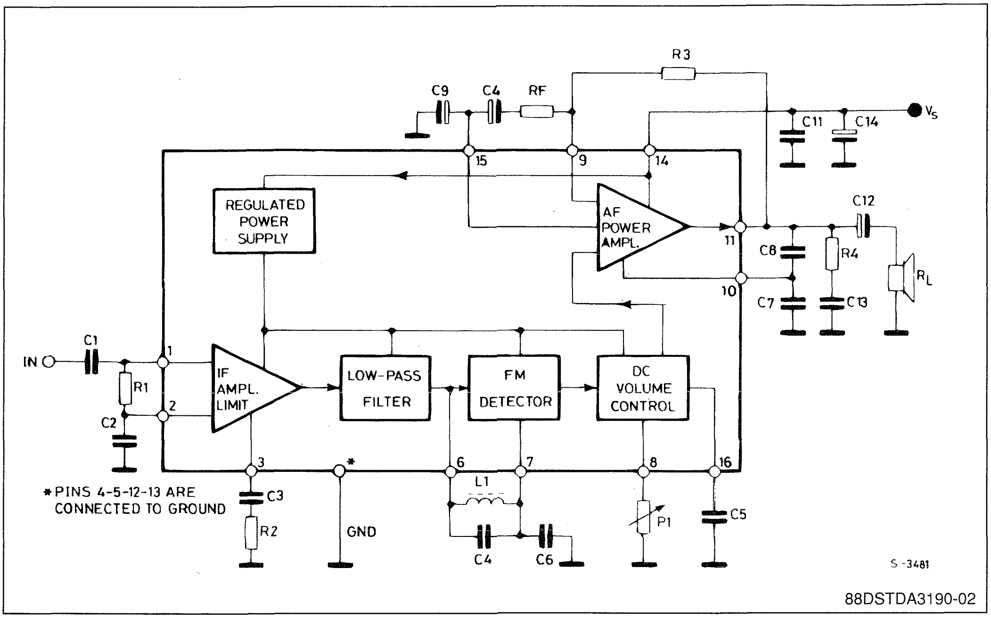
The TDA3190 can give an output power of 4.2 W (d = 10 %) into a 16 Ω load at V_S = 24 V, or 1.5 W (d = 10 %) into an 8 Ω load at V_S = 12 V. This performance, together with the FM-IF section characteristics of high sensitivity, high AM rejection and low distortion, enables the device to be used in almost every type of television receivers.
The device has no irradiation problems, hence no external screening is needed.
The TDA3190 is a pin to pin replacement of TDA1190Z.

PIN CONNECTIONS



91DSTDA3190-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 10)	28	V
V_i	Input Signal Voltage (pin 1)	1	V
I_o	Output Peak Current (non-repetitive)	2	A
I_o	Output Peak Current (repetitive)	1.5	A
P_{tot}	Power Dissipation : at T_{pins} = 90 °C at T_{amb} = 70 °C (free air)	4.3 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

TAB-01

THERMAL DATA

$R_{th\ j\text{-}pins}$ $R_{th\ j\text{-}amb}$	Thermal Resistance Junction-pins Max Thermal Resistance Junction-ambient Max	14 80*	°C/W °C/W

TAB-02

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

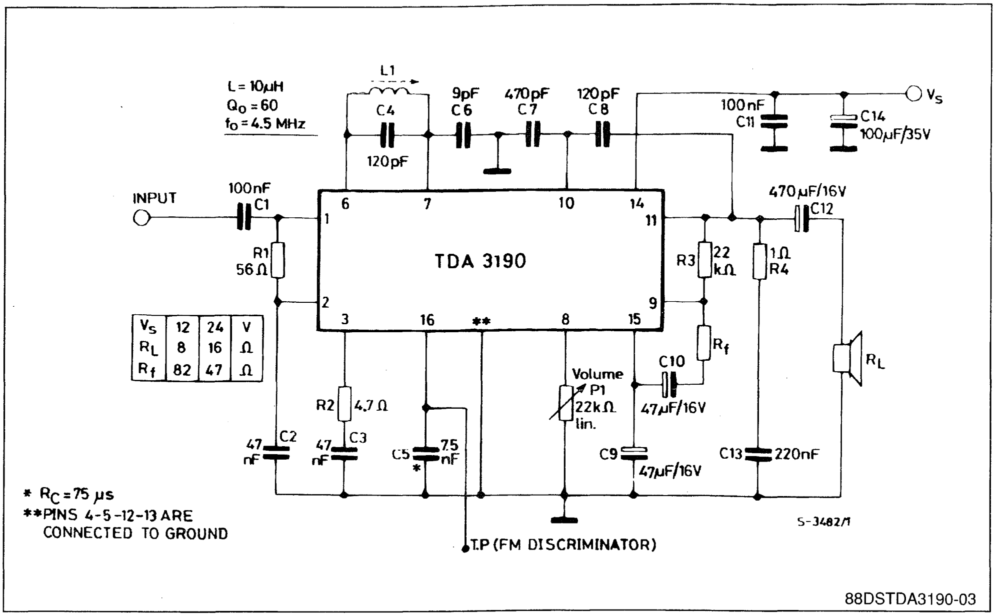
ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_S = 24V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage (pin 14)		9		28	V
V_o	Quiescent Output Voltage (pin11)	V_s = 24 V V_s = 12 V	11 5.1	12 6	13 6.9	V V
I_d	Quiescent Drain Current	P_1 = 22 KΩ V_s = 24 V V_s = 12 V	 11	 22 19	 45 40	 mA mA
Po	Output Power	d = 10 % f_m = 400 Hz f_o = 4.5 MHz Δf = ± 25 KHz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		 4.2 1.5		 W W
		d = 2 % f_m = 400 Hz f_o = 4.5 MHz Δf = ± 25 KHz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		 3.5 1.4		 W W
V_i	Input Limiting Voltage (– 3dB) atPin 1	f_o = 4.5 MHz Δf = ± 7.5 KHz f_m = 400 Hz P_1 = 0		40	100	μV
d	Distortion	P_o = 50 mW f_m = 400 Hz f_o = 4.5 MHz Δf = ± 7.5 KHz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		 0.75 1		 % %
B	Frequency Response of audio amplifier (– 3 dB)	R_L = 16 Ω C_8 = 120 pF C_7 = 470 pF P_1 = 22 KΩ R_f = 82 Ω R_f = 47 Ω		 70 to 1200 70 to 7000		 Hz Hz
V_o	Recovered Audio Voltage (pin16)	V_i ≥ 1 mV f_o = 4.5 MHz f_m = 400 Hz Δf = ± 7.5 KHz P_1 = 0		120		mV
AMR	Ampliture Modulation Rejection	V_i ≥ 1 mV f_o = 4.5 MHz f_m = 400 Hz Δ_f = ± 25 KHz m = 0.3		55		dB
$\frac{S+N}{N}$	Signal to Noise Ratio	V_I ≥ 1 mV V_o = 4 V f_o = 4.5 MHz f_m = 400 Hz Δf = ± 25 KHz	50	65		dB
R_3	External Feedback Resistance (betweenpins9and11)				25	KΩ
R_i	Input Resistance (pin1)	V_i = 1 mV fo = 4.5 MHz		30		KΩ
C_i	Input Capacitance (pin1)			5		pF
SVR	Supply Voltage Rejection	R_L = 16 Ω f_{ripple} = 120 Hz P_1 = 22 KΩ		46		dB
A_v	DC Volume Control Attenuation	P_1 = 12 KΩ		90		dB

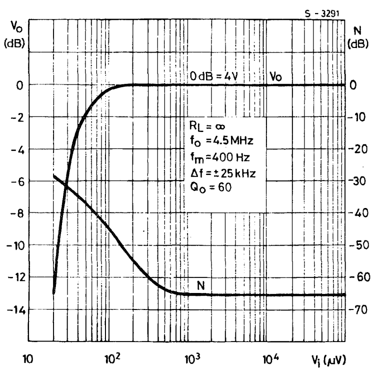
TAB-03

TEST CIRCUIT



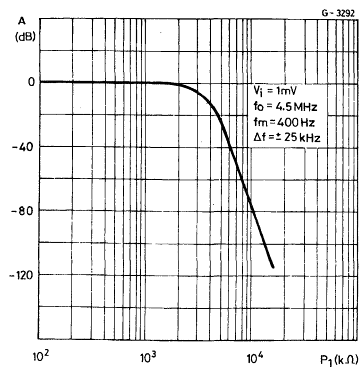
88DSTDA3190-03

Figure 1 : Relative Audio Output Voltage and Output Noise vs. Input Signal.



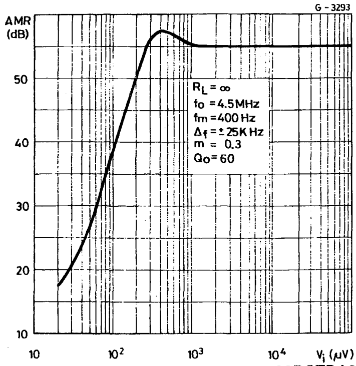
88DSTDA3190-04

Figure 2 : Output Voltage Attenuation vs. DC Volume Control Resistance.



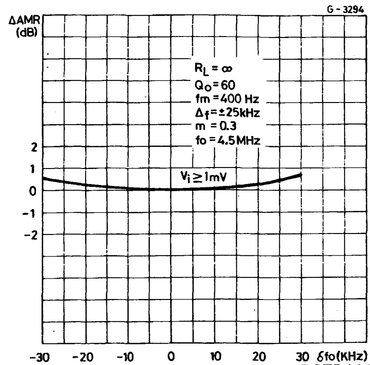
88DSTDA3190-05

Figure 3 : Amplitude Modulation Rejection vs. Input Signal.



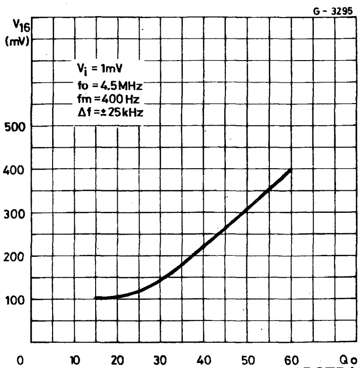
88DSTDA3190-06

Figure 4 : Δ AMR vs. Tuning Frequency Change.



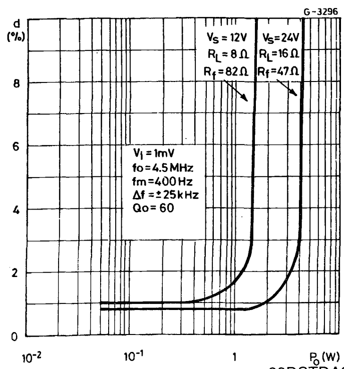
88DSTDA3190-07

Figure 5 : Recovered Audio Voltage vs. Unloaded Q Factor of the Detector Coil.



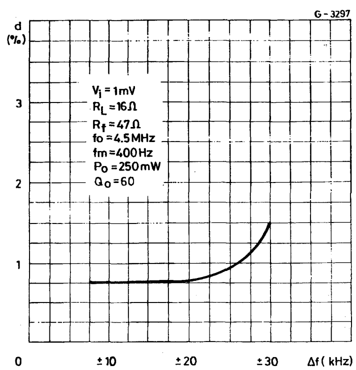
88DSTDA3190-08

Figure 6 : Distortion vs. Output Power.



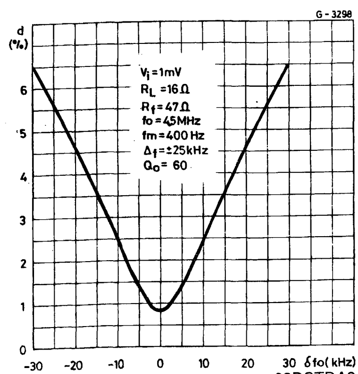
88DSTDA3190-09

Figure 7 : Distortion vs. Frequency Deviation.



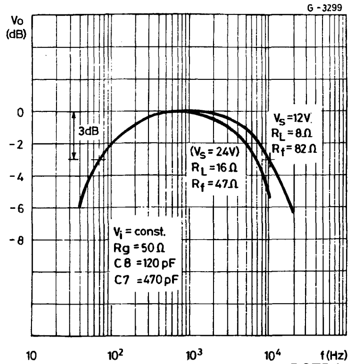
88DSTDA3190-10

Figure 8 : Distortion vs. Tunning Frequency Change.



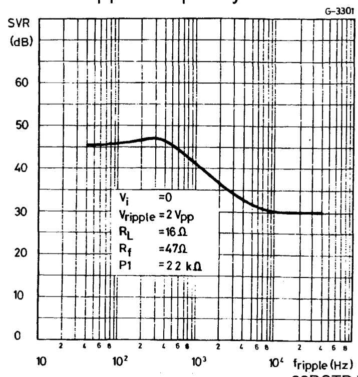
88DSTDA3190-11

Figure 9 : Audio Amplifier Frequency Response.



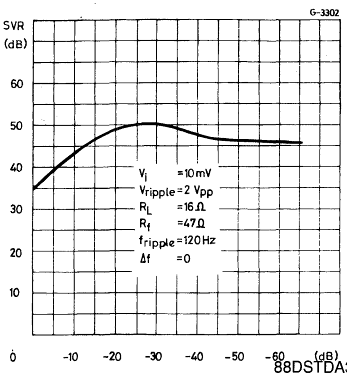
88DSTDA3190-12

Figure 10 : Supply Voltage Ripple Rejection vs. Ripple Frequency.



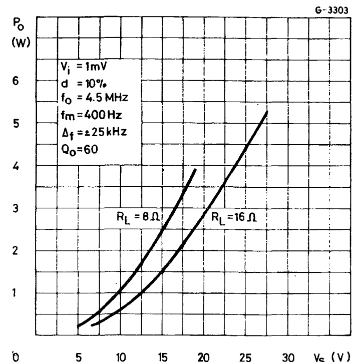
88DSTDA3190-13

Figure 11 : Supply Voltage Ripple Rejection vs; Volume Control Attenuation.



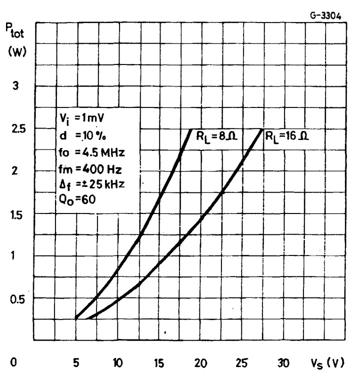
88DSTDA3190-14

Figure 12 : Output Power vs. Supply Voltage.



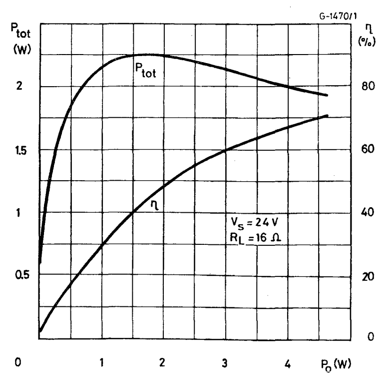
88DSTDA3190-15

Figure 13 : Maximum Power Dissipation vs. Supply Voltage (sine wave operation).



88DSTDA3190-16

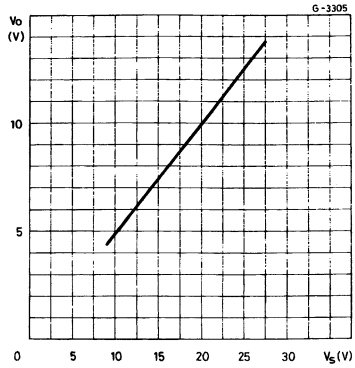
Figure 14 : Power Dissipation and Efficiency vs. Output Power.



88DSTDA3190-17

SGS-THOMSON MICROELECTRONICS

Figure 15 : Quiescent Output Voltage (pin 11) vs. Supply Voltage.



88DSTDA3190-18

APPLICATION INFORMATION

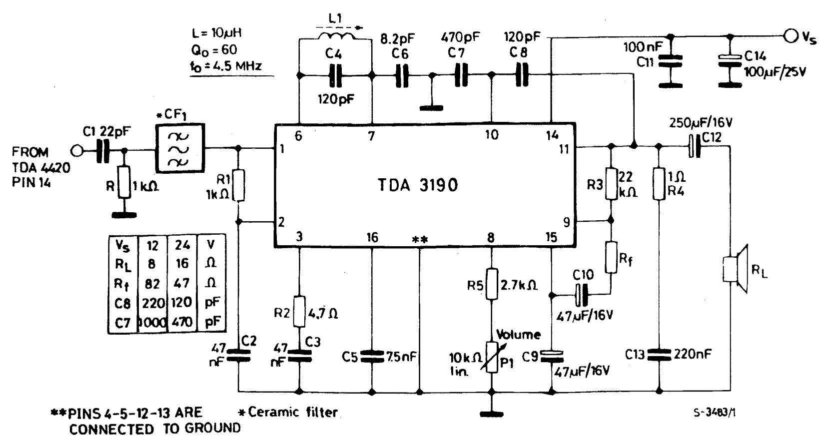
The electrical characteristics of the TDA3190 remain almost constant over the frequency range 4.5 to 6 MHz, therefore it can be used in all television standards (FM mod.). The TDA3190 has a high input impedance, so it can work with a ceramic filter or with a tuned circuit that provide the necessary input selectivity.

The value of the resistors connected to pin 9, determine the AC gain of the audio frequency amplifier. This enables the desired gain to be selected in relation to the frequency deviation at which the output stage of the AF amplifier, must enter into clipping.

Capacitor C8, connected between pins 10 and 11, determines the upper cutoff frequency of the audio bandwidth. To increase the bandwidth the values of C8 and C7 must be reduced, keeping the ratio C7/C8 as shown in the table of fig. 16.

The capacitor connected between pin 16 and ground, together with the internal resistor of 10 KΩ forms the de-emphasis network. The Boucherot cell eliminates the high frequency oscillations caused by the inductive load and the wires connecting the loudspeaker.

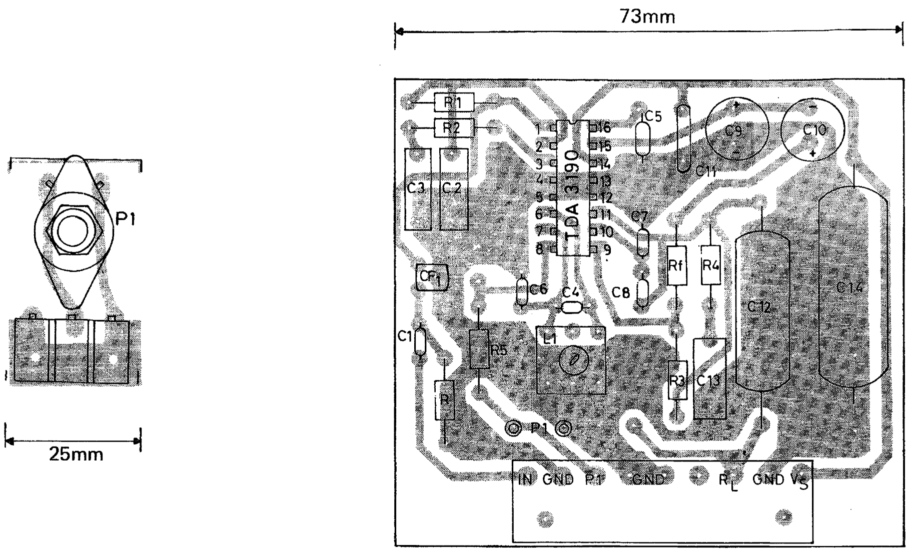
Figure 16 : Typical Application Circuit.



Vs	12	24	V
RL	8	16	Ω
Rf	82	47	Ω
C8	220	120	pF
C7	1000	470	pF

88DSTDA3190-19

Figure 17 : P.C. Board and Component Layout of the Circuit Shown in Fig. 16 (1 : 1 scale).



CS-0097/1

88DSTDA3190-20

MOUNTING INSTRUCTION

The Rth j-amb of the TDA3190 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (fig. 18) or to an external heatsink (fig. 19).
The diagram of figure 20 shows the maximum dissipable power Ptot and the Rth j-amb as a function of the side "l" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 18 : Example of P.C. Board Copper Area which is used as Heatsink.

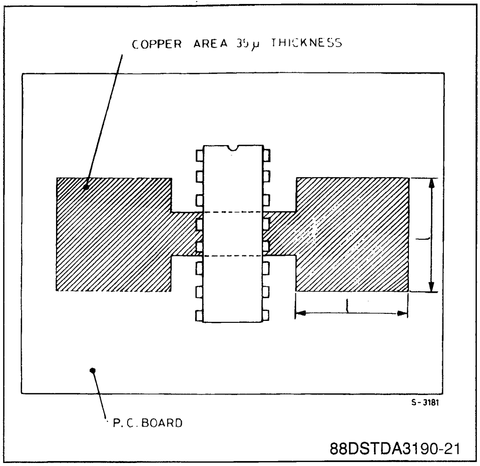


Figure 19 : External Heatsink Mounting Example.

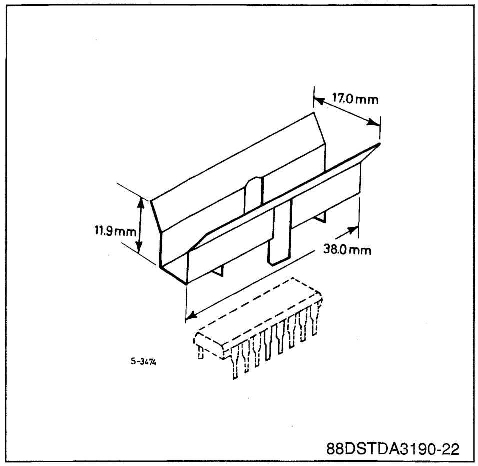
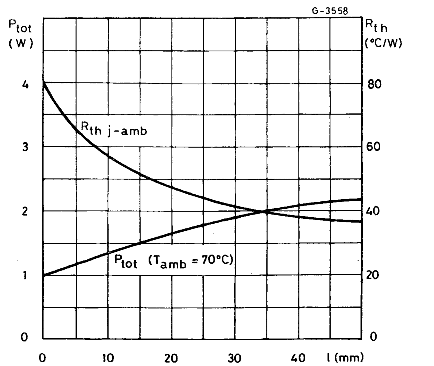
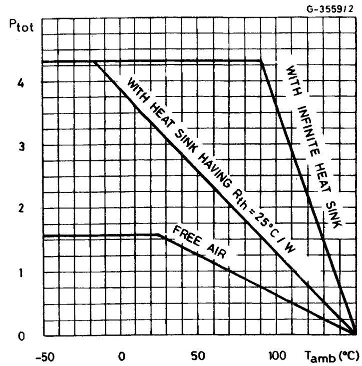


Figure 20 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l"



88DSTDA3190-23

Figure 21 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

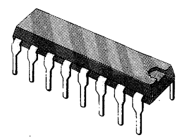


88DSTDA3190-24

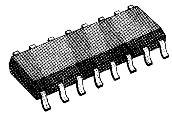
DUAL VERY LOW NOISE PREAMPLIFIER

The TDA 3420D is a dual preamplifier for applications requiring very low noise performance, as **stereo cassette players** and quality audio systems. Each channel consists of two independent amplifiers.
The first one has a fixed gain while the second one is an operational amplifier for audio application.
The TDA 3420D is available in two packages: 16-lead dual in-line plastic and 16 lead micropackage.
Its main features are:

- Very low noise
- High gain
- Low distortion
- Single supply operation
- Large output voltage swing
- Short circuit protection



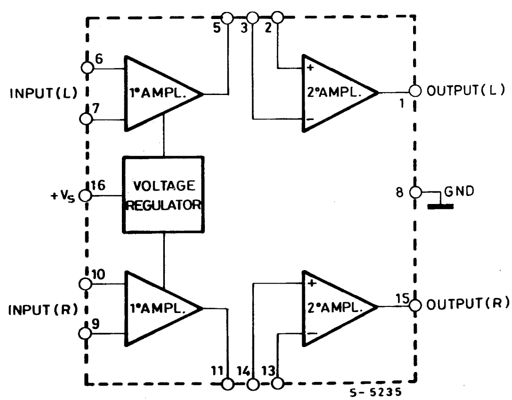
DIP-16 Plastic
(0.4)



SO-16J

ORDERING NUMBER: TDA3420 (DIP-16)
TDA3420D (SO-16)

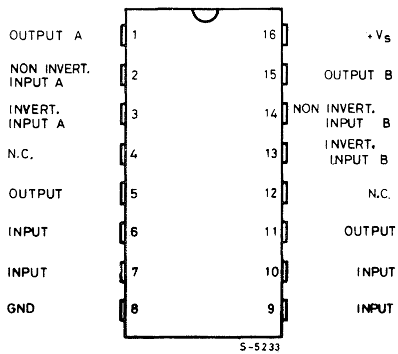
BLOCK DIAGRAM (Pin numbers refer to the DIP)



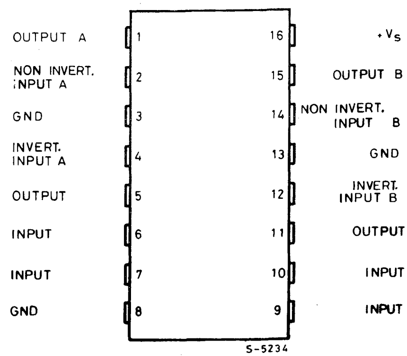
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
P_{tot}	Total power dissipation at T_{amb} = 70°C Dip-16	550	mW
	SO-16	400	mW
T_j, T_{stg}.	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAMS



DIP



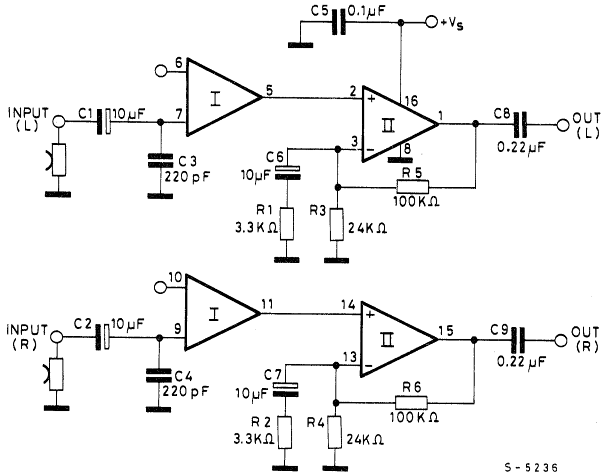
SO-16

THERMAL DATA

			DIP	SO-16
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150 °C/W	200°C/W(*)

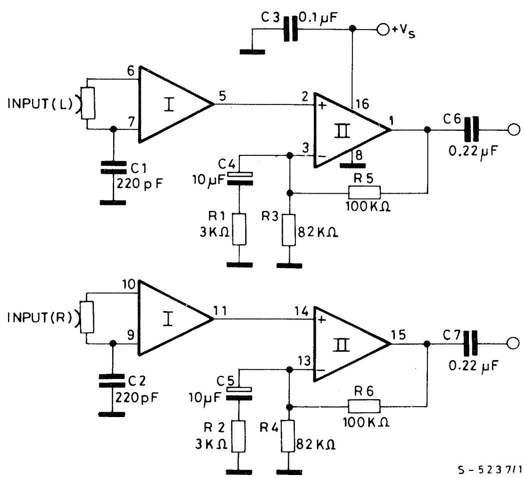
* The thermal resistance is measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

Fig. 1 - Test circuit



Note: Pin numbers refer to DIP.

Fig. 2 - Test circuit without input capacitors



Note: Pin numbers refer to the DIP.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 14.4V, G_v = 60 dB refer to the test circuit of fig. 1, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_s	Supply current	V_s = 8V to 20V			8		mA
I_o	Output current	Source	V_s = 8V to 20V		10		mA
		Sink			1		mA
G_v	Gain	f = 1 KHz			60		dB
R_i	Input resistance			50	100		KΩ
R_o	Output resistance				50		Ω
THD	Total harmonic distortion without noise	V_o = 300 mV	f = 1 KHz		0.05		%
			f = 10 KHz		0.05		%
V_o	Peak to peak output voltage	f = 40 Hz to 15 KHz			12		V
e_n	Total input noise (°)	R_s = 50 Ω R_s = 600 Ω R_s = 5 KΩ			0.25 0.4 1.3	0.7	μV μV μV
S/N	Signal to noise ratio (°)	V_{in} = 0.3 mV V_{in} = 1 mV	R_s = 600 Ω R_s = 0		57 73		dB
	(°°)	V_{in} = 0.3 mV V_{in} = 1 mV	R_s = 600 Ω R_s = 0		55 71		dB
CS	Channel separation	f = 1 KHz			60		dB
SVR	Supply voltage rejection (°°°)	f = 1 KHz	R_s = 600 Ω		110		dB

AMPLIFIER N° 1

G_v	Gain (pin 6 to pin 5)			27.5	28.5	29	dB
d	Distortion	V_o = 300 mV	f = 1 KHz f = 10 KHz		0.05 0.05		%
e_n	Total input noise (°)	R_s = 600Ω			0.4		μV
Z_o	Output impedance (pin 5)	f = 1 KHz			100		Ω
I_o	Output current (pin 5)				1		mA
V5	DC output voltage (pin 5)	Test circuit fig. 2			2.8		V
		Test circuit fig. 1		1.0	1.5		V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
AMPLIFIER N° 2						
G_V	Open loop voltage gain			100		dB
I_B	Input bias current			0.2		μA
V_{os}	Input offset voltage			2		mV
I_{os}	Input offset current			50		nA
e_n	Total input noise (°)	R_s= 600Ω		2		μV
R_i	Input impedance	f = 1 KHz (open loop)	150	500		KΩ

(°) Weighting filter : curve A.
(°°) Weighting filter : Dolby CCIR/ARM.
(°°°) Referred to the input.

Fig. 3 - Total input noise vs. source resistance (curve A)

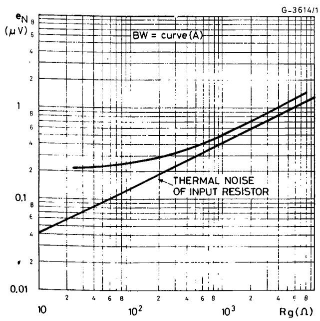


Fig. 4 - Total input noise vs. source resistance(BW=22Hz to 22 KHz)

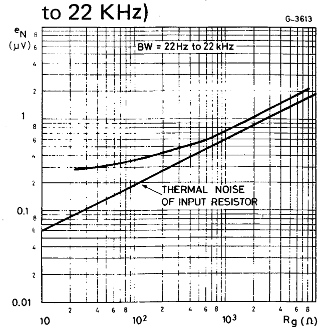


Fig. 5 - Total harmonic distortion vs. output voltage

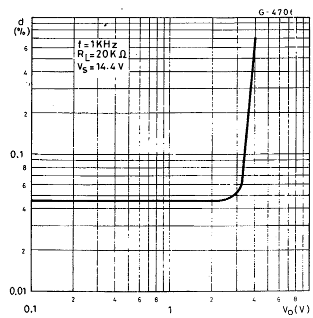


Fig. 6 - Output voltage vs. frequency

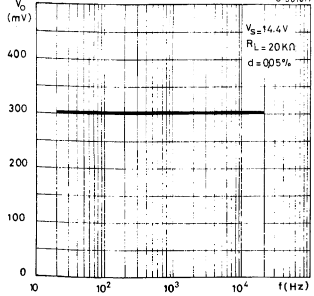


Fig. 7 - Distortion vs. input level (test circuit of fig. 1)

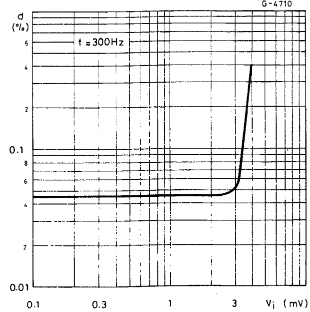
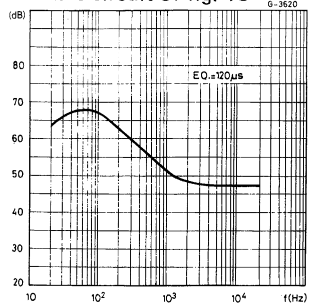


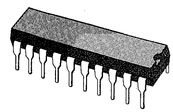
Fig. 8 - Frequency response of the circuit of fig. 10



TV SOUND CHANNEL WITH DC CONTROLS

- INTERNAL VCR INPUT/OUTPUT SWITCHING
- 4W OUTPUT POWER INTO 16Ω
- NO SCREENING REQUIRED
- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- LOW DISTORTION
- DC TONE/VOLUME CONTROLS
- THERMAL PROTECTION

High output, high sensitivity, excellent AM rejection and low distortion make the device suitable for use in TVs of almost every type. Further, no screening is necessary because the device is free of radiation problems.



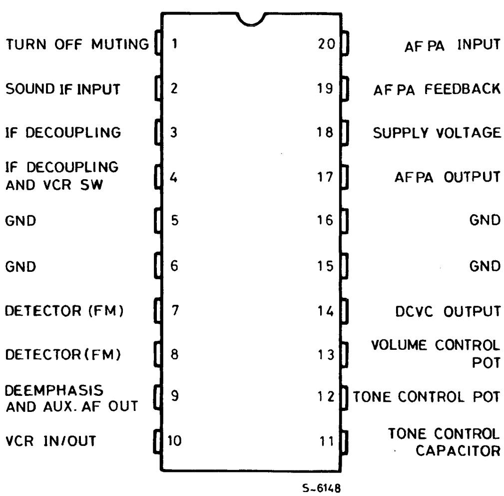
DIP-20
(plastic package)

ORDER CODE : TDA4190A

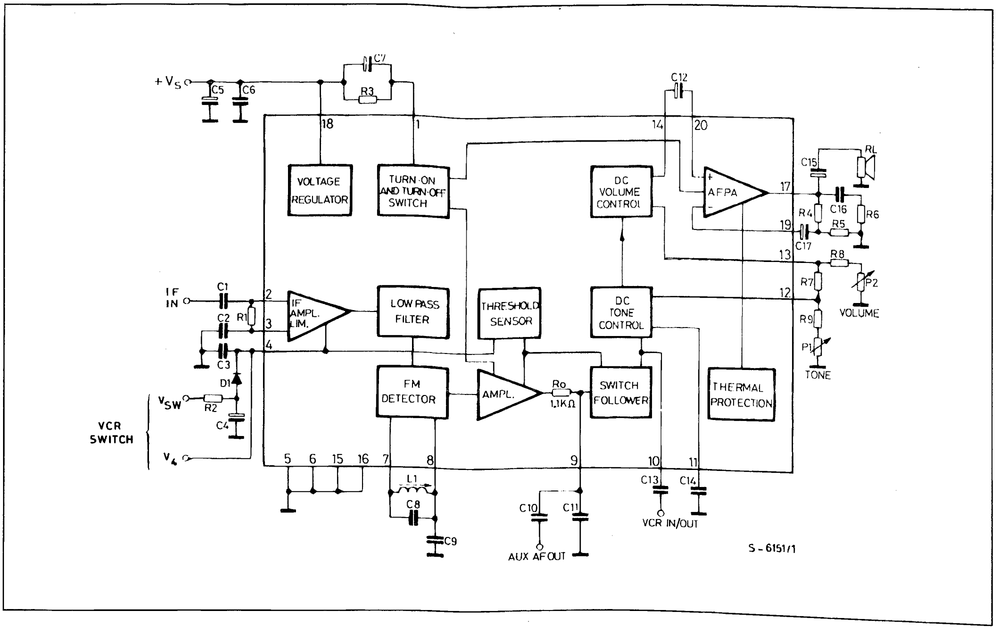
DESCRIPTION

The TDA4190 is a complete TV sound channel with DC tone and volume controls plus an internally switched VCR input/output. Mounted in a Powerdip 16 + 2 + 2 package, the device delivers an output power of 4 W into 16Ω (d = 10%, V_S = 24V) or 1.5W into 8Ω (d = 10%, V_S = 12V). Included in the TDA4190 are : IF amplifier limiter, active low-pass filter, AF preamplifier and power amplifier, turn-off muting, VCR switch, mute circuit and thermal protection.

CONNECTION DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 18)	28	V
V_I	Voltage at pin 1	$\pm V_S$	
V_i	Input Voltage (pin 2)	1	V_{pp}
I_o	Output Peak Current (repetitive)	1.5	A
I_o	Output Peak Current (non repetitive)	2	A
I_4	Current (pin 4)	10	mA
P_{tot}	Power Dissipation : at T_{pins} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W*

(*) Obtained with GND pins soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_s = 24V, V_{sw} = 2V or no V4, Δf = ± 25KHz, R_L = 16Ω, V_i = 1mV, P_1 = 12KΩ, f_o = 4.5MHz, f_m = 400Hz, T_{amb} = 25°C, unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 18)	P_2 = 12 KΩ	10.8		27	V
V_O	Quiescent Output Voltage (pin 18)	P_2 = 12 KΩ	11	12	13	V
V_1	Pin 1 DC Voltage	P_2 = 12 KΩ R_1 = 270 KΩ		5.3		V
V_4	Pin 4 DC Voltage	P_2 = 12 KΩ		3.2		V
I_d	Quiescent Drain Current	P_2 = 12 KΩ		32		mA

IF AMPLIFIER AND DETECTOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{i\ (threshold)}$	Input Limiting Voltage at Pin 2 (– 3 dB)	V_o = 4 V_{rms}		50	100	µV
V_9	Recovered Audio Voltage (pin 9)	Δf = ± 7.5 KHz P_2 = 12 KΩ	140	200	280	mV
AMR	Amplitude Modulation Rejection (*)	m = 0.3 ; V_I = 1 mV ; V_o = 4 V_{rms}		60		dB
R_i	Input Resistance (pin 2)	Δf = 0 P_2 = 12 KΩ		30		KΩ
C_i	Input Capacitance (pin 2)	Δf = 0 P_2 = 12 KΩ		6		pF
R_9	Deemphasis Resistance	C_1 = 68 to 888 nF	0.75	1.1	1.5	KΩ

DC VOLUME CONTROL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Kv	Volume Attenuation (resistance control)	P_2 = 0 KΩ P_2 = 4.3 KΩ P_2 = 12 KΩ	20	0 26 88	32	dB dB dB
Vc	Control Voltage	K = 0 dB K = 26 dB K = 88 dB		0 1.3 2.6		V V V
$\frac{\Delta K_V}{\Delta T_{pins}}$	Volume Attenuation Thermal Drift (resistance control)	T_{pins} 25 to 85 °C P_2 = 4.3 KΩ		– 0.05		$\frac{dB}{°C}$

DC TONE CONTROL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
K_T	Tone Cut	V_{sw} = 8 V or V_4 = 2 V V_{10} = 200 mV P_1 = 12 KΩ to 100 Ω f = 10 KHz		14		dB

ELECTRICAL CHARACTERISTICS (continued)

AUDIO FREQUENCY AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
P_o	Output Power (d = 10 %)	V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω	3.5	4.1 1.5		W W
B	Frequency Response of Audio Amplifier (– 3 dB)	P_o = 1 W R_L = 16 Ω V_{sw} = 8 V or V_4 = 2 V V_{10} = 200 mV V_o = 4 Vrms @ 400 Hz	15	50		KHz
SVR	Supply Voltage Rejection	P_2 = 12 KΩ Δf = 0 f_{ripple} = 120 Hz		26		dB

V.C.R.

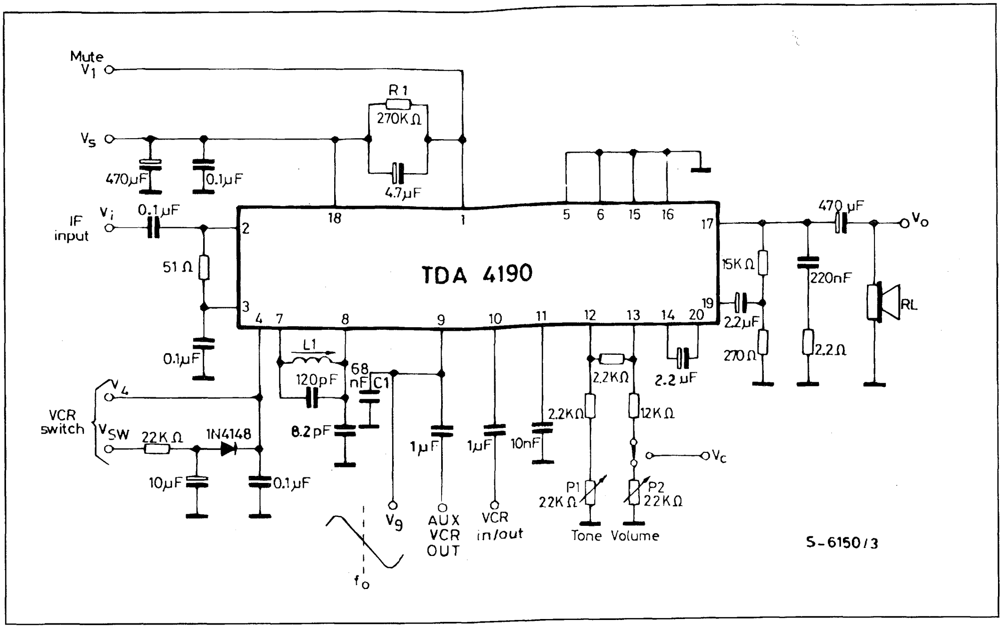
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_4	Input Switching Voltage for Recording for Playback		Floating			
					2	V
V_{sw}	Input Switching voltage for Recording for Playback				2	V
			8			V
V_{10}	Input Voltage (playback)	V_4 = 2 V or V_{sw} = 8 V V_o = 4 V_{rms} P_2 = 0	50	70	100	mV
V_{10}	Output Voltage (recording)	P_2 = 12 KΩ Δf = ± 7.5 KHz	140	200	280	mV
R_{10}	Input Resistance (playback)	V_4 = 2 V or V_{sw} = 8 V	10			KΩ
R_{10}	Output Resistance (recording)	Δf = ± 7.5 KHz, no V_4 or V_{sw} = 2 V			100	Ω
d	Total harmonic Distortion of Pin 10 Output Signal	Δf = ± 7.5 KHz V_i = 1 mV		0.5		%
d	Total Harmonic distortion of 20 dB Over Load V_{10}	V_4 = 2 V V_{sw} = 8 V V_{10} = 1 V_{rms} V_o = 4 V_{rms}		0.5	3	%
SVR	Supply Voltage Rejection at Output Pin 10	Δf = 0 f_{ripple} = 120 Hz P_2 = 12 KΩ		66		dB
$\frac{S+N}{N}$	Signal and Noise Ratio at Output Pin 10	Δf = ± 25 KHz $V_i \geq$ 1 mV		70		dB

OVERALL CIRCUIT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\frac{S+N}{N}$	Signal to Noise Ratio (*)	$V_i \geq$ 1 mV V_o = 4 Vrms Δf = 0		70		dB
d	Distortion (*)	P_o = 50 mW Δf = ± 7.5 Hz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		 0.5 0.5		 % %
M	Muting (*)	V_o = 4 V_{rms} @ no V_1 ; V_1 = 0	100			dB
Δf		P_2 = 0 V_o = 4 Vrms		3	6	KHz

* Test bandwidth = 20 KHz.

TEST CIRCUIT



TEST CONDITIONS (unless otherwise specified)

V_s = 24V ; V_{SW} = 2V or no V4 ; R_L = ∞ ;
V_{in} = 1mV ; Q_o = 60 ; f_o = 4.5MHz ;
P_1 = 12KW ; f_m = 400Hz ; Δf = ± 25KHz.

Figure 1 : Relative Audio Output Voltage and Output Noise vs. Input Signal.

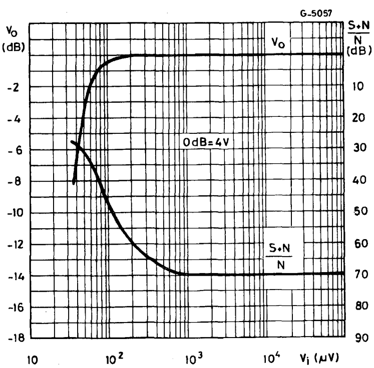


Figure 2 : Output Voltage Alternance vs. DC Volume Control Resistance (a) or Vs. DC Volume Control Voltage (b).

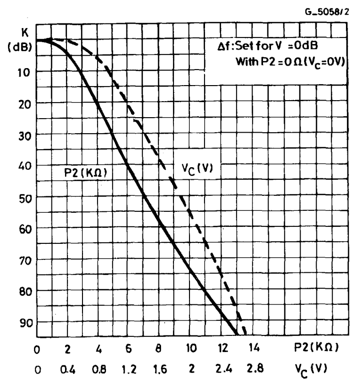


Figure 3 : DC Tone Control Cut of the High Audio Frequencies for some Values of Resistance Adjusted by P1.

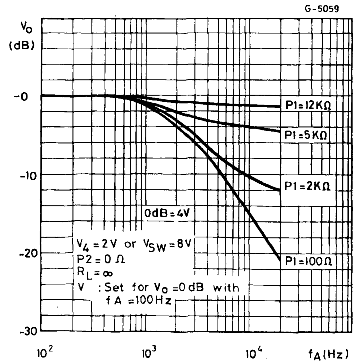


Figure 4 : Amplitude Modulation Rejection vs. Input Signal.

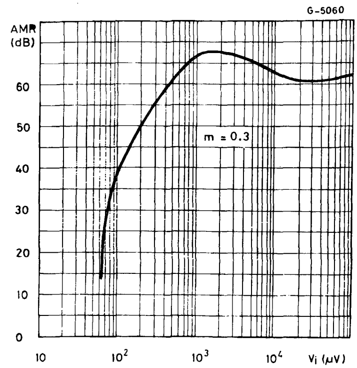


Figure 5: Δ AMR vs. Tuning Frequency Change

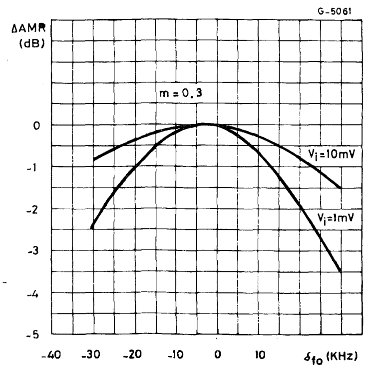


Figure 6 : Recovered Audio Voltage vs. Unloaded Q-factor of the Detector Coil.

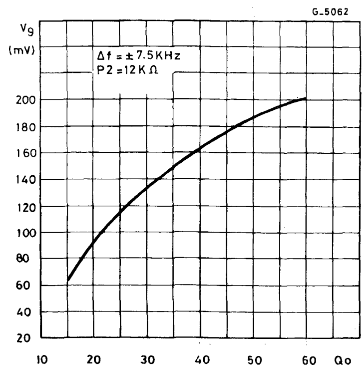


Figure 7 : Distortion vs. Unloaded Q-factor of the Detector Coil.

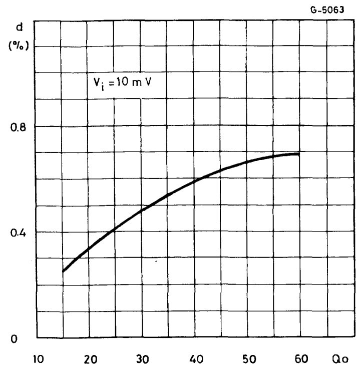


Figure 8 : Distortion vs. Frequency Variation.

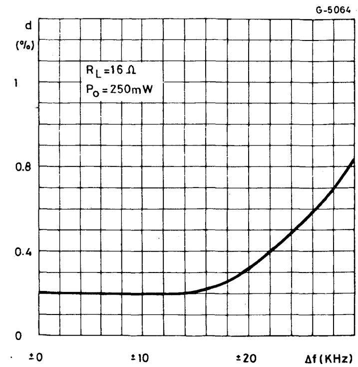


Figure 9 : Distortion vs. Tuning Frequency Change.

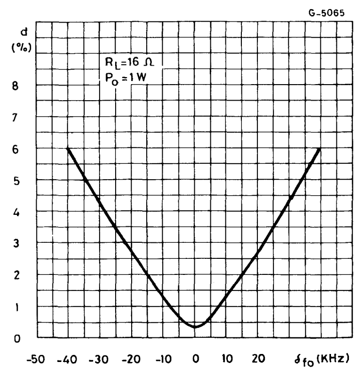


Figure 10 : Distortion vs. Output Power.

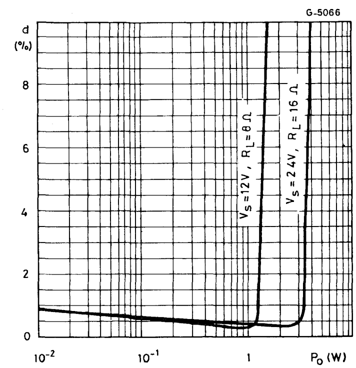


Figure 11 : Audio Amplifier Frequency Response.

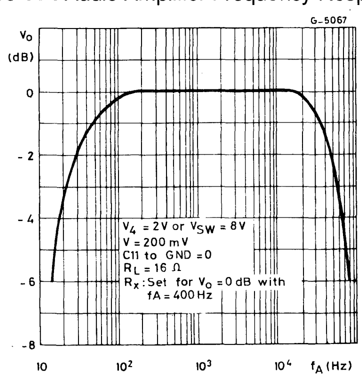


Figure 12 : Output Power vs. Supply Voltage.

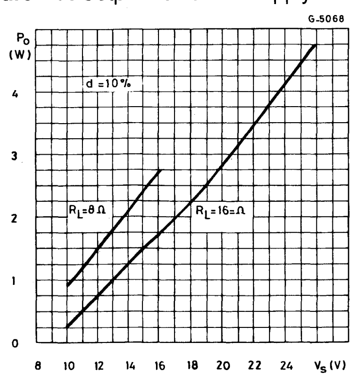


Figure 13 : Power Dissipation vs. Supply Voltage (sine Wave operation).

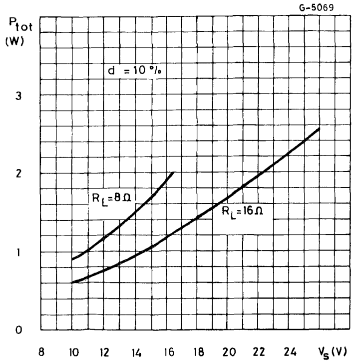


Figure 14 : Power Dissipation and Efficiency vs. Output Power.

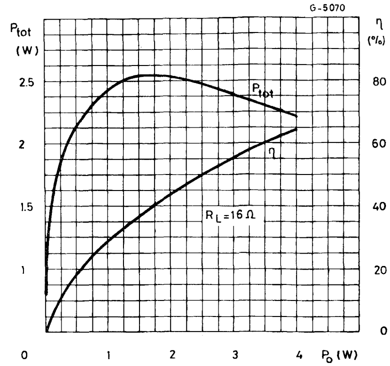
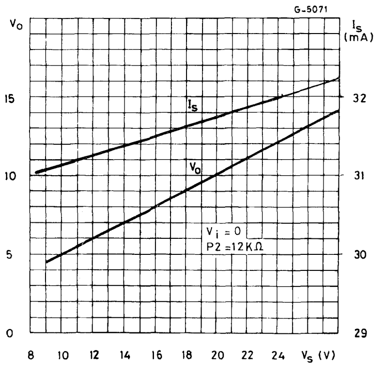


Figure 15 : Quiescent Drain and Quiescent Output Voltage vs. Supply Voltage.



APPLICATION INFORMATION (refer to the block diagram)

IF AMPLIFIER-LIMITER

It is made by six differential stages of 15dB gain each so that an open loop gain of 90 dB is obtained.

While a unity DC gain is provided, the AC closed loop gain is internally fixed at 70dB that allows a typical input sensitivity of 50μV.

The differential output signal is single ended by a 20dB gain amplifier that through a buffer stage, feeds the detector system.

Internal diodes protect the inputs against overloads.

- Pin 2 is the IF non-inverting input
- Pin 3 is decoupled by a capacitor to open the AC loop
- Pin 4 grounded by a capacitor, allows a typical sensitivity of 50μV. (see VCR facility too).

LOW-PASS FILTER, FM DETECTOR AND AMPLIFIER

The IF signal is detected by converting the frequency modulation into amplitude modulation and then detecting it.

Since the available modulated signal is a square wave, a 40dB/decade low-pass filter cuts its harmonics so that a sine wave can feed the two-resonances external network L1, C8 and C9.

This network defines the working frequency value, the amplitude of the recovered audio signal and its distortion at the highest frequency deviations.

The two resonances f1 (series resonance) and f2 (parallel resonance) can be computed respectively by :

$$X_{C9} = \frac{X_{L1} \cdot X_{C8}}{X_{L1} + X_{C8}} \quad \text{and } X_{L1} = X_{C8}$$

The ratio of these frequencies defines the peak-to-peak separation of the "S" curve :

$$\frac{f2}{f1} = \sqrt{1 \; \frac{C_9}{C_8}}$$

A differential peak detector detects the audio frequency signal that amplified, reaches the deemphasis network R0 ; C11.

The AF amplifier can be muted (see turn-on and turn-off switch and VCR facility).

- Pin 7 is the output of the low-pass filter and one input of the differential peak detector
- Pin 8 is the other input of the differential peak detector
- Pin 9 is used to provide the required deemphasis time constant by grounding it with C11. At this pin, the internal impedance of which is typically of 1.1 KΩ, is available the recovered audio signal as auxiliary output.

VCR FACILITY

The deemphathized AF signal reaches the switch follower block can provide to change the impedance of its output depending on the VCR function required.

The switch follower is driven by the threshold sensor block. This one switches both the amplifier and the switch follower by sensing the voltage at pin 4.

When no voltage is forced at pin 4 the function of pin 10 is of VCR output with low impedance ; when the voltage at pin 4 is lower or higher than its quiescent value, the amplifier is muted and the impedance of pin 10 is switched to a high value for a proper VCR input operation.

Since pin 4 reaches also the inverting input of the IF amplifier-limiter, this one can be switched off two for best insulation of the pin 10 with the TV signal path.

So, the VCR facility followed this truth table :

Mode	Vsw	or V_4	Function of Pin 10	Impedance of Pin 10
Recording	≤ 2 V	No One	Output	≤ 100 Ω
Playback	≥ 8 V	≤ 2 V	Input	≥ 10 KΩ

The output signal available when operating during recording is not dependent from both the volume and tone controls while, during playback, the input signal can be regulated by P1 and P2.

Pin 10, as input, can accept until 1 VRMS of overload.

- Pin 4 is the VCR switch driver
- Pin 10 is the VCR input/output pin.

DC TONE CONTROL

The same signal available or applied to pin 10, after a voltage to current converter, reaches, the DC Tone Control block. It operates, inside the 10 KHz bandwidth, by cutting the high audio frequencies with a variable slope of an RC network, by means of P_1

The maximum slope of the RC network is of 20 dB per decade and its pole is defined by :

X_{C11} = 6.8KΩ, typically.
Pin 11 – At this pin is tied the tone capacitor
Pin 12 – is the DC Tone Control input.

DC VOLUME CONTROL

After tone control regulation, the AF current signal reaches the DC volume control block, that controls its intensity. The normal control, for which the block has been designed for a narrow spread, is produced by P2 ; however, without P2, a voltage control can be operated by forcing a voltage at pin 13 through R8.

- Pin 12, already seen as a DCTC input, is the reference voltage for the DCVC. Because of this, a small interface between tone and volume regulation can be expected.
- Pin 13 is the DC volume control input.
- Pin 14 after a current to voltage converter, the audio frequency signal comes out a this pin.

AUDIO FREQUENCY POWER AMPLIFIER AND THERMAL PROTECTION

Through C12 the signal reaches the amplifier non-inverting input. The closed loop gain is defined by the feedback at pin 19 (inverting input) or by the ratio :

$$G_V = 20 \, \text{Log} \, \frac{R5 + R4}{R5} \, (\text{dB})$$

The amplifier, thermally protected, can supply 4 W of power into a 16 Ω load with 24 V of supply voltage. The power output stage is a class B type.

- Pin 20 is the non-inverting input
- Pin 19 is the inverting input
- Pin 17 is the output of the AFPA.

TURN-ON AND TURN-OFF SWITCH

This block has been mainly designed to avoid, turning on the TV set, that transients, produced by the vision output, can reach the speaker.

Moreover this block, together an optimized rise time and full time of the supply voltage V_S, can avoid any pop generally produced during the turn-on and the turn-off transients.

Turning on, pin 1 follows the supply voltage V_S by means of C7 ; a threshold is reached and the muting of the AFPA output (pin 17) is suddenly produced.

When V_S reaches it stop, C7 charges itself through the input impedance of pin 1 and the muting is removed with a time constant depending on the C7 value.

Turning off, the V_S trend, in series to the voltage $V_S - V_1$ and which C7 is charged, drives pin 1 at a low level threshold and a sudden muting is produced again.

Since the turn-off can be operated with high output power, if the muting operates when the current through the inductance of the speaker is different from zero, a flyback is generated and then a small pop can be produced.

The flyback is clipped by integrated diodes.

The threshold that produce the muting have been chosen in the way that 1 Vpp of ripple on the supply voltage does not produce any switching.

By shorting pin 1 to ground through a 10 KΩ resistor the muting can be obtained.

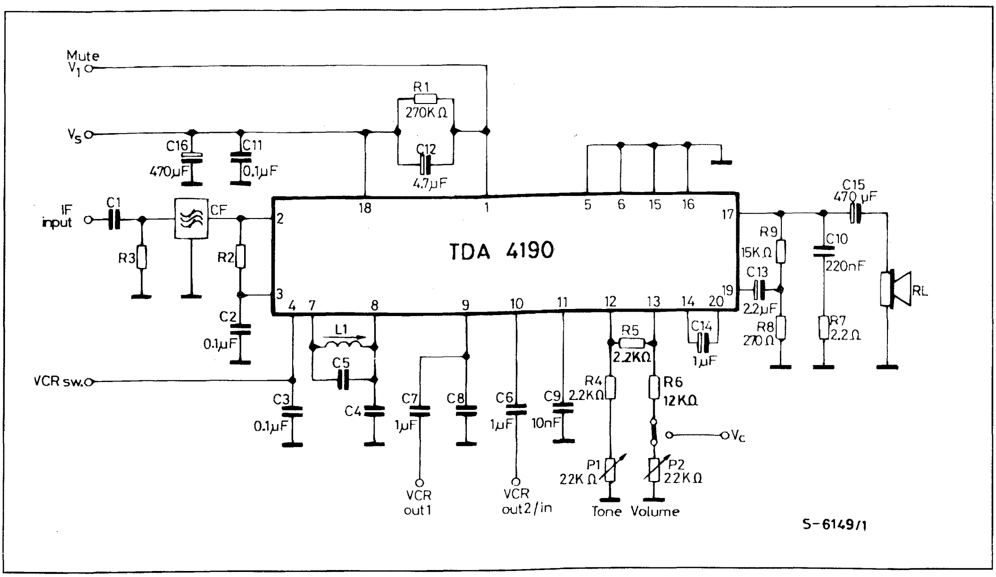
- Pin 1 is the turn-on and turn-off muting input.

SUPPLY

An integrated voltage regulator with different output levels, supplies all the blocks operating with small signal.

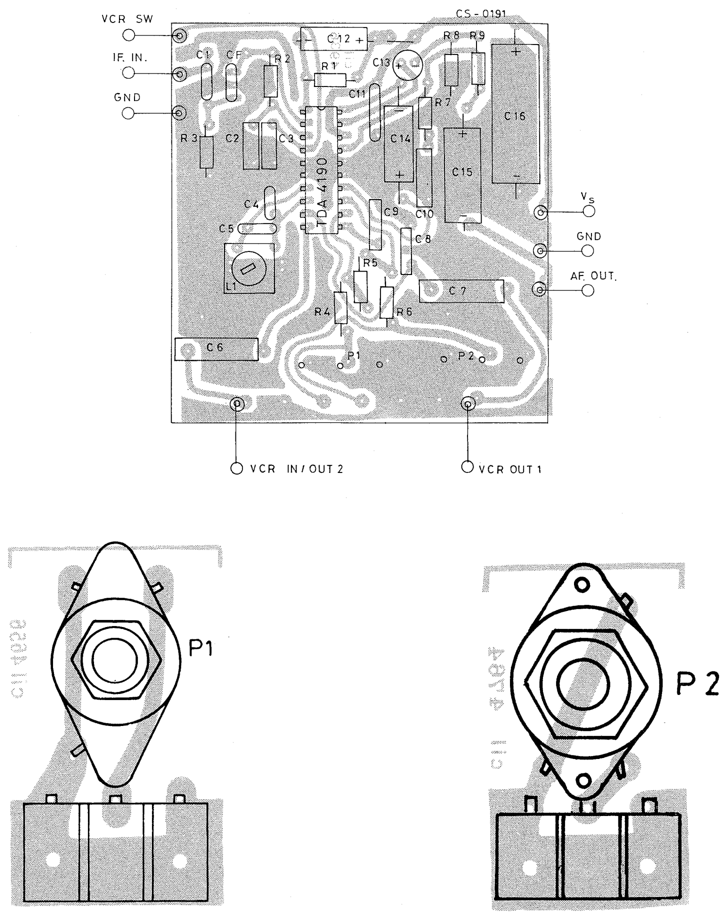
- Pin 18 is the main supply of the device.
- Pin 5 ; pin 6 ; pin 15 and pin 16 are the ground of the supply. These pins are used to drain out from the device the heat produced by the dissipated power.

Figure 16 : Application Circuit.



Components	Units	Appl. 4.5 MHz	Appl. 5.5 MHz	Appl. 6 MHz
L1	µH	10 $Q_0 = 60$	12 $Q_0 = 80$	10 $Q_0 = 70$
C5	pF	120	68	68
C4	pF	9	8.2	6.8
C8	nF	68	47	47
C.F.	–	Murata SFE 4.5 MA	Murata SFE 5.5 MB	Murata SFE 6.0 MB
C1	pF	22	18	18
R2	Ω	1000	560	470
R3	Ω	1000	560	470

Figure 17 : PC Board and Components Layout of the Circuit of Fig. 16 (1 : 1 scale).



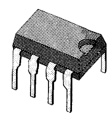
SGS-THOMSON MICROELECTRONICS

TDA7211A

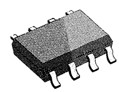
LOW VOLTAGE FM FRONT END

- LOW OSCILLATOR RADIATION
- OPERATING SUPPLY VOLTAGE: 1.3V TO 6V
- EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE
- HIGH SIGNAL HANDLING
- FEW EXTERNAL COMPONENTS
- BUILT-IN VARICAP FOR AFC
- MINIDIP PACKAGE PERMITS RATIONAL LAYOUT AND LOW PROFILE
- COVERS JAPANESE, US AND EUROPEAN BANDS

The TDA7211A is a monolithic FM turner suitable for portable radio and radio/cassette player applications where a very low supply voltage is used and compactness is an important design consideration. It contains an RF amplifier, balanced mixer, one-pin local oscillator and a varicap diode for AFC. Very few external components are required. Mounted in a Minidip or SO-8 package, the TDA7211A is particularly suitable for slimline cassette-type radios.



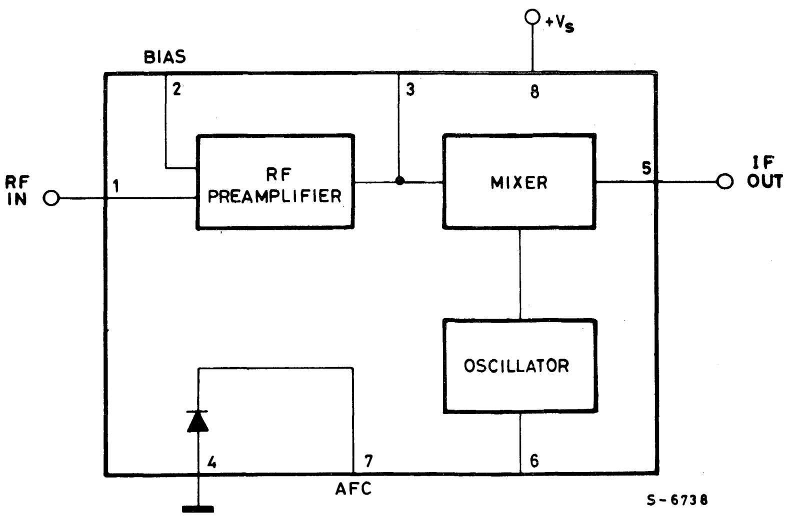
Minidip Plastic



SO-8

ORDERING NUMBER: TDA7211A (Minidip)
TDA7211D (SO-8)

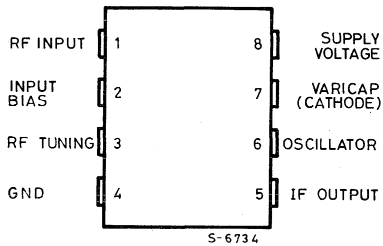
BLOCK DIAGRAM



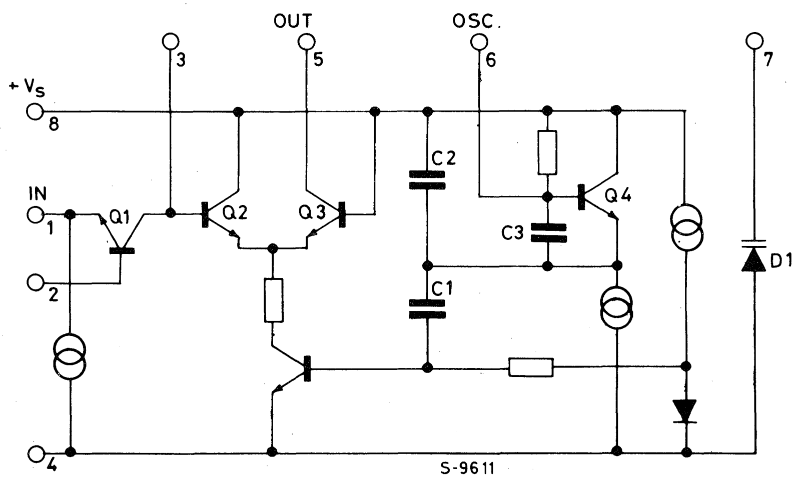
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	7	V
P_{tot}	Total power dissipation at $T_{amb} < 70°C$	400	mW
T_{op}	Operating temperature	-20 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 3V, test circuit of fig. 1, T_{amb} = 25°C, unless otherwise specified)

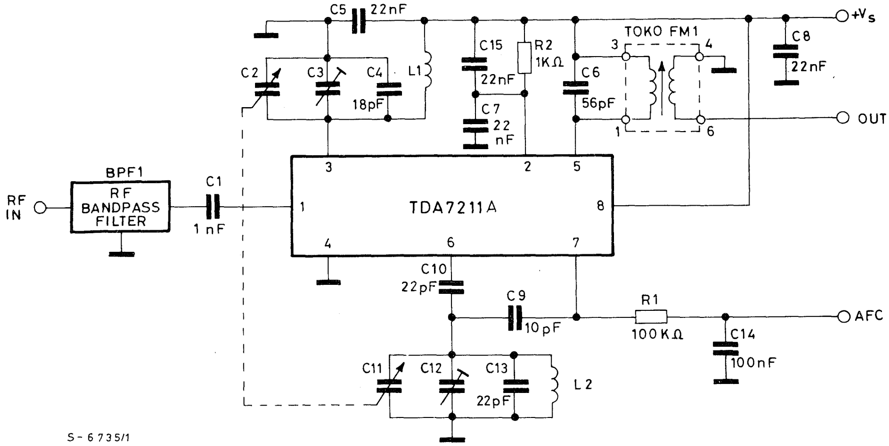
Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			1.3	3	6	V
V_{osc}	Local oscillator voltage					330	mV_{rms}
I_s	Supply current	V_s = 1.5 to 4.5V		2	3	4.5	mA
C_{AFC}	AFC diode capacitance	V_{AFC} = 1V			4		pF
K(*)	AFC diode variation	V_{AFC} = 1 to 3V			0.24		
G_c(**)	Conversion gain	V_s = 3V	f = 83 MHz f = 98 MHz	25 25	34 34		dB
		V_s = 1.6V	f = 83 MHz f = 98 MHz		32 32		dB
V_{STP}	Local oscillator stop voltage				1.2		V

(*) $K = \frac{C\,(1V) - C\,(3V)}{C\,(3V)}$ (**) $R_i = 75\Omega$; $R_L = 300\Omega$

TYPICAL DC VOLTAGES (test circuit)

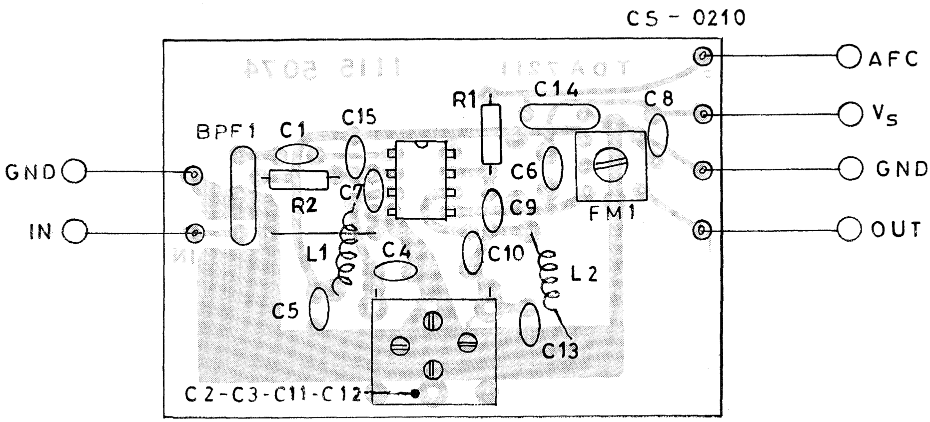
Pin	1	2	3	4	5	6	7	8
(V)	2.3	3	3	0	3	2.9	0	3

Fig. 1 - Test circuit



BPF1 = TAIYO YUDEN - B10861
C_V = C2, C3, C11, C12 = 20 + 20 pF
L1 = RF coil - 5 turns - 0.6 mm/4 mm.
L2 = OSC. coil - 4 turns - 0.6 mm/4 mm.

Fig. 2 - P.C. board and components layout of the test circuit (1:1 scale)



APPLICATION INFORMATION

Fig. 3 - Typical application for portable AM/FM radio

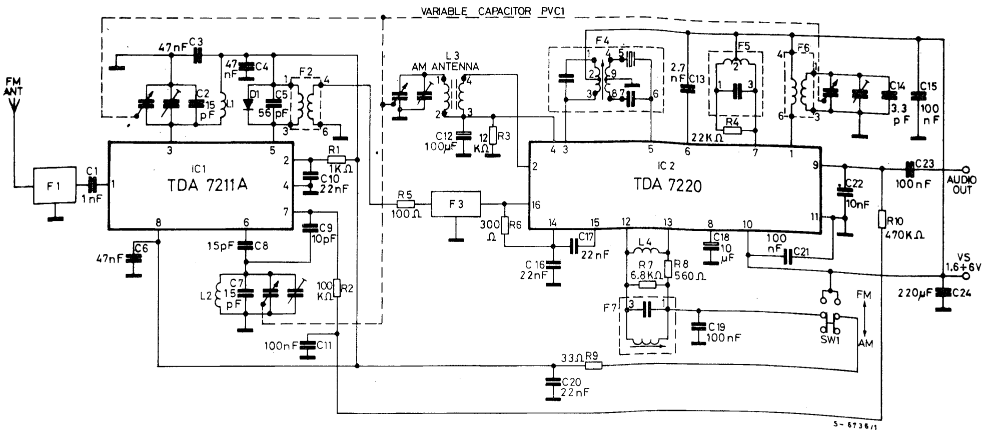
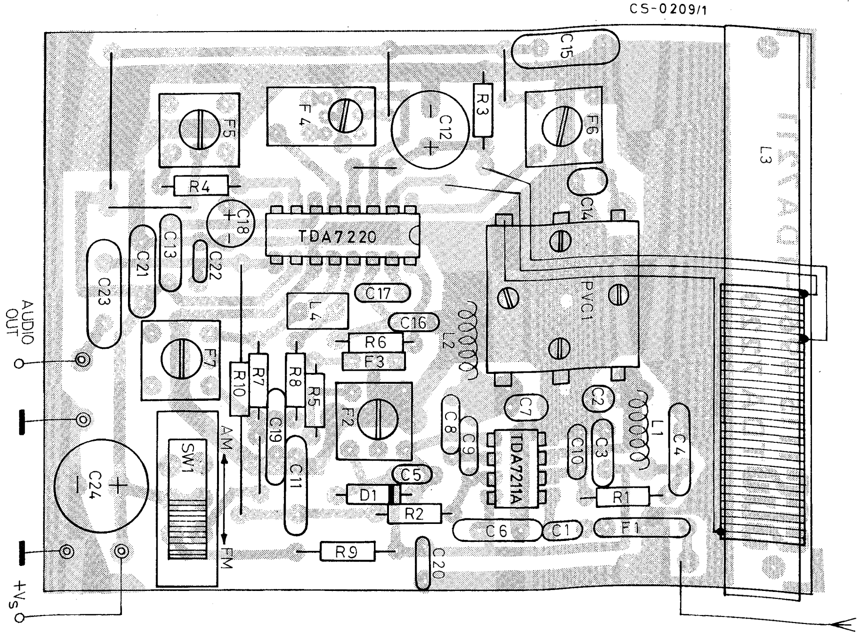


Fig. 4 - P.C. board and components layout of the circuit of fig. 3 (1:1 scale)

CS-0209/1



APPLICATION INFORMATION (continued)

PARTS LIST (Radioreceiver of fig. 3)

Code number	Value	Description
PVC 1	FM 20 pF x 2 AM 140/82 pF	TOKO POLYVARICON QT 22124
L1	ϕ 4 mm. - 5 T # 0.6 mm.	FM RF COIL
L2	ϕ 4 mm. - 4 T # 0.6 mm.	FM OSC. COIL
L3	600 μH PRIMARY SEC. - 7 TURNS	AM ANT. COIL with ferrite bar ϕ 10 mm. x 80 mm.
L4	22 μH INDUCTOR	TOKO 144LY - 220K
D1	AA 119	GE DIODE
F1	TAIYO YUDEN BPF10861K	FM BAND PASS FILTER
F2	TOKO FM1 - 154 AN - 7A5965R	FM IFT
F3	SFE 10.7 MA	CERAMIC FILTER
F4	TOKO CF2 455C	AM IFT WITH CERAMIC FILTER
F5	TOKO AM2 RLC - 4A7524EK	AM DET. COIL
F6	TOKO RWO - 6A6574N	AM OSC. COIL
F7	TOKO KACS - K586HM	FM DIS. COIL

Typical performance of the radio receiver of fig. 3

Parameter		Test conditions		V_s = 3V	V_s = 1.6V
WAVEBANDS	FM			87 to 109 MHz	
	AM			523 to 1620 KHz	
SENSITIVITY	FM	S/N = 26 dB	Δf = ± 22.5 KHz	1.8 μV	2 μV
	AM	S/N = 20 dB	m = 0.3	400 μV	400 μV
AUDIO SIGNAL OUT	FM	Δf = ± 22.5 KHz		70 mV	55 mV
	AM	V_i = 1 mV/m	m = 0.3	80 mV	75 mV
DISTORTION (f_m= 1 KHz)	FM	V_i = 1 mV	Δf = ± 22.5 KHz	0.35%	0.5%
			Δf = 75 KHz	0.7%	0.75%
	AM	5 mV/m	m = 0.3	0.8%	0.8%
		100 mV/m	m = 0.8	2%	1.9%
SIGNAL TO NOISE (f_m= 1 KHz)	FM	V_i = 1 mV	Δf = ± 22.5 KHz	50 dB	50 dB
	AM	V_i = 1 mV/m	m = 0.3	33 dB	32 dB
AMPLITUDE MODULATION REJECTION	FM	V_i = 1 mV	Δf = 22.5 KHz m = 0.3	32 dB	31 dB
TWEET	2nd H.	f = 911 KHz		1%	1%
	3rd H.	f = 1370 KHz		0.2%	0.2%
QUIESCENT CURRENT				13.5 mA	12.5 mA

APPLICATION INFORMATION (continued)

Inversion of "S" shaped curve in quadrature discriminators

In FM receivers, the frequency used for the local oscillator is usually greater than the receiving frequency.
Anyway, in some cases it may be required to work with a local oscillator showing a frequency lower than the frequency of the received signal. According to this choice, the "S" shaped curve of the discriminator is therefore either positive or negative (the output d.c. voltage either increases or decreases as the input frequency increases) and the varicap diode of the AFC will have to be referred either to ground or to a reference voltage. The additional reference voltage may be circuitally unsuitable, besides increasing the costs. In the case of circuits using the monolithic tuner TDA7211 (internal varicap diode, with a side already connected to ground) the things would get still more complicated.
To overcome the problem, figure 5 shows a simple circuit solution to perform the inversion. The traditional diagram is shown in figure 6 for comparision.

This solution may be used with all the SGS-THOMSON radio circuits (TDA7220, TDA1220B, etc.) with performance equal to that achieved through the conventional circuitry.

In the diagram shown, the inversion of the curve is obtained through the replacement of the inductive reactance (normally 22 μH) with a capacitance (12 pF) and the recovery of the d.c. voltages through L3.
L3, which is forced to resonance and strongly smoothed by R1, also performs the function of resistive load across the collector of the output transistor in IF limiter.
The described circuit doesn't modify the ease of calibration of the quadrature discriminators, makes the amplitude modulation rejection (AMR) more continuous and significantly reduces the harmonic radiation from the last limiter stage.

Fig. 5

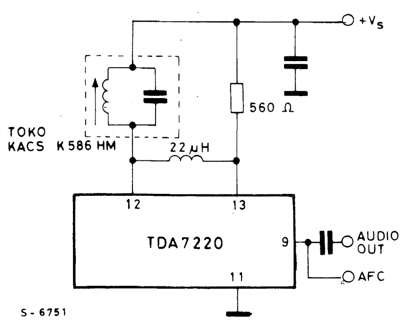
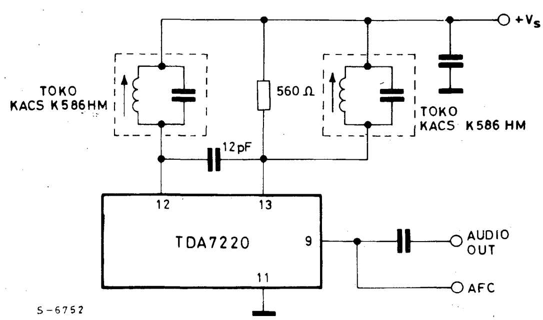


Fig. 6



VERY LOW VOLTAGE AM-FM RADIO

- OPERATING SUPPLY VOLTAGE: 1.5 to 6V
- HIGH SENSITIVITY AND LOW NOISE
- LOW BATTERY DRAIN
- VERY LOW TWEET
- HIGH SIGNAL HANDLING
- VERY SIMPLE DC SWITCHING OF AM-FM
- AM SECTION OPERATES UP TO 30 MHz

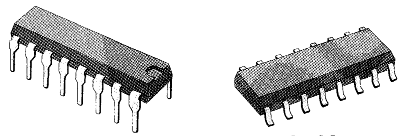
The TDA 7220 is a monolithic integrated circuit in a 16-lead dual in-line plastic package designed for use in 3V, 4.5V and 6V portable AM-FM radio receivers.
The functions incorporated are:

AM SECTION

- Preamplifier and double balanced mixer with AGC
- On pin local oscillator
- IF amplifier with internal AGC
- Detector and audio preamplifier

FM SECTION

- IF amplifier and limiter
- Quadrature detector
- Audio preamplifier



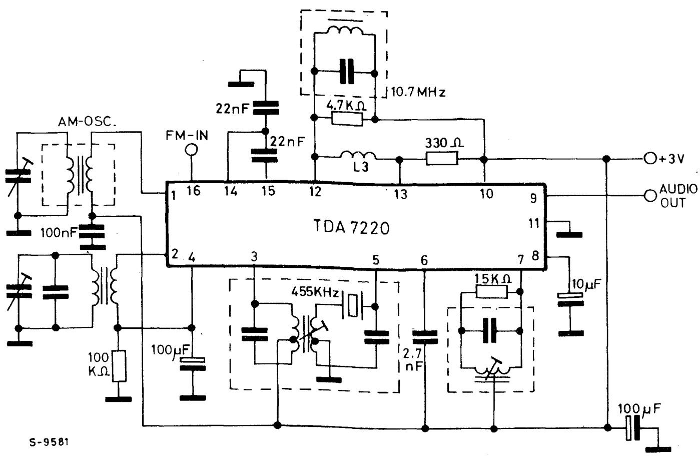
DIP-16 Plastic (0.25) SO-16

ORDERING NUMBERS: TDA7220 (DIP-16)
TDA7220D (SO-16)

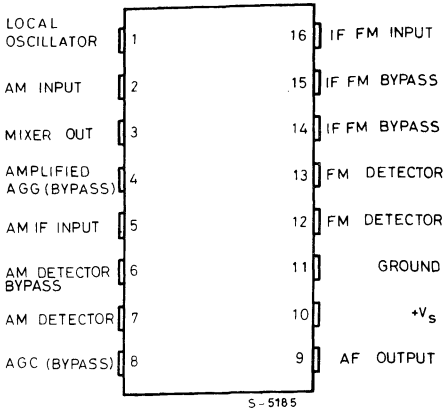
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	6.5	V
P_{tot}	Total power dissipation at $T_{amb} < 110°C$ (DIP-16)	400	mW
T_{op}	Operating temperature	-20 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

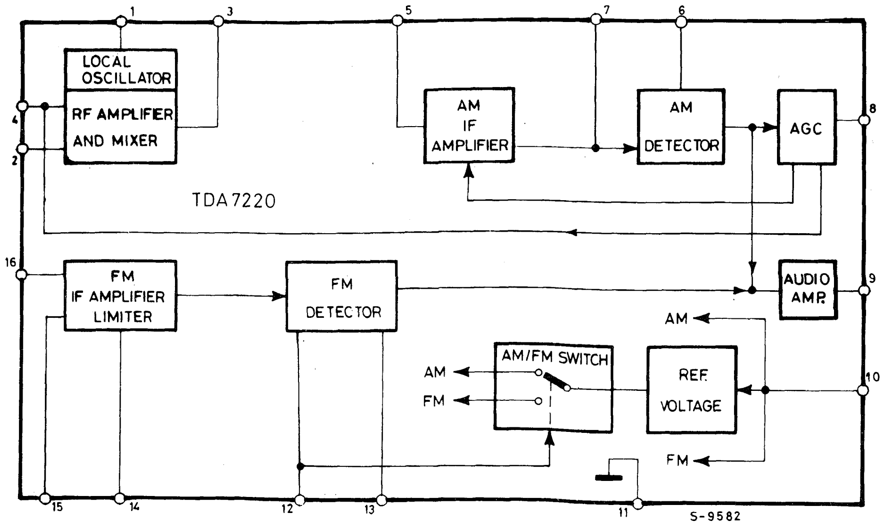
TYPICAL APPLICATION



CONNECTION DIAGRAM



BLOCK DIAGRAM



THERMAL DATA

			DIP-16	SO-16	
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	100	200	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 3V unless otherwise specified, refer to test circuit)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_d	Drain current	AM section			11	18	mA
		FM section			10	15	mA

AM SECTION (f_o = 1 MHz; f_m = 1 KHz)

				Min.	Typ.	Max.	Unit
V_i	Input sensitivity	S/N = 26 dB	m = 0.3		12	25	μV
S/N	Signal to noise	V_i = 1 mV	m = 0.3	40	50		dB
ΔV_i	AGC range	ΔV_{out} = 10 dB	m = 0.8	90			dB
V_o	Recovered audio signal (pin 9)	V_i = 1 mV	m = 0.3	40	80	110	mV
d	Distortion				0.6		%
V_H	Max input signal handling capability	m = 0.8	d < 10%	0.5			V
R_i	Input resistance between pins 2 and 4	m = 0			7.5		KΩ
C_i	Input capacitance between pins 2 and 4	m = 0			18		pF
R_o	Output resistance (pin 9)				4.5		KΩ
	Tweet 2 IF	m = 0.3	V_i = 1 mV		40		dB
	Tweet 3 IF				55		dB

FM SECTION (f_o = 10.7 MHz; f_m = 1 KHz)

				Min.	Typ.	Max.	Unit
V_i	Input limiting voltage	-3 dB limiting point			33	80	μV
AMR	Amplitude modulation rejection	Δf = ± 22.5 KHz V_i = 3 mV	m = 0.3		40		dB
S/N	Signal to noise	Δf = ± 22.5 KHz	V_i = 1 mV	50	65		dB
d	Distortion	Δf = ± 22.5 KHz	V_i = 1 mV		0.3		%
		Δf = ± 75 KHz			1.1	1.5	%
V_o	Recovered audio signal (pin 9)	Δf = ± 22.5 KHz	V_i = 1 mV	40	70	90	mV
R_i	Input resistance between pin 16 and ground				6.5		KΩ
C_i	Input capacitance between pin 16 and ground				14		pF
R_o	Output resistance (pin 9)				4.5		KΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 1.6V unless otherwise specified, refer to test circuit)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_d	Drain current	AM section			8	15	mA
		FM section			7	13	mA

AM SECTION (f_o = 1 MHz; f_m = 1 KHz)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_i	Input sensitivity	S/N = 26 dB	m = 0.3		15	25	μV
S/N	Signal to noise	V_i = 1 mV	m = 0.3	40	48		dB
V_i	AGC range	ΔV_{out} = 10 dB	m = 0.8	90			dB
V_o	Recovered audio signal (pin 9)	V_i = 1 mV	m = 0.3	40	75		mV
d	Distortion				0.5		%
V_H	Max input signal handling capability	m = 0.8	d < 10%	0.5			V
R_i	Input resistance between pins 2 and 4	m = 0			7.5		KΩ
C_i	Input capacitance between pins 2 and 4	m = 0			18		pF
R_o	Output resistance (pin 9)				4.5		KΩ
	Tweet 2 IF	m = 0.3	V_i = 1 mV		40		dB
	Tweet 3 IF				55		dB

FM SECTION (f_o = 10.7 MHz; f_m = 1 KHz)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_i	Input limiting voltage	–3 dB limiting point			50		μV
AMR	Amplitude modulation rejection	$\Delta f = \pm$ 22.5 KHz, V_i = 3 mV	m = 0.3		34		dB
S/N	Ultimate quieting	$\Delta f = \pm$ 22.5 KHz	V_i = 1 mV		55		dB
d	Distortion	$\Delta f = \pm$ 22.5 KHz	V_i = 1 mV		0.6		%
V_o	Recovered audio signal (pin 9)	$\Delta f = \pm$ 22.5 KHz	V_i = 1 mV		55		mV
R_i	Input resistance between pin 16 and ground				6.5		KΩ
C_i	Input capacitance between pin 16 and ground				14		pF
R_o	Output resistance (pin 9)				4.5		KΩ

Fig. 1 - Test circuit

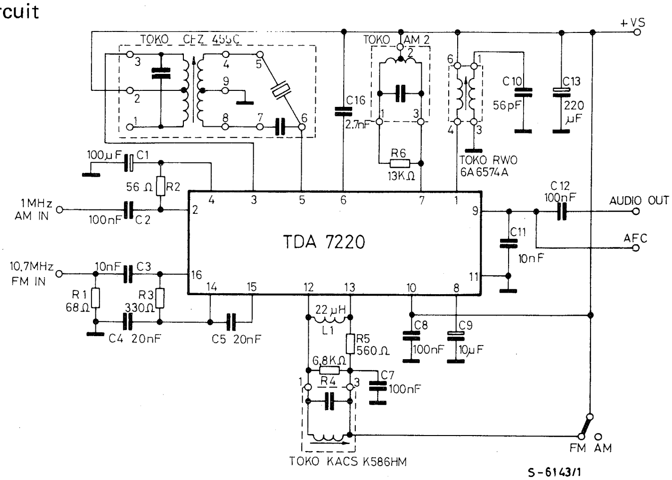
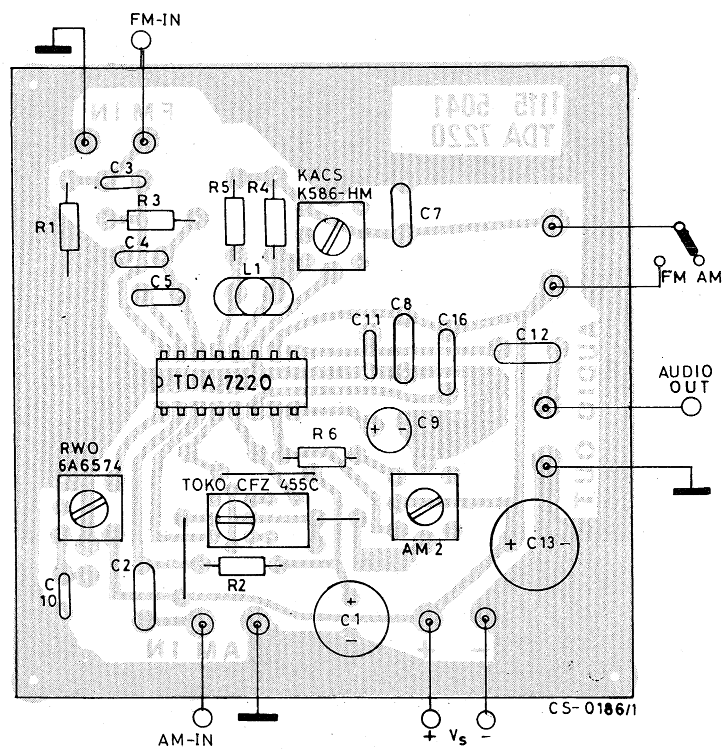


Fig. 2 - PC board and component layout (1:1 scale) of the test circuit



AM-FM SWITCHING

AM-FM switching is achieved by applying a DC voltage at pin 13, to switch the internal reference.

Typical DC voltage (refer to the test circuit)

Pins	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Unit
AM	3	1.1	3	1.1	1.1	2.5	3	0.7	1.2	3	0	2.1	2.1	2.9	3	2.9	V
FM	3	0	3	0	0	2.4	3	0	0.9	3	0	3	3	2.7	2.7	2.7	V

APPLICATION SUGGESTION

Recommended values referred to the test circuit of Fig. 1

Part number	Recommended value	Purpose	Smaller than recommended value	Larger than recommended value
C1	100 μF	AGC bypass	Increase of the distortion at low audio frequency	Increase of the AGC time constant
C2 (*)	100 nF	AM input DC cut		
C3 (*)	10 nF	FM input DC cut		
C4 C5	20 nF 20 nF	FM amplifier bypass	Reduction of sensitivity	– Bandwidth increase – Higher noise
C7	100 nF	FM detector decoupling	Danger of RF irradiation	
C8	100 nF	Power supply bypass	Noise increase of the audio output	
C9	10 μF	AGC bypass	Increase of the distortion at low audio frequency	Increase of the AGC time constant
C10 (*)	56 pF	Tuning of the AM oscillator at 1455 KHz		
C11	10 nF	50 μs FM de-enphasis		
C12	100 nF	Output DC decoupling	Low audio frequency cut	
C13	220 μF	Power supply decoupling	Increase of the distortion at low frequency	
C16	2.7 nF	AM detector capacitor	Low suppression of the IF frequency and harmonics	Increase of the audio distortion
R1 (*)	68 ohm	FM input matching		
R2 (*)	56 ohm	AM input matching		
R3	330 ohm	Ceramic filter matching		
R4	6.8 Kohm	FM detector coil Q setting	Audio output decrease and lower distortion	Audio output increase and higher distortion
R5	560 ohm	FM detector load resistor	Audio output decrease and higher AMR	
R6	13 Kohm	AM detector coil Q setting	Lower IF gain and Lower AGC range	Higher IF gain and lower AGC range

(*) Only for test circuit.

Fig. 3 - Audio output and noise vs. input signal (AM section) $V_s = 3V$

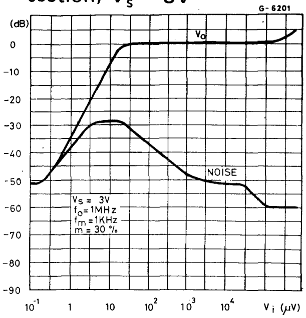


Fig. 4 - Audio output and noise vs. input signal (AM section) $V_s = 1.6V$

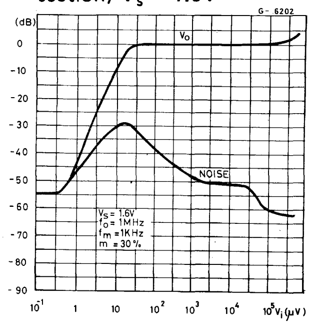


Fig. 5 - Distortion vs. input signal (AM section) $V_s = 3V$

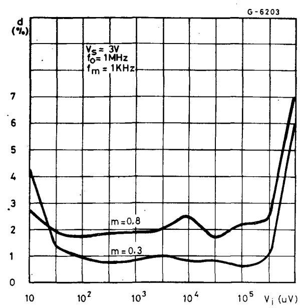


Fig. 6 - Distortion vs. input signal (AM section) $V_s = 1.6V$

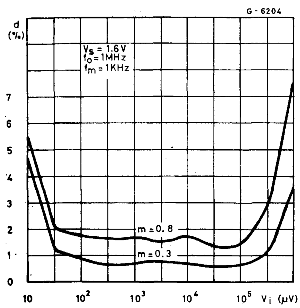


Fig. 7 - Audio output vs. supply voltage (AM section)

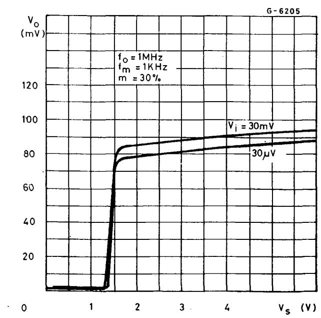


Fig. 8 - Amplified AGC voltage (pin 4) vs. input signal (AM section)

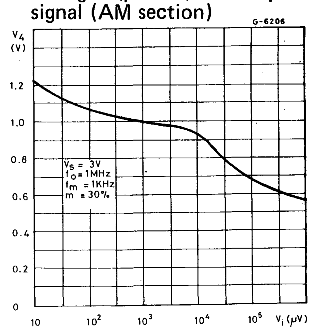


Fig. 9 - Audio output and noise vs. input signal (FM section) $V_s = 3V$

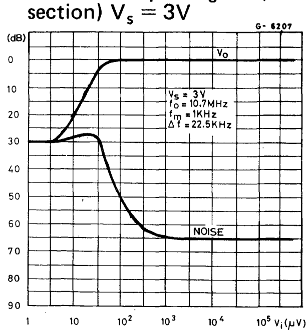


Fig. 10 - Audio output and noise vs. input signal (FM section) $V_s = 1.6V$

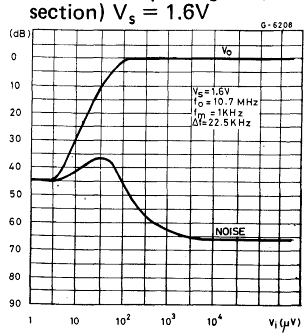


Fig. 11 - Distortion vs. input signal (FM section) $V_s = 3V$

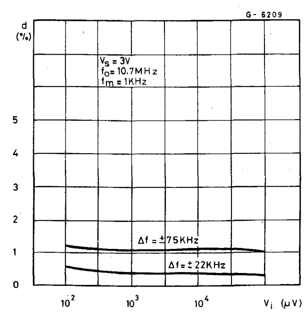


Fig. 12 - Distortion vs. input signal (FM section) $V_s = 1.6V$

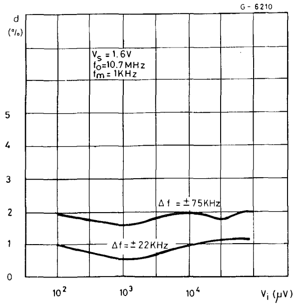


Fig. 13 - Audio output vs. supply voltage (FM section)

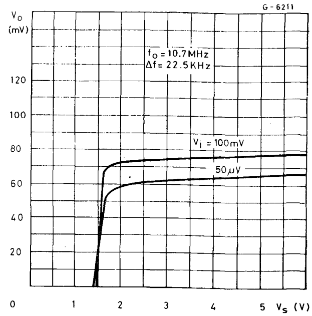


Fig. 14 - Amplitude modulation rejection vs. input signal (FM section)

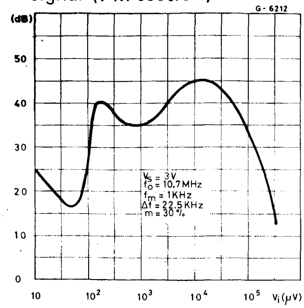


Fig. 15 - DC output voltage (pin 9) vs. supply voltage (FM section)

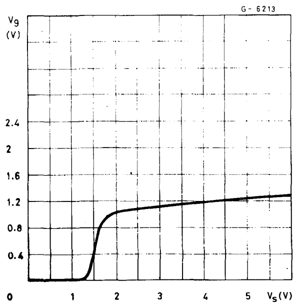


Fig. 16 - AFC output voltage (pin 9) vs. frequency deviation (FM section)

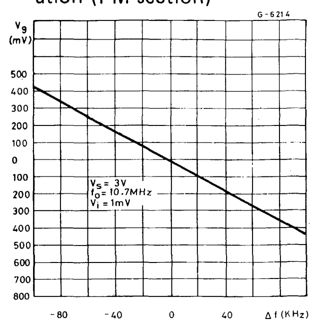
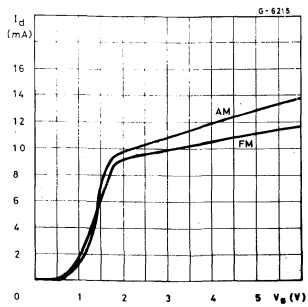
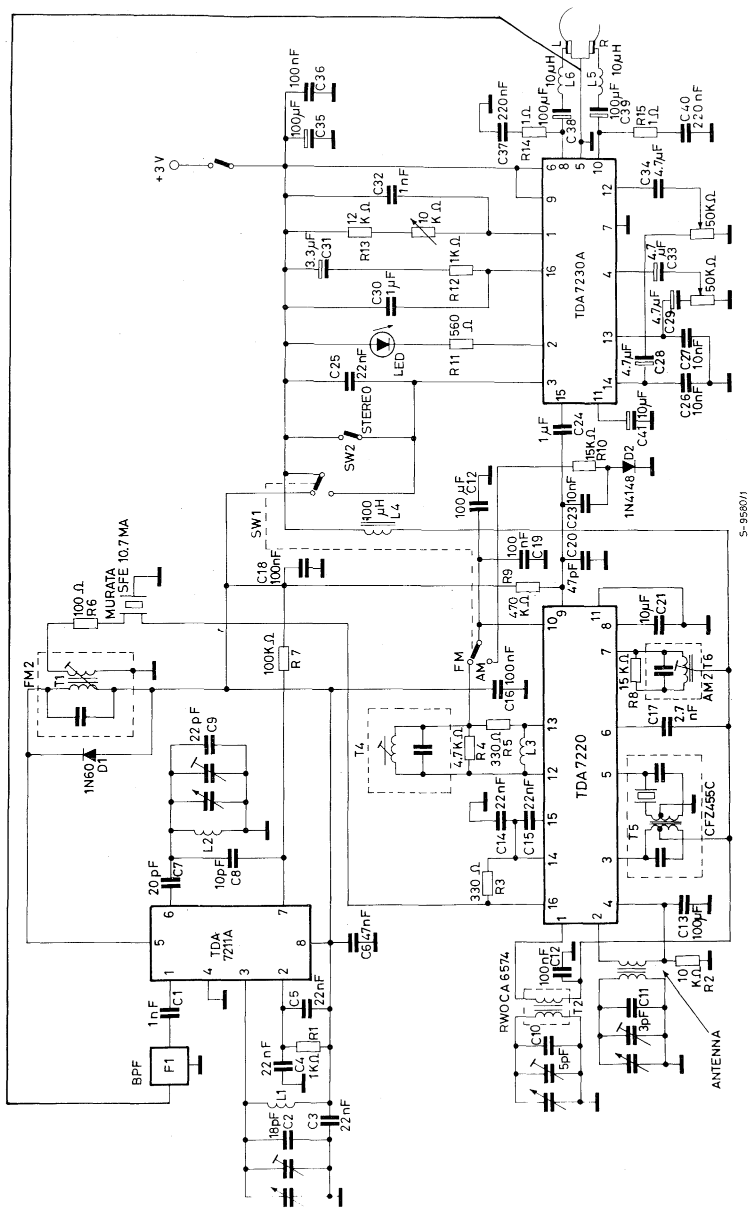


Fig. 17 - Drain current vs. supply voltage



APPLICATION INFORMATION

Fig. 18 - Stereo AM/FM miniradio



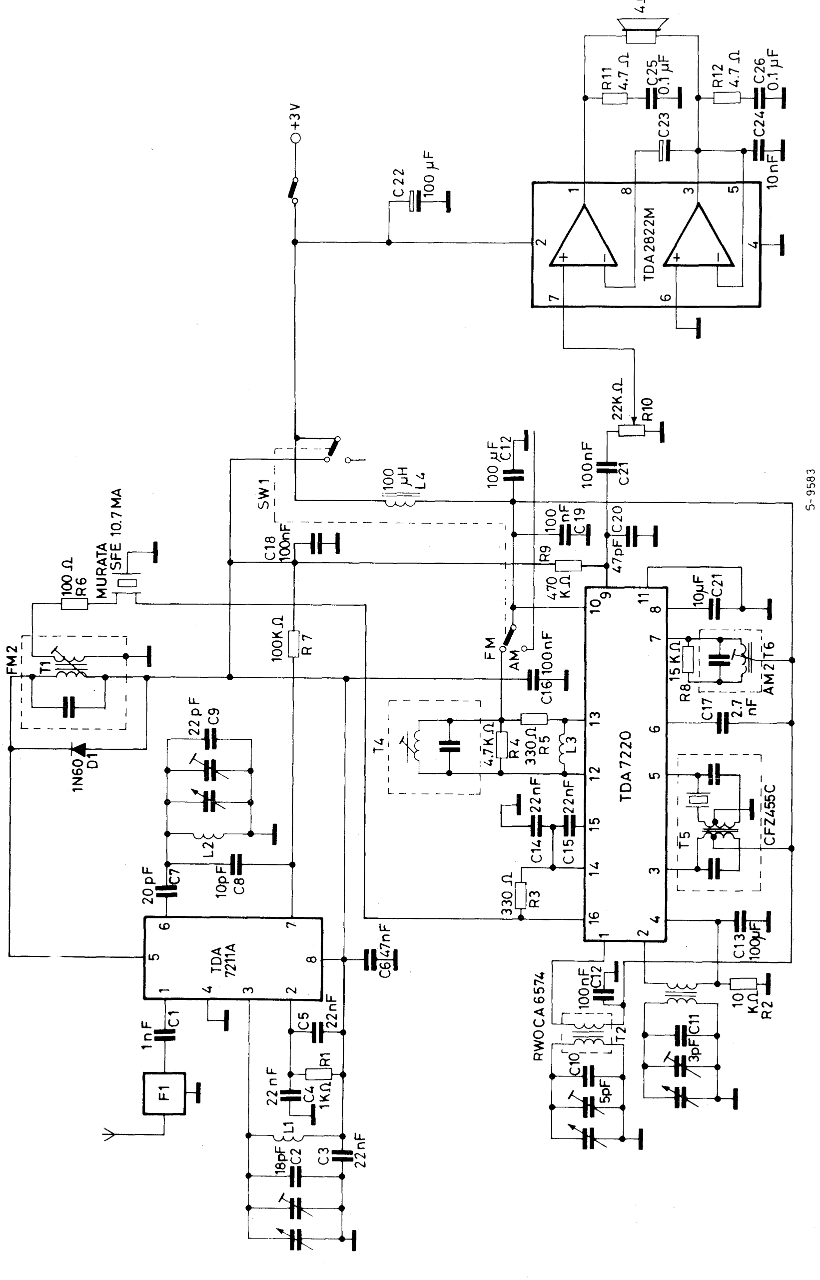
APPLICATION INFORMATION (continued)

Typical performance of the radio receiver of fig. 18 ($V_s = 3V$, $R_L = 32\Omega$)

Parameter		Test Conditions		Value
WAVEBANDS	FM			87.5 to 108 MHz
	AM			510 to 1620 KHz
SENSITIVITY	FM	S/N = 26 dB	Δf = 22.5 KHz	3 μV
	AM	S/N = 6 dB	m = 0.3	2 μV
	AM	S/N = 26 dB	m = 0.3	10 μV
DISTORTION (fm = 1 KHz)	FM	P_o = 20 mW	Δf = 22.5 KHz	0.5%
			Δf = 75 KHz	1.8%
	AM	V_i = 100 μV	m = 0.8	1.1%
SIGNAL TO NOISE (fm = 1 KHz)	FM	P_o = 20 mW V_i = 100 μV	Δf = 22.5 KHz	60 dB
	AM	P_o = 20 mW V_i = 1 mV	m = 0.3	45 dB
AMPLITUDE MODULATION REJECTION	FM	V_i = 100 μV	Δf = 22.5 KHz m = 0.3	40 dB
QUIESCENT CURRENT				16 mA
SUPPLY VOLTAGE RANGE				1.6 to 3V

APPLICATION INFORMATION (continued)

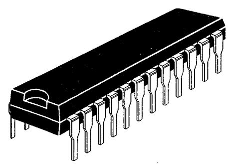
Fig. 19 - 0.3W AM/FM Mono-Radio



3V AM/FM ONE-CHIP RADIO

ADVANCE DATA

- BUILT-IN FM F/E, AM/FM IF AND FM MPX
- AM DETECTOR COIL AND IF COUPLING CAPACITOR ARE NOT NEEDED
- COMPACT PACKAGE : 24-Pin Shrink
- OPERATING SUPPLY VOLTAGE RANGE $V_{CC\ (opr)}$ = 1.8 to 7.0V
- LED DRIVE CIRCUIT FOR TUNING INDICATION



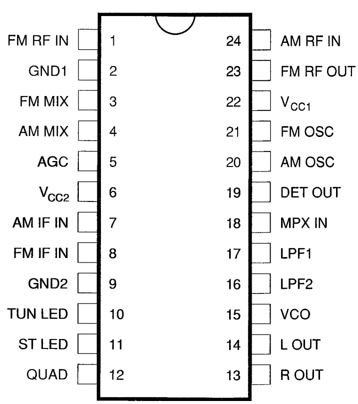
SDIP24
(Plastic Package)

ORDER CODE : TDA7222

DESCRIPTION

TDA7222 is AM/FM chip tuner ICs, which is designed for portable radios and 3V headphone radios.

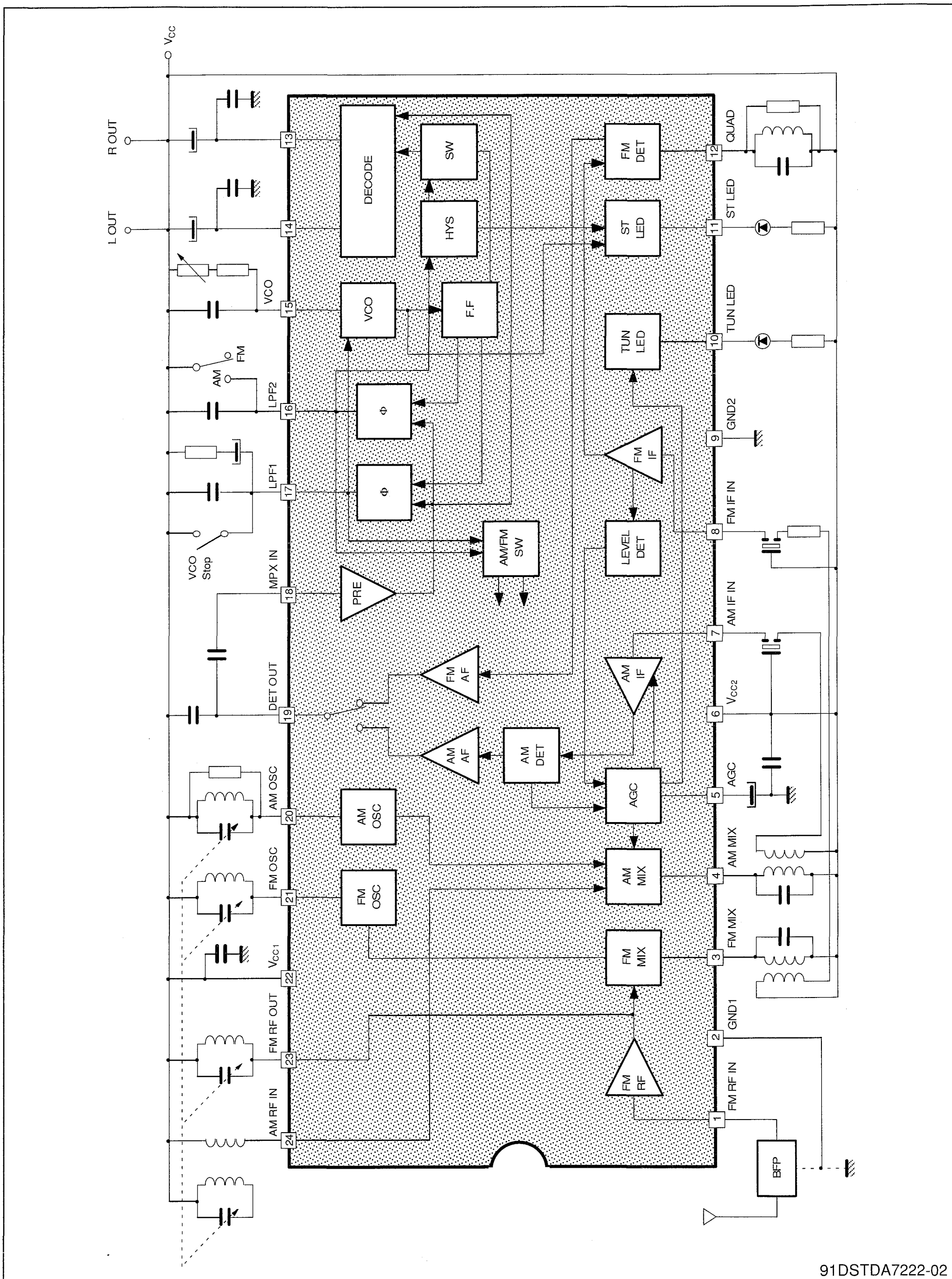
PIN CONNECTIONS



91DSTDA7222-01

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



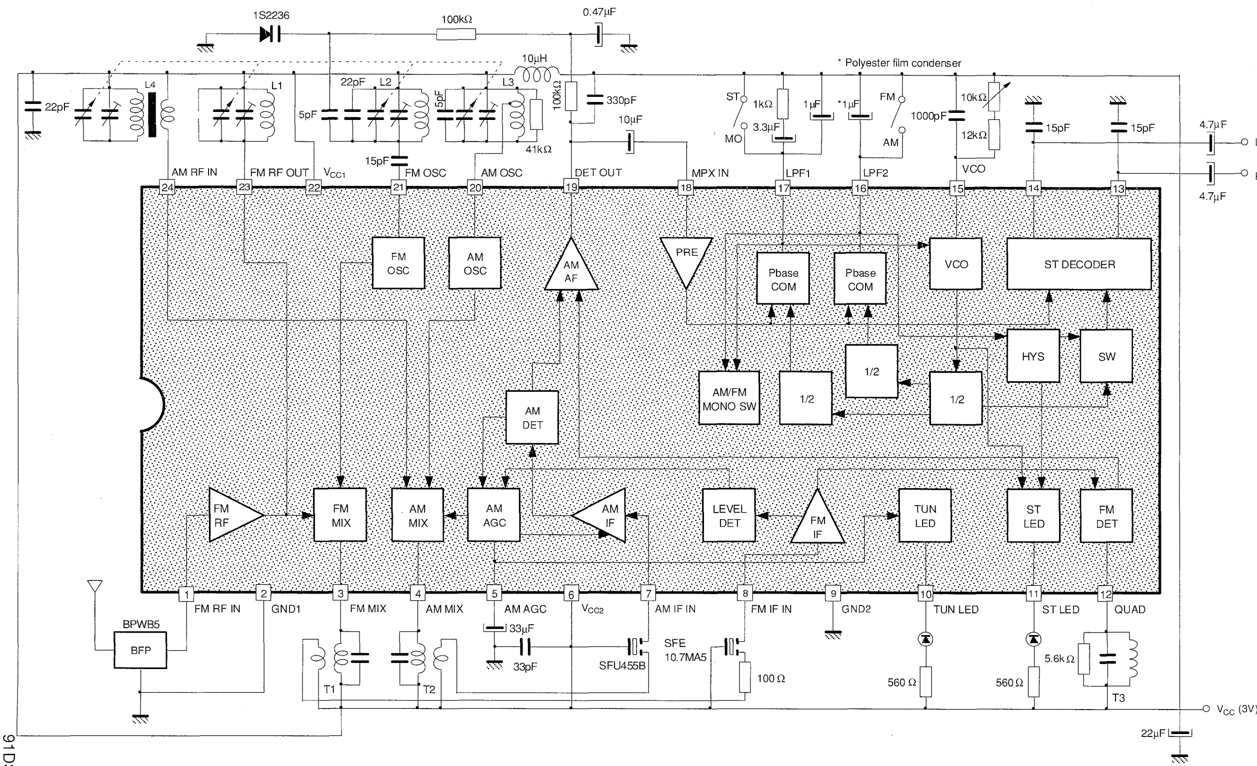
91DSTDA7222-02

ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $V_{CC} = 3V$ F/E : f = 83MHz, f_m = 1kHz
FM IF : f = 10.7MHz, Δf = ± 22.5kHz, f_m = 1kHz
AM : f = 1MHz, MOD = 30%, f_m = 1kHz
MPX : f_m = 1kHz
(unless otherwise specified)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_{CC} (FM)	Supply Current		V_{IN} = 0, FM mode		13.2	20	mA
I_{CC} (AM)			V_{IN} = 0, AM mode		8.4	13.5	mA
V_{IN} (lim)	F/E	Input Limiting Voltage	- 3dB limiting		10.0		dBμ
V_{OSC}		Local OSC Voltage	f_{OSC} = 72.3MHz		105		mV_{RMS}
V_{IN} (lim) IF	FM IF	Input Limiting Voltage	- 3dB limiting	40	46	53	dBμ
VOD		Recovered Output Voltage	V_{IN} = 80dBμ		100	130	mV_{RMS}
S/N		Signal to Noise Ratio	V_{IN} = 80dBμ		70		dB
THD		Total Harmonic Distortion	V_{IN} = 80dBμ		0.4		%
AMR		AM Rejection Ratio	V_{IN} = 80dBμ		40		dB
V_L		Lamp ON Sensitivity	I_L = 1mA		51		dBμ
G_V	AM	Gain	V_{IN} = 26dBμ	40	70	110	mV_{RMS}
VOD		Recovered Output Voltage	V_{IN} = 60dBμ	55	80	110	mV_{RMS}
S/N		Signal to Noise Ratio	V_{IN} = 60dBμ		42		dB
THD		Total Harmonic Distortion	V_{IN} = 60dBμ		1.0		%
V_L		Lamp ON Sensitivity	I_L = 1mA		25		dBμ
R19	Pin 19 Output Resistance		FM mode AM mode		0.75 12.5		kΩ kΩ
R_{IN}	MPX	Input Resistance			24		kΩ
R_{OUT}		Output Resistance			5		kΩ
$V_{IN\ (Max.)}$ Stereo		Max. Composite Signal Input Voltage	L + R = 90%, P = 10% f_m = 1kHz, THD = 3%		350		mV_{RMS}
Sep		Separation f_m = 100Hz f_m = 1kHz f_m = 10kHz	L + R = 135mV_{RMS} P = 15mV_{RMS}	20	42 35 42		dB dB dB
THD Monaural		Total Harmonic Distortion (monaural)	V_{IN} = 150mV_{RMS}		0.2		%
THD Stereo		Total Harmonic Distortion (stereo)	L + R = 135mV_{RMS} P = 15mV_{RMS}		0.2		%
G_V (MPX)		Voltage Gain	V_{IN} = 150mV_{RMS}	- 6	- 4	- 1	dB
C.B.		Channel Balance	V_{IN} = 150mV_{RMS}	- 2	0	2	dB
V_L (ON)		Stereo Lamp (ON) Sensitivity	Pilot Input		8	16	mV_{RMS}
V_L (OFF)		Stereo Lamp (OFF) Sensitivity		2	6		mV_{RMS}
V_H		Stereo Lamp Hysteresis			2		mV_{RMS}
C.R.		Capture Range	P = 15mV_{RMS}		± 3		%
S/N		Signal to Noise Ratio			70		dB

APPLICATION CIRCUIT

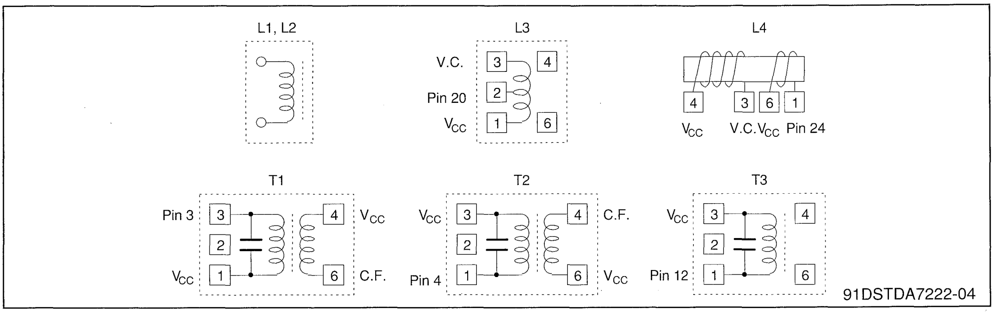


91DSTDA7222-03

COIL DATA

Coil N°		f (Hz)	L (µH)	Co (pF)	Qo	Turns				Wire	Ref. *
						1 - 2	2 - 3	1 - 3	4 - 6		
L_1	FM RF	100M	0.06		100			$2\frac{1}{4}$		0.5∅ UEW	S - 0258-00-021
L_2	FM OSC	100M	0.045		100			$1\frac{3}{4}$		0.5∅ UEW	S - 0258-000-021
L_3	MW OSC	796k	268		125	14	86			0.06∅ UEW	S - 2157-2239-213A
L_4	MW ANT	796k	600		200					0.07∅ x 3 USTC	S - CORE 10∅ x 80mm
T_1	FM MIX	10.7M		75	100			13	2	0.1∅ UEW	S - 2153-414-041
T_2	AM MIX	455k		330	115			132	9	0.06∅ UEW	S - 2150-2162-057
T_3	FM DET	10.7M		47	165			16		0.1∅ MUEW	S - 2153-4095-122

* S : Sumida Electric CO, LTD.



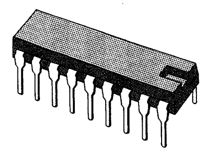
SGS-THOMSON
MICROELECTRONICS

TDA7227

SINGLE-CHIP AM/FM RADIO WITH FRONT-END

ADVANCE DATA

- BUILT-IN FM F/E AND AM/FM IF
- AM DETECTOR COIL AND IF COUPLING CAPACITOR ARE NOT NECESSARY
- WIDE OPERATING VOLTAGE RANGE (1.8 - 7V)
- LED DRIVE CIRCUIT FOR TUNING INDICATOR



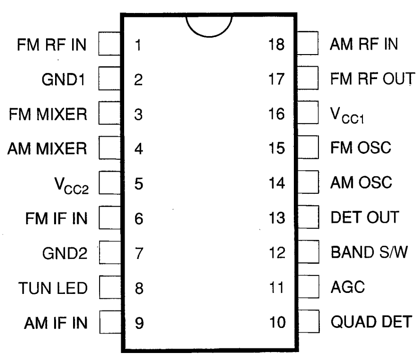
DIP18
(Plastic Package)

ORDER CODE : TDA7227

DESCRIPTION

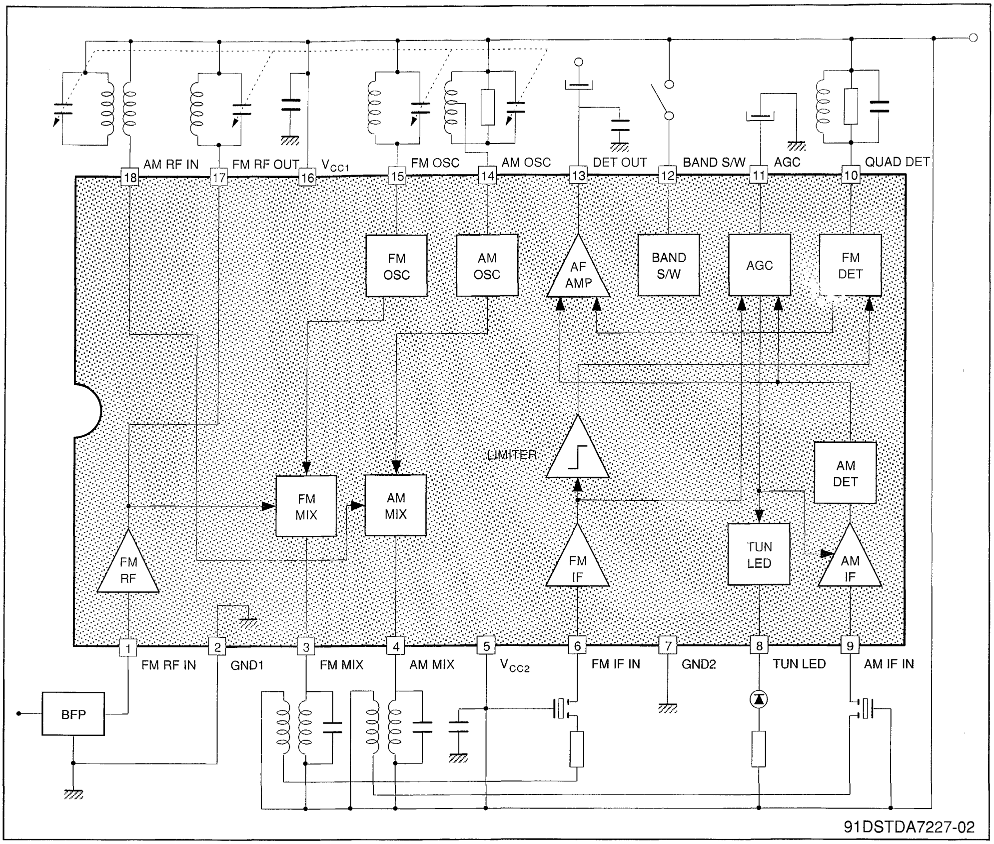
TDA7227 is a mono AM/FM one chip tuner ICs which is designed for portable radios, clock radios and radio cassette recorders.

PIN CONNECTIONS



91DSTDA7227-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	9	V
I_{LED}	LED Current	10	mA
V_{LED}	Led Voltage	10	V
T_{oper}	Operating Temperature	- 25 to 75	°C
T_{stg}	Storage Temperature	-55 to 150	°C

RECOMMENDED OPERATING CONDITION AT T_A = 25°C

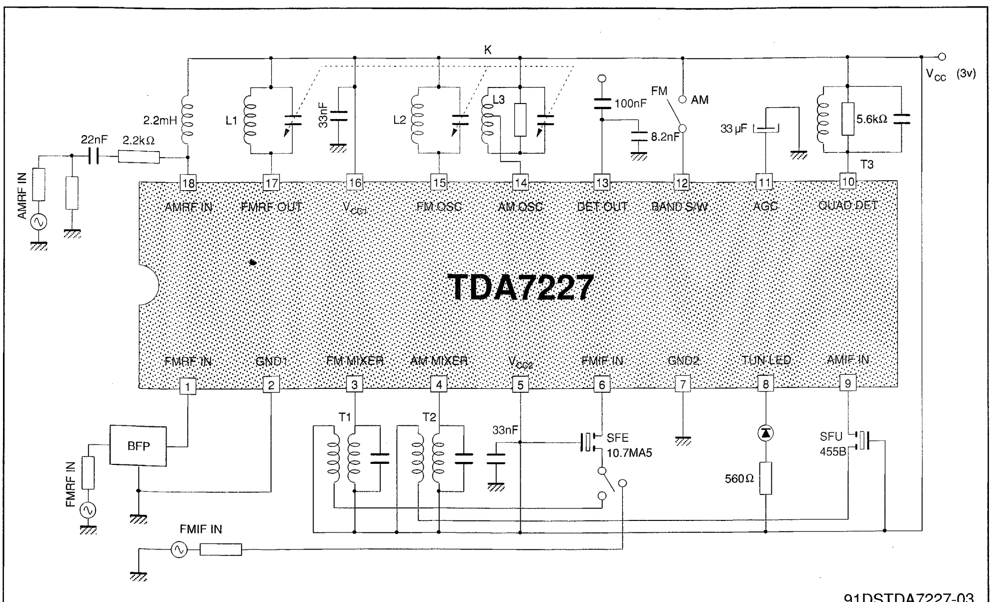
Symbol	Parameter	Value	Unit
V_S	Supply Voltage	1.8 to 7	V
T_{oper}	Operating Temperature	- 20 to 60	°C

ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $V_{CC} = 3V$ F/E : f = 100MHz, f_m = 1kHz
FM IF : f = 10.7MHz, f = + 22.5kHz, f_m = 1kHz
AM : f = 1MHz, m = 30%, f_m = 1kHz

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		1.8	3	7	V
I_{CC}	Supply Current	V_{IN} = 0, FM mode V_{IN} = 0, AM mode		9 7		mA mA
V_{IN} (lim)	FM F/E Input Limiting Voltage	- 3dB limiting		10		dBμ
FM SECTION						
V_{IN} (lim)	Input Limiting Voltage	- 3dB limiting		44		dBμ
V_O	Recovered Output Voltage	V_{IN} = 80dBμ		80		mV
S/N	Signal to Noise Ratio	V_{IN} = 80dBμ		70		dB
THD	Total Harmonic Distorsion	V_{IN} = 80dBμ		0.4		%
AMR	AM Rejection Ratio	V_{IN} = 80dBμ		50		dB
AM SECTION						
G_V	Gain	V_{IN} = 26dBμ		40		mV
V_O	Recovered Output Voltage	V_{IN} = 60dBμ		60		mV
S/N	Signal to Noise Ratio	V_{IN} = 60dBμ		44		dB
THD	Total Harmonic Distorsion	V_{IN} = 60dBμ		1.0		%
R_O	Pin 12 Output Resistance	FM mode AM mode		5 5		kΩ kΩ

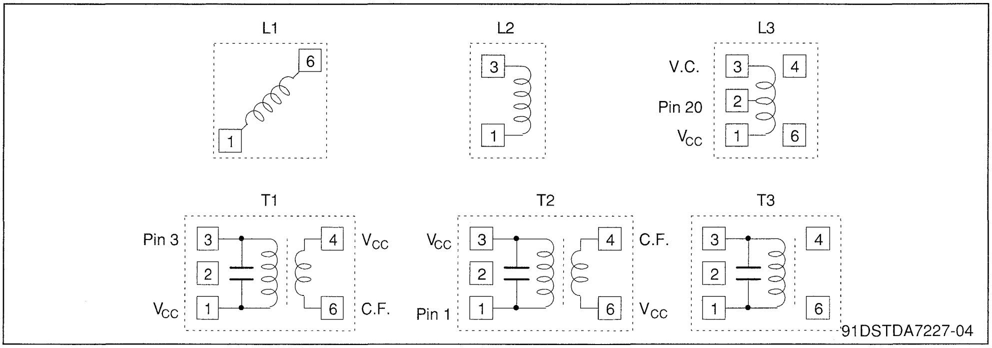
TEST CIRCUIT



COIL DATA

Coil N°	f (Hz)	L (µH)	C_O (pF)	Q_O	Turns 1 - 2	Turns 2 - 3	Turns 1 - 3	Turns 1 - 4	Turns 1 - 6	Wire (mm∅)	Ref. *
L1 FM RF	100M			100				$2\frac{1}{2}$		0.5 UEW	
L2 FM OSC	100M			100			$2\frac{3}{4}$			0.5 UEW	
L3 AM OSC	796k	288		115	13	73				0.08 UEW	S - 4147 - 1356 - 045
T1 FM MIX	10.7M		75	115			12		1	0.12 UEW	S - 0133 - 309 - 045
T2 AM MIX	455k		180	120			180		15	0.08 UEW	S - 2150 - 2162 - 165
T3 FM DET	10.7M		47	165			16			0.09 UEW	S - 2153 - 4095 - 132

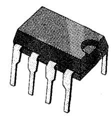
* S : Sumida Electronic CO, Ltd.



1.6W AUDIO AMPLIFIER

- OPERATING VOLTAGE 1.8 TO 15V
- LOW QUIESCENT CURRENT
- HIGH POWER CAPABILITY
- LOW CROSSOVER DISTORTION
- SOFT CLIPPING

The TDA7231 is a monolithic integrated circuit in 4+4 lead minidip package. It is intended for use as class AB power amplifier with wide range of supply voltage in portable radios, cassette recorders and players, etc.



Powerdip (4 + 4)

ORDERING NUMBER: TDA7231

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
P_{tot}	Total power dissipation at $T_{amb} = 50°C$	1.25	W
	at $T_{case} = 70°C$	4	W
I_o	Output peak current	1	A
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(Top view)

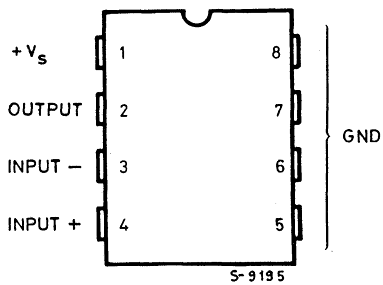
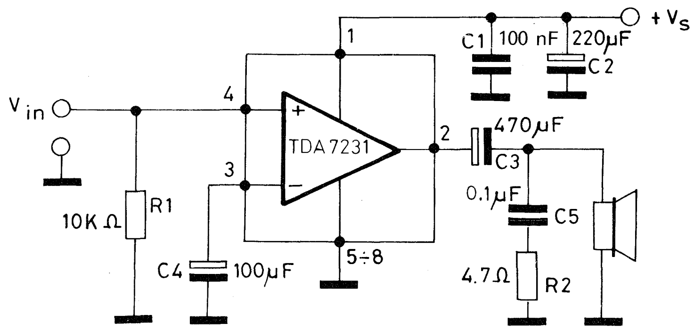
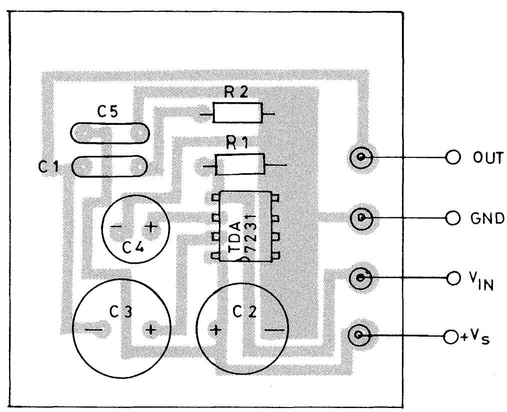


Fig. 1 - Test and application circuit



S-9196

Fig. 2 - P.C. board and components layout



CS-0235

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance juction ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	15	°C/W

ELECTRICAL CHARACTERISTICS ($V_s = 6V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			1.8		15	V
Vo	Quiescent out voltage	$V_S = 6V$			2.7		V
		$V_S = 3V$			1.2		V
I_d	Quiescent drain current				3.6	9	mA
I_b	Input bias current				100		nA
P_o	Output power	d = 10%	f = 1KHz				
		V_s = 12V	R_L = 8Ω		1.8		W
		V_s = 9V	R_L = 4Ω		1.6		W
		V_s = 6V	R_L = 8Ω		0.4		W
		V_s = 6V	R_L = 4Ω		0.7		W
		V_s = 3V	R_L = 4Ω		110		mW
		V_s = 3V	R_L = 8Ω		70		mW
d	Distortion	P_o = 0.2W f = 1KHz	R_L = 8Ω		0.3		%
G_v	Closed loop voltage gain				38		dB
R_{in}	Input resistance	f = 1KHz		100			KΩ
e_N	Total input noise	R_s = 10KΩ	B = Curve A		2		μV
			B = 22Hz to 22KHz		3		μV
SVR	Supply voltage rejection	f = 100Hz	Rg = 10KΩ	24	33		dB

Fig. 3 - Output power versus supply voltage

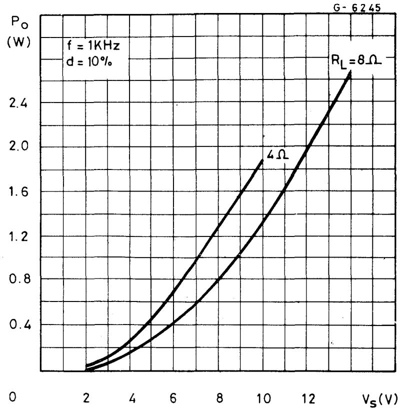


Fig. 4 - Quiescent current versus supply voltage

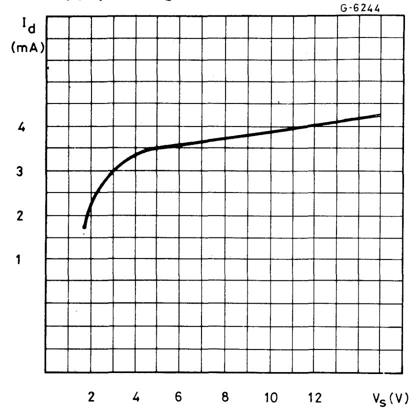


Fig. 5 - Quiescent output voltage versus supply voltage

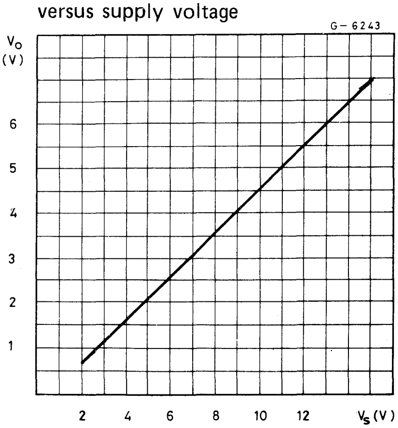
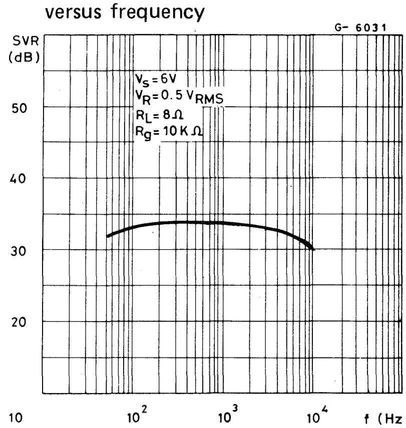


Fig. 6 - Supply voltage rejection versus frequency



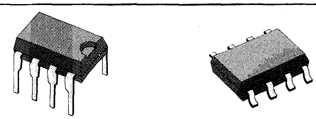
SGS-THOMSON
MICROELECTRONICS

TDA7233/D

1W AUDIO AMPLIFIER WITH MUTE

- OPERATING VOLTAGE 1.8 TO 15V
- EXTERNAL MUTE OR POWER DOWN FUNCTION
- IMPROVED SUPPLY VOLTAGE REJECTION
- LOW QUIESCENT CURRENT
- HIGH POWER CAPABILITY
- LOW CROSSOVER DISTORTION

The TDA7233 is a monolithic integrated circuit in 8 pin Minidip or SO-8 package, intended for use as class AB power amplifier with a wide range of supply voltage from 1.8V to 15V in portable radios, cassette recorders and players.



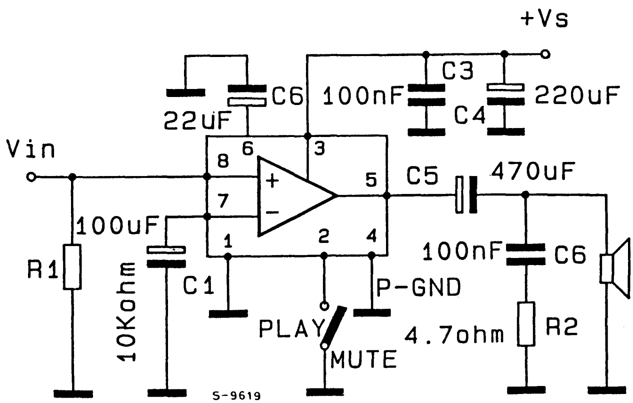
Minidip Plastic **SO-8J**

ORDERING NUMBER: TDA7233 (Minidip)
TDA7233D (SO-8)

ABSOLUTE MAXIMUM RATINGS

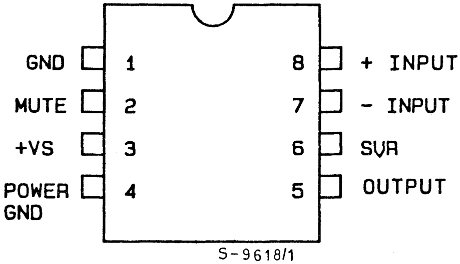
V_s	Supply voltage	16	V
I_o	Output peak current	1	A
P_{tot}	Total power dissipation at $T_{amb} = 50°C$	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

APPLICATION CIRCUIT

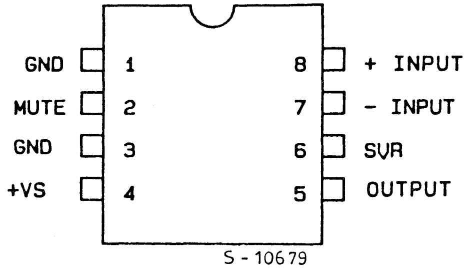


CONNECTION DIAGRAMS

(Top view)

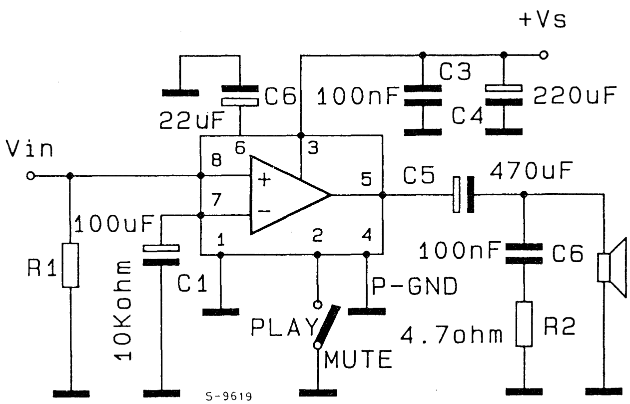


Minidip



SO-8

Fig. 1 - Test and application circuit



Note: Switch Open = Mute
Swith Closed = Play

THERMAL DATA			SO-8	Minidip
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200°C/W	100°C/W

ELECTRICAL CHARACTERISTICS (V_s = 6V, T_{amb} = 25°C, unless otherwise speficied)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		1.8		15	V
V_o	Quiescent out voltage			2.7		V
		V_s = 3V V_s = 9V		1.2 4.2		V V
I_d	Quiescent drain current	MUTE HIGH		3.6	9	mA
		MUTE LOW		0.4		
I_b	Input bias current			100		nA
P_o	Output power	d = 10% f = 1KHz V_s = 12V R_L = 8Ω V_s = 9V R_L = 4Ω V_s = 9V R_L = 8Ω V_s = 6V R_L = 8Ω V_s = 6V R_L = 4Ω V_s = 3V R_L = 4Ω V_s = 3V R_L = 8Ω		 1.9 1.6 0,8 0.4 0,45 110 70		 W W W W W mW mW
d	Distortion	P_o = 0.5W R_L = 8Ω f = 1KHz V_s = 9V		0.3		%
G_v	Closed loop voltage gain	f = 1KHz		39		dB
R_{IN}	Input resistance	f = 1KHz	100			KΩ
e_N	Total input noise (R_s = 10KΩ)	B = Curve A		2		μV
		B = 22Hz to 22KHz		3		
SVR	Supply voltage rejection	f = 100Hz, Rg = 10KΩ	40	45		dB
	MUTE attenuation	V_o = 1V f = 100Hz to 10KHz		70		dB
	MUTE threshold			0.6		V
I_M	MUTE current	V_s = 15V		0.4		mA

Fig. 2 - Output power vs. supply voltage

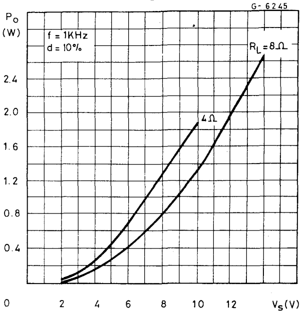


Fig. 3 - Supply voltage rejection vs. frequency

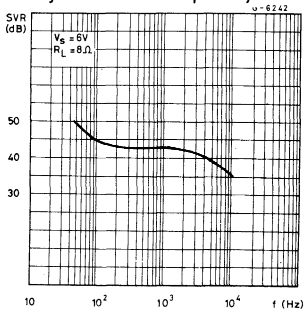


Fig. 4 - DC output voltage vs. supply voltage

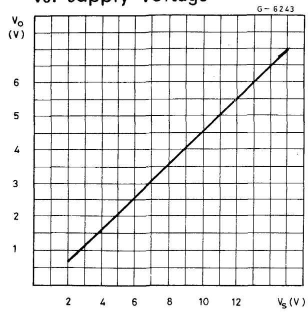


Fig. 5 - Quiescent current vs. supply voltage

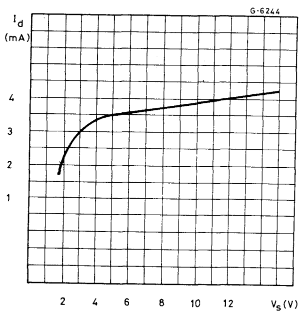
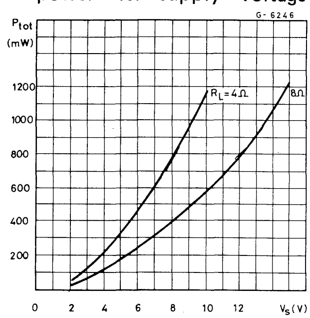


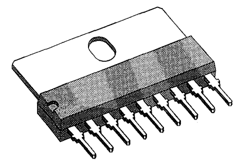
Fig. 6 - Total dissipated power vs. supply voltage



1W AUDIO AMPLIFIER WITH MUTE

ADVANCE DATA

- OPERATING VOLTAGE 1.8 TO 15V
- EXTERNAL MUTE OR POWER DOWN FUNCTION
- IMPROVED SUPPLY VOLTAGE REJECTION
- LOW QUIESCENT CURRENT
- HIGH POWER CAPABILITY
- LOW CROSSOVER DISTORTION



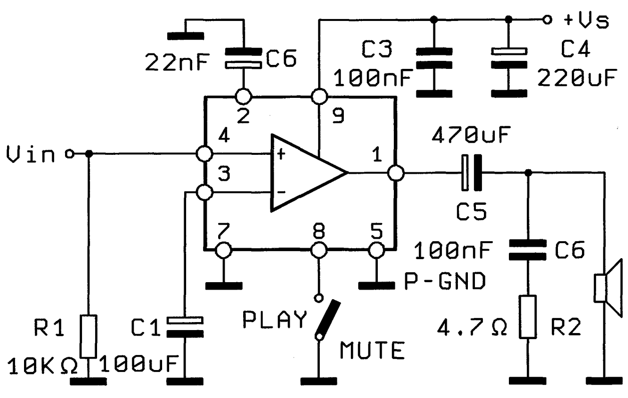
SIP9

ORDERING NUMBER: TDA7233S

DESCRIPTION

The TDA7233S is a monolithic integrated circuit in SIP 9, intended for use as class AB power amplifier with a wide range of supply voltage from 1.8V to 15V in portable radios, cassette recorders and players.

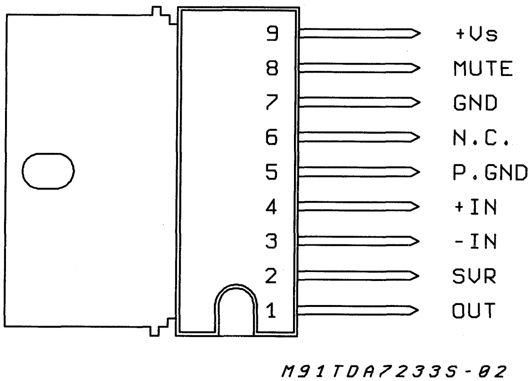
TEST AND APPLICATION CIRCUIT



MUTE SWITCH	CONDITION
OPEN	MUTE
CLOSED	PLAY

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	16	V
I_O	Output Peak Current	1	A
P_{tot}	Total Power Dissipation T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-pins	Max	10	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 6V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		1.8		15	V
V_O	Quiescent Output Voltage			2.7		V
		V_S = 3V V_S = 9V		1.2 4.2		V V
I_d	Quiescent Drain Current	PLAY		3.6	9	mA
		MUTE		0.4		mA
I_b	Input Bias Current			100		nA
P_O	Output Power	d = 10% f = 1kHz V_S = 12V R_L = 8Ω V_S = 9V R_L = 4Ω V_S = 9V R_L = 8Ω V_S = 6V R_L = 8Ω V_S = 6V R_L = 4Ω V_S = 3V R_L = 4Ω V_S = 3V R_L = 8Ω	 0.8 0.45 	 1.9 1.6 1 0.4 0.7 110 70		 W W W W W mW mW
d	Distortion	P_O = 0.5W R_L = 8Ω f = 1KHz V_S = 9V		0.3		%
G_V	Closed Loop Voltage Gain	f = 1KHz		39		dB
R_{IN}	Input Resistance	f = 1KHz	100			KΩ
e_N	Total Input Noise (R_S = 10KΩ)	B = Curve A		2		µV
		B = 22Hz to 22KHz		3		µV
SVR	Supply Voltage Rejection	R_g = 10KΩ f = 100Hz	40	45		dB
	MUTE Attenuation	V_O = 1V, f = 100Hz to 10KHz		70		dB
	MUTE Threshold			0.6		V
I_M	MUTE Current	V_S = 15V		0.4	2	mA

Figure 1: Output Power vs. Supply Voltage

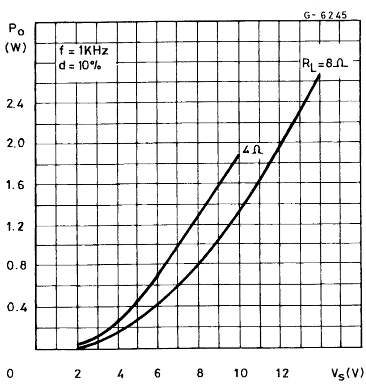


Figure 2: Supply Voltage Rejection vs. Frequency

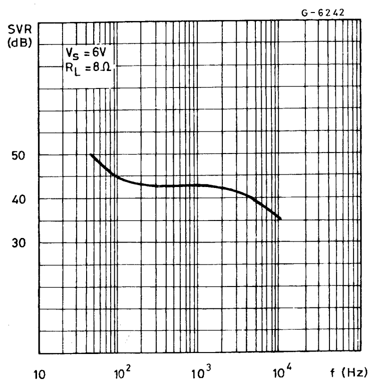


Figure 3: DC Output Voltage vs. Supply Voltage

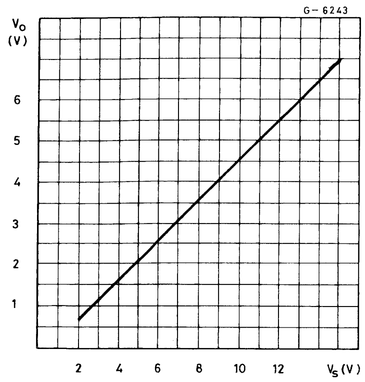


Figure 4: Quiescent Current vs. Supply Voltage

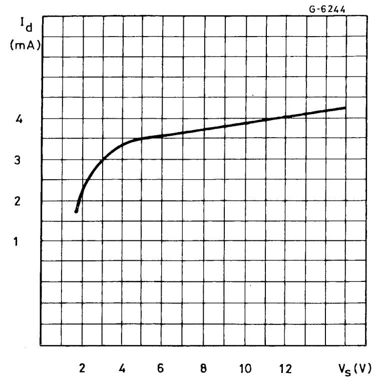
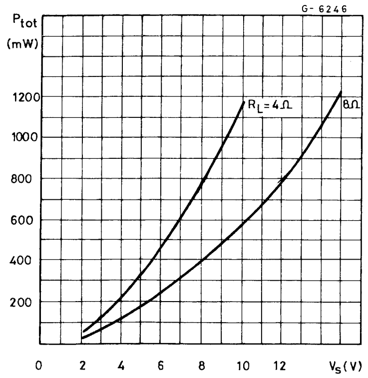


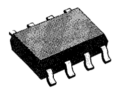
Figure 5: Total Dissipated Power vs. Supply Voltage



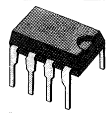
VERY LOW VOLTAGE AUDIO BRIDGE

ADVANCE DATA

The TDA7236 is a monolithic bridge audio amplifier in minidip and SO-8J package intended for use as audio power amplifier in telephone sets, mono radio receivers, etc.. Its main features are: minimum working supply voltage of 0.9V and low quiescient current.



SO-8J



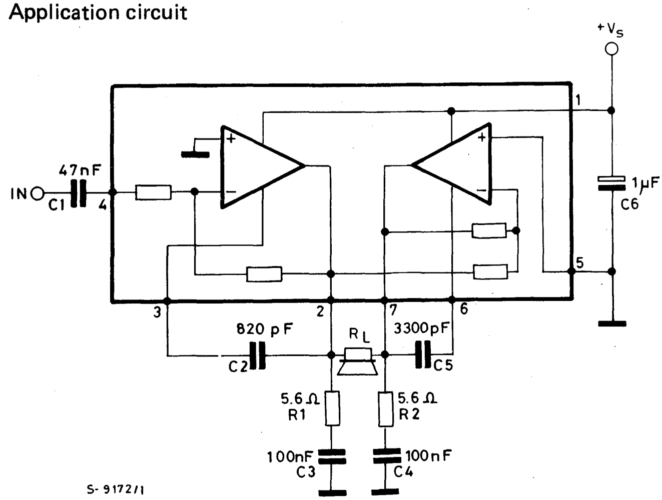
Minidip Plastic

ORDERING NUMBER: TDA7236 (Minidip)
TDA7236D (SO-8J)

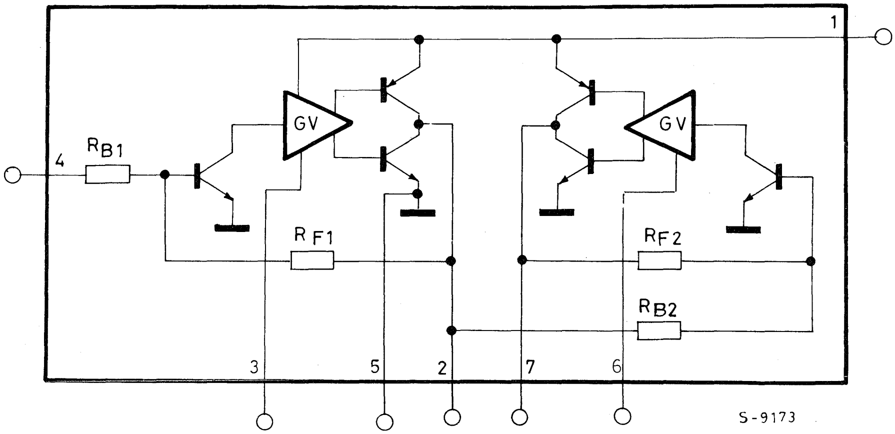
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	1.8	V
I_o	Output power current	50	mA
P_{tot}	Total power dissipation at $T_{amb} = 50°C$	0.5	W
T_{stg}, T_j	Storage and junction temperature	-40 to +150	°C

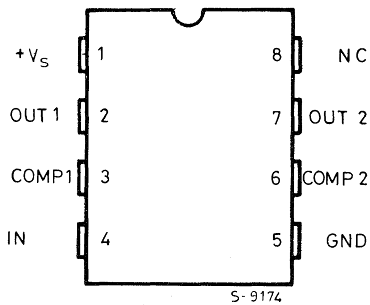
Fig. 1 - Test and Application circuit



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit $V_s = 1.25V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range		0.9		1.6	V
V_o	Quiescent output voltage			0.62		V
I_d	Total quiescent drain current			1	3	mA
G_v	Voltage gain			31		dB
R_i	Input resistance			10		KΩ
P_o	Output power	R_L = 32Ω; f = 1KHz; d = 10%	13	17		mW
d	Distortion	R_L = 32Ω; f = 1KHz; P_o = 5mW		1		%
B	Bandwidth		200Hz to 10KHz			
e_N	Total input noise voltage (curve A)			2		μV
V_{os}	Output DC offset voltage			30		mV

Fig. 2 - Output power vs. supply voltage

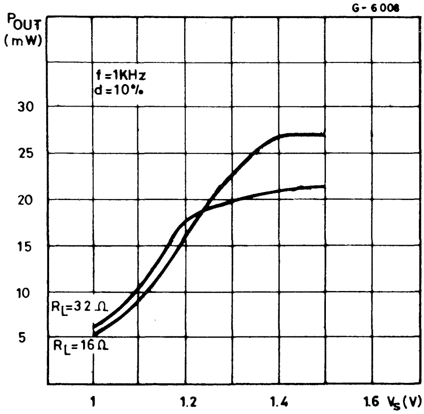


Fig. 3 - Drain current vs. supply voltage referred to Fig. 2

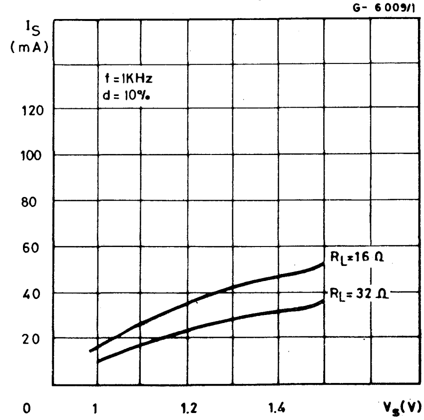
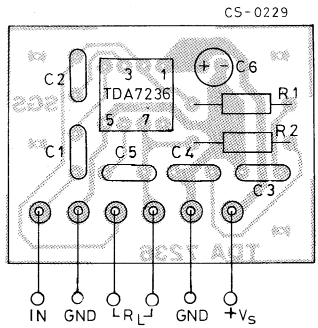
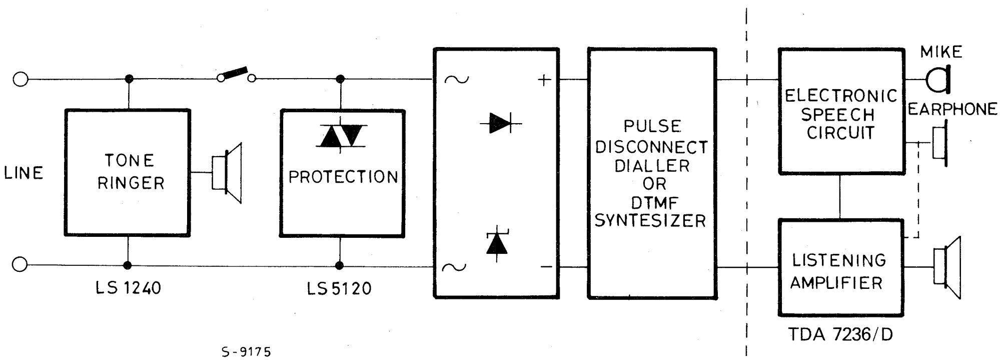


Fig. 4 - P.C. board and components layout of the circuit of Fig. 1 (1 : 1 scale)



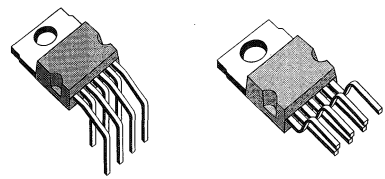
TYPICAL APPLICATION CIRCUIT

Fig. 5 - Telephone listening amplifier



20W BRIDGE AMPLIFIER FOR CAR RADIO

- COMPACT HEPTAWATT PACKAGE
- FEW EXTERNAL COMPONENTS
- OUTPUT PROTECTED AGAINST SHORT CIRCUITS TO GROUND AND ACROSS LOAD
- DUMP TRANSIENT
- THERMAL SHUTDOWN
- LOUDSPEAKER PROTECTION
- HIGH CURRENT CAPABILITY
- LOW DISTORTION/LOW NOISE



Heptawatt H **Heptawatt V**

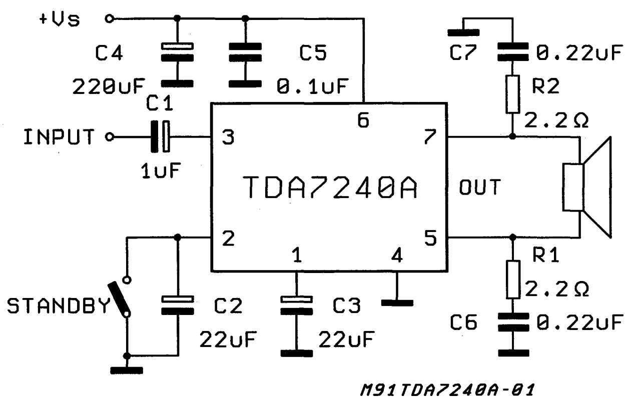
ORDERING NUMBERS : TDA7240AH
TDA7240AV

DESCRIPTION

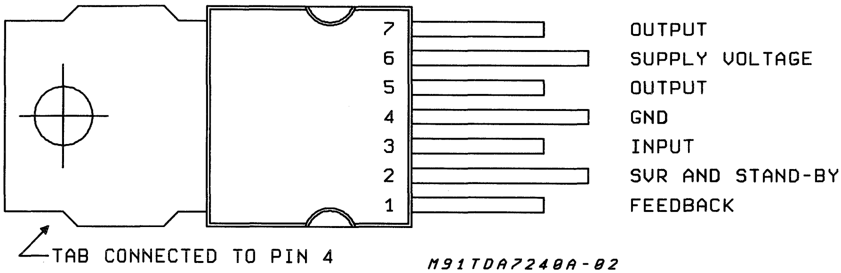
The TDA7240A is a 20W bridge audio amplifier IC designed specially for car radio applications. Thanks to the low external part count and compact Heptawatt 7-pin power package the TDA7240A occupies little space on the printed circuit board.

Reliable operation is guaranteed by a comprehensive array of on-chip protection features. These include protection against AC and DC output short circuits (to ground and across the load), load dump transients, and junction overtemperature. Additionally, the TDA7240A protects the loudspeaker when one output is short-circuited to ground.

Figure 1: Test and Application Circuit



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Operating Supply Voltage	18	V
V_s	DC Supply Voltage	28	V
V_s	Peak Supply Voltage (for 50ms)	40	V
I_o (*)	Peak Output Current (non repetitive t = 0.1ms)	4.5	A
I_o (*)	Peak Output Current (repetitive f ≥ 10Hz)	3.5	A
P_{tot}	Power Dissipation at T_{case} = 85°C	16	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

(*) Internally limited

THERMAL DATA

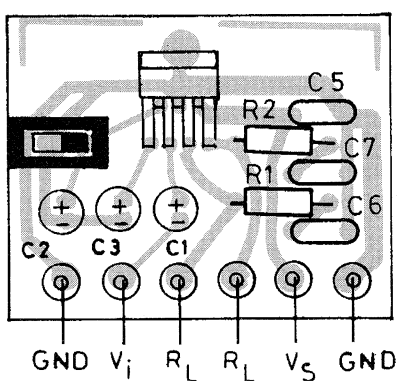
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W

ELECTRICAL CHARACTERISTICS (refer to the circuit of fig. 1, T_{amb} = 25 °C, R_{th} (heatsink) = 4 °C/W, V_s = 14.4 V)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage					18	V
V_{os}	Output Offset Voltage					150	mV
I_d	Total Quiescent Current	R_L = 4Ω			65	120	mA
P_o	Output Power	f = 1KHz d = 10%	R_L = 4Ω	18	20		W
			R_L = 8Ω	10	12		W
d	Distortion	R_L = 4Ω P_o = 50mW to 12W	f = 1KHz		0.1	0.5	%
		R_L = 8Ω P_o = 50 mW to 6W	f = 1KHz		0.05	0.5	%
G_v	Voltage Gain	f = 1KHz		39.5	40	40.5	dB
SVR	Supply Voltage Rejection	f = 100Hz	R_g = 10KΩ	35	40		dB
E_N	Total Input Noise	(*)	R_s = 10KΩ		2		µV
		(**)	R_s = 10KΩ		3	10	µV
η	Efficiency	R_L = 4Ω P_o = 20W	f = 1KHz		65		%
I_{sb}	Stand-by Current				200		µA
R_i	Input Resistance	f = 1KHz		70			KΩ
V_i	Input Sensitivity	f = 1KHz P_o = 2W	R_L = 4Ω		28		mV
f_L	Low Frequency Roll Off (– 3dB)	P_o = 15W	R_L = 4Ω			30	Hz
f_H	High Frequency Roll Off (– 3dB)	P_o = 15W	R_L = 4Ω	25			KHz
A_s	Stand-by Attenuation	V_o = 2V_{rms}		70	90		dB
$V_{TH\ (pin\ 2)}$	Stand-by Threshold					1	V

(*) B= Curve A (**) B = 22Hz to 22 KHz

Figure 2 : P.C. Board and Components layout of the Circuit of Fig. 1.(1:1scale)



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of Fig. 1. Different values can be used, the following table can help the designer.

Component	Recommanded Value	Purpose	Larger Than	Smaller Than
R1, R2	2.2Ω	Frequency Stability	Danger of High Frequency Oscillation	
C1	1µF	Input DC Decoupling	Higher Turn On and Stand-by Delay	Higher Turn On Pop. Higher Low Frequency Cutoff
C2	22µF	Ripple Rejection	Increase of SVR Increase of the Turn On Delay	Degradation of SVR
C3	22µF	Feedback Low Frequency Cutoff		Higher Low Frequency Cutoff
C6, C7	0.22µF	Frequency Stability		Danger of Oscillation
C4	220µF	Supply Filter		Danger of Oscillation
C5	0.1µF	Supply Bypass		Danger of Oscillation

Figure 3 : Output Power vs. Supply Voltage.

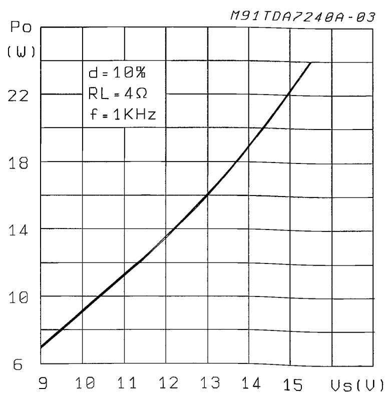


Figure 4 : Distortion vs. Output Power.

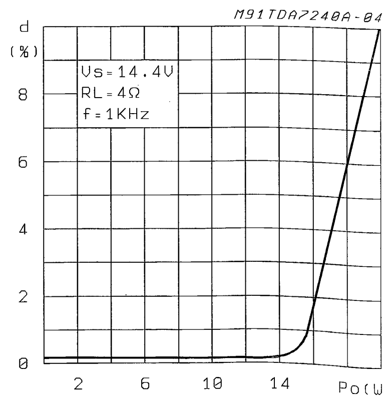


Figure 5 : Output Power vs. Supply voltage.

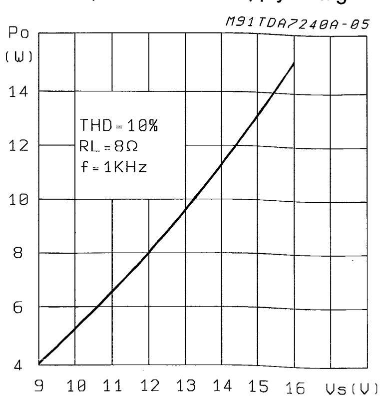


Figure 6 : Distortion vs. Output Power.

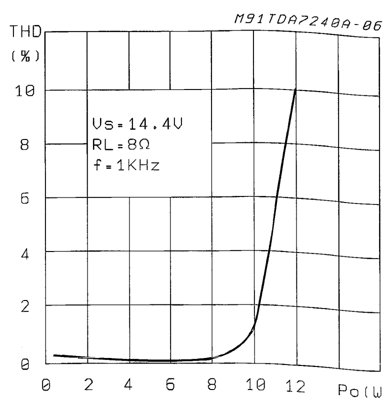


Figure 7 : Distortion vs. Frequency.

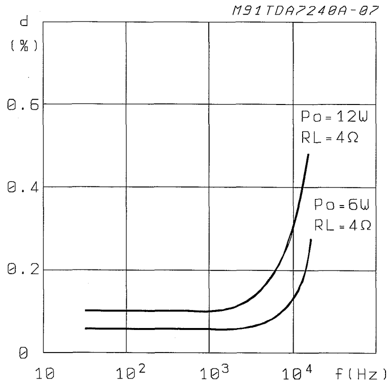


Figure 8 : Supply Voltage Rejection vs. Frequency.

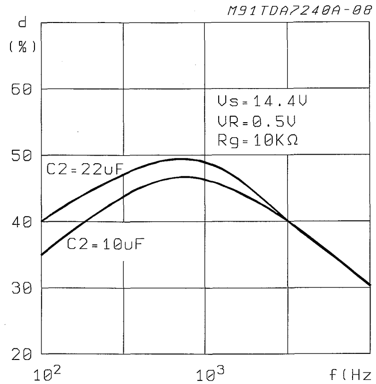


Figure 9 : Power Dissipation and Efficiency vs. Output Power.

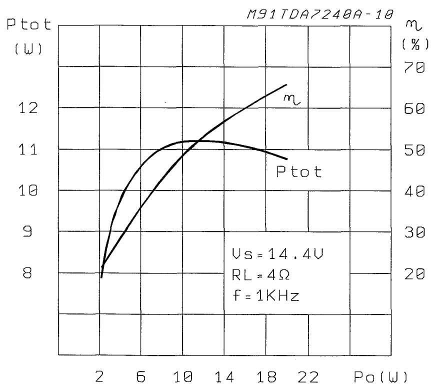
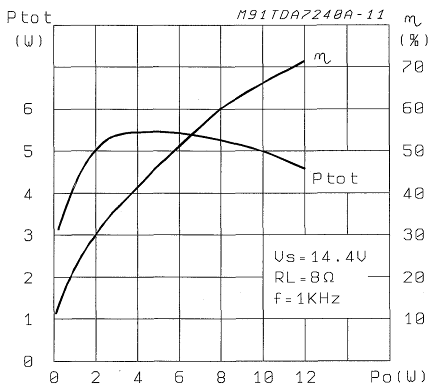


Figure 10 : Power Dissipation and Efficiency vs. Output Power.



SGS-THOMSON MICROELECTRONICS

TDA7241

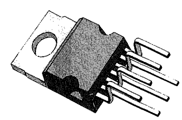
20W BRIDGE AMPLIFIER FOR CAR RADIO

- VERY LOW STAND-BY CURRENT
- GAIN = 26dB
- OUTPUT PROTECTED AGAINST SHORT CIRCUITS TO GROUND AND ACROSS LOAD
- COMPACT HEPTAWATT PACKAGE
- DUMP TRANSIENT
- THERMAL SHUTDOWN
- LOUDSPEAKER PROTECTION
- HIGH CURRENT CAPABILITY
- LOW DISTORTION / LOW NOISE

The TDA7241 is a 20W bridge audio amplifier IC designed specially for car radio applications. Thanks to the low external part count and compact Heptawatt 7-pin power package the TDA7241 occupies little space on the printed circuit board.

Reliable operation is guaranteed by a comprehensive array of on-chip protection features.

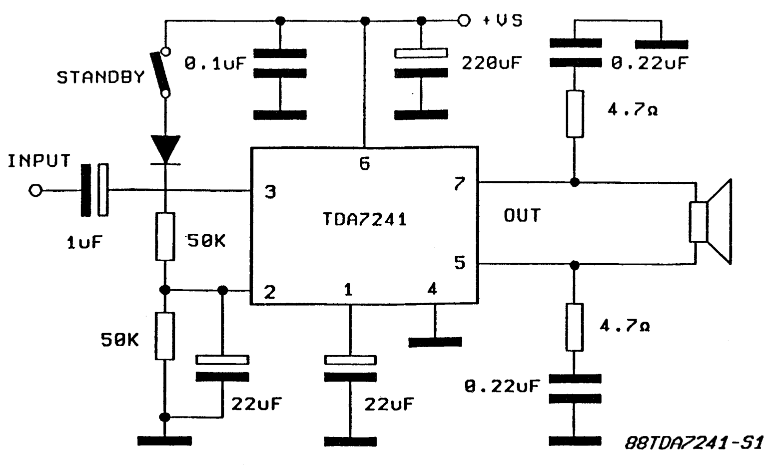
These include protection against AC and DC output short circuits (to ground and across the load), load dump transients, and junction overtemperature. Additionally, the TDA7241 protects the loudspeaker when one output is short-circuited to ground.



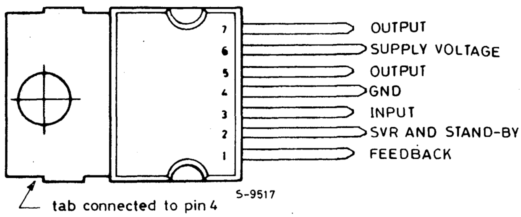
Heptawatt

ORDERING NUMBERS: TDA 7241V
TDA 7241H

TEST CIRCUIT



CONNECTION DIAGRAM
(Top view)



ABSOLUTE MAXIMUM RATINGS

V_s	Operating supply voltage	18	V
V_s	DC supply voltage	28	V
V_s	Peak supply voltage (for 50ms)	40	V
I_o (*)	Peak output current (non repetitive t = 0.1ms)	4.5	A
I_o (*)	Peak output current (repetitive f ≥ 10Hz)	3.5	A
P_{tot}	Power dissipation at T_{case} = 70°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

(*) Internally limited

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the circuit of Fig. 1, $T_{amb} = 25°C$, R_{th} (heatsink)= 4°C/W, V_s = 14.4V)

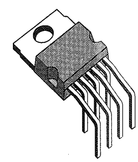
	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			9.5		18	V
V_{os}	Output offset voltage					150	mV
I_d	Total quiescent current	$R_L = 4\Omega$			65	120	mA
P_o	Output power	f = 1 KHz d = 10%	$R_L = 4\Omega$	18	20		W
			$R_L = 8\Omega$	10	12		W
d	Distortion	$R_L = 4\Omega$ P_o = 50 mW to 12W	f = 1 KHz		0.1	0.5	%
		$R_L = 8\Omega$ P_o = 50 mW to 6W	f = 1 KHz		0.05	0.5	%
G_v	Voltage gain	f = 1 KHz			26		dB
SVR	Supply voltage rejection	f = 100 Hz		45	52		dB
E_n	Total input noise	(*)	$R_s = 10\ K\Omega$		2	4	μV
		(**)	$R_s = 10\ K\Omega$		3		μV
η	Efficiency	$R_L = 4\Omega$ P_o = 20W	f = 1 KHz		65		%
I_{sb}	Stand-by current				1		μA
R_i.	Input resistance	f = 1 KHz		70			KΩ
V_i	Input sensitivity	f = 1 KHz P_o = 2W	$R_L = 4\Omega$		140		mV
f_L	Low frequency roll off (-3 dB)	P_o = 15W	$R_L = 4\Omega$			30	Hz
f_H	High frequency roll off (-3 dB)	P_o = 15W	$R_L = 4\Omega$	25			KHz
A_s	Stand-by attenuation	$V_o = 2\ V_{rms}$		70	90		dB
V_{TH}(pin. 2)	Stand-by threshold					1	V

(*) B = Curve A (**) B = 22 Hz to 22 KHz

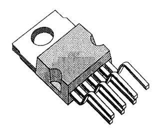
20W BRIDGE AMPLIFIER FOR CAR RADIO

ADVANCE DATA

- VERY LOW STAND-BY CURRENT
- GAIN = 32dB
- OUTPUT PROTECTED AGAINST SHORT CIRCUITS TO GROUND AND ACROSS LOAD
- COMPACT HEPTAWATT PACKAGE
- DUMP TRANSIENT
- THERMAL SHUTDOWN
- LOUDSPEAKER PROTECTION
- HIGH CURRENT CAPABILITY
- LOW DISTORTION / LOW NOISE



Heptawatt H



Heptawatt V

ORDERING NUMBERS:

TDA7241BH TDA7241BV

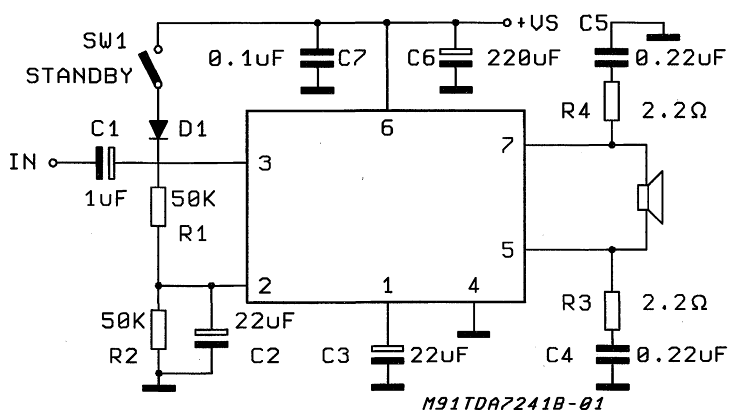
DESCRIPTION

The TDA7241B is a 20W bridge audio amplifier IC designed specially for car radio applications. Thanks to the low external part count and compact Heptawatt 7-pin power package the TDA7241B occupies little space on the printed circuit board.

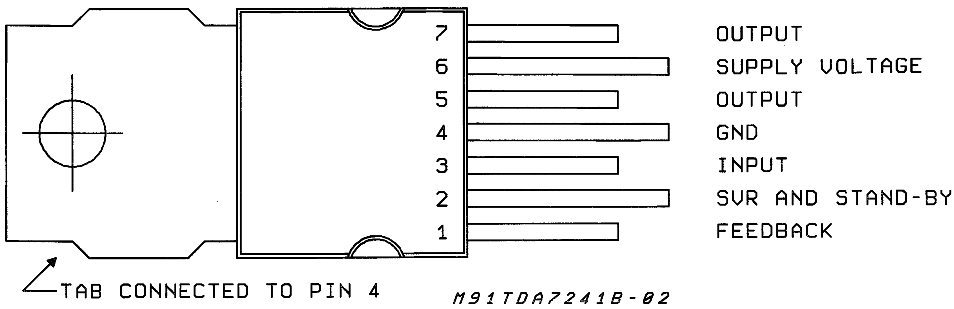
Reliable operation is guaranteed by a comprehensive array of on-chip protection features.

These include protection against AC and DC output short circuits (to ground and across the load), load dump transients, and junction overtemperature. Additionally, the TDA7241B protects the loudspeaker when one output is short-circuited to ground.

Figure 1: Test and Appliication Circuit



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	18	V
V_S	DC Supply Voltage	28	V
V_S	Peak Supply Voltage (t = 50ms)	40	V
I_O	Peak Output Current (non repetitive t = 0.1ms)	4.5	A
I_O	Peak Output Current (repetitive f ≥ 10Hz)	3.5	A
P_{tot}	Power Dissipation at T_{case} = 85°C	16	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the circuit of Fig. 1; V_S = 14.4V; R_{th} (heatsink) = 4°C/W, T_{amb} = 25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Range				18	V
I_d	Total Quiescent Current	R_L = 4Ω			80	mA
V_{OS}	Output Offset Voltage				100	mV
P_O	Output Power	f = 1KHz d = 10% R_L = 2Ω R_L = 4Ω R_L = 8Ω	18	26 20 12		W
d	Distortion	R_L = 4Ω f = 1KHz P_O = 50mW to 12W		0.1	0.5	%
		R_L = 8Ω f = 1KHz P_O = 50mW to 6W		0.05		%
G_V	Voltage Gain	f = 1KHz	31	32	33	dB
SVR	Supply Voltage Rejection	f =100Hz R_S = 10KΩ	40	50		dB
E_n	Total Input Noise	B = Curve A R_S = 10KΩ		2		µV
		B = 22Hz to 22KHz R_S = 10KΩ		3	10	mV
η	Efficiency	R_L = 4Ω f = 1KHz P_O = 20W		65		%
I_{sb}	Stand-by Current				100	µA
R_i	Input Resistance	f = 1KHz	70			KΩ
V_i	Input Sensitivity	f = 1KHz P_O = 2W R_L = 4Ω		70		mV
f_L	Low Frequency Roll Off (-3dB)	P_O = 15W R_L = 4Ω		30		Hz
f_H	High Frequency Roll Off (-3dB)	PO = 15W R_L = 4Ω	25			KHz
A_S	Stand-by Attenuation	V_O = 2Vrms	70	90		dB
V_{TH}(pin.2)	Stand-by Threshold				1	V
T_{sd}	Thermal Shutdown Junction Temp.			150		°C

(*) B = Curve (**) B = 22Hz to 22KHz

Figure 2: P.C. Board and Component Layout of the Circuit of Fig. 1 (1:1 scale).

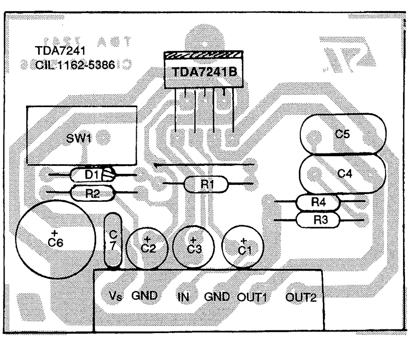


Figure 3: Output Power vs. Supply Voltage

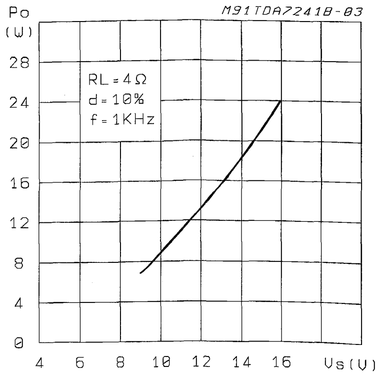


Figure 4: Output Power vs. Supply Voltage

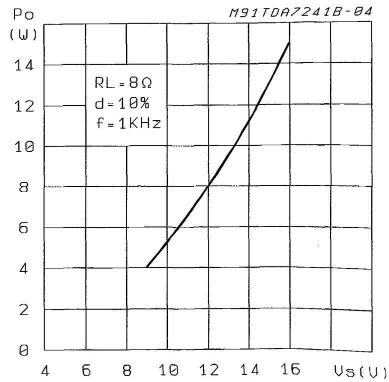


Figure 5: Distortion vs. Output Power

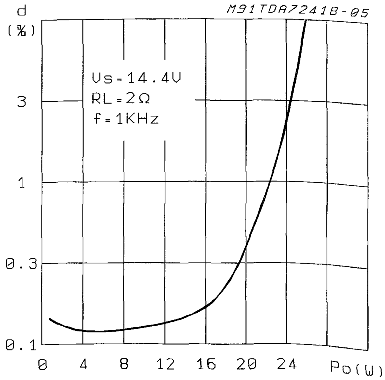


Figure 6: Distortion vs. Output Power

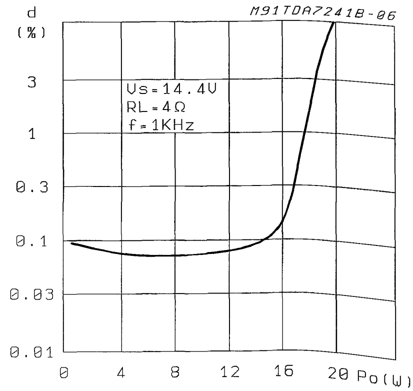


Figure 7: Distortion vs. Output Power

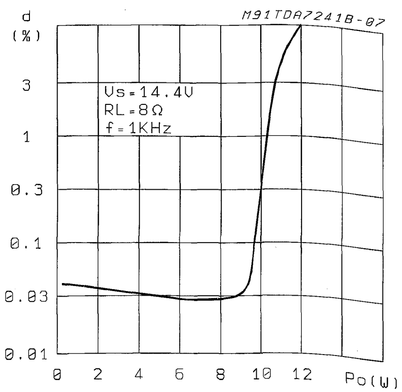


Figure 8: SVR vs. Frequency

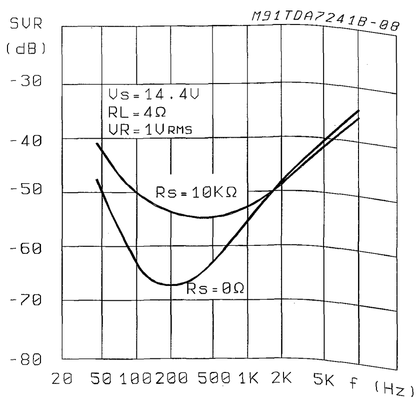


Figure 9: Power Dissipation and Efficiency vs. Output Power

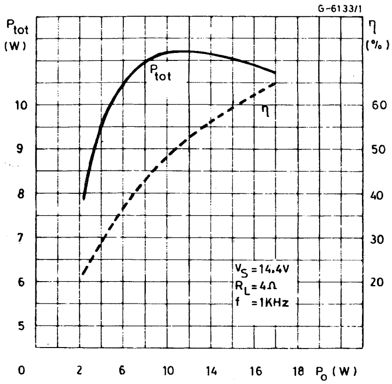
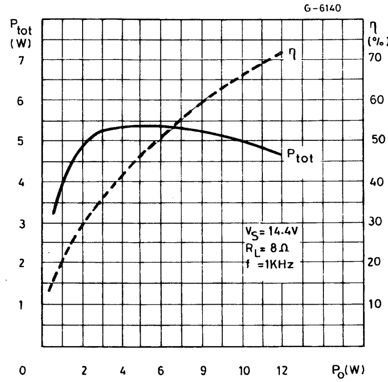


Figure 10: Power Dissipation and Efficiency vs. Output Power



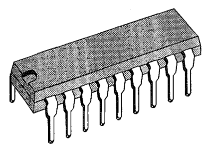
SGS-THOMSON MICROELECTRONICS

TDA7245

5W AUDIO AMPLIFIER WITH MUTING AND STAND-BY

ADVANCE DATA

- MUTING AND STAND-BY FUNCTIONS
- VOLTAGE RANGE UP TO 30V
- HIGH SUPPLY VOLTAGE REJECTION SVR TYP = 50dB (f = 100Hz)
- MUSIC POWER = 12W (R_L = 4Ω, d = 10%)
- PROTECTION AGAINST CHIP OVER TEMPERATURE



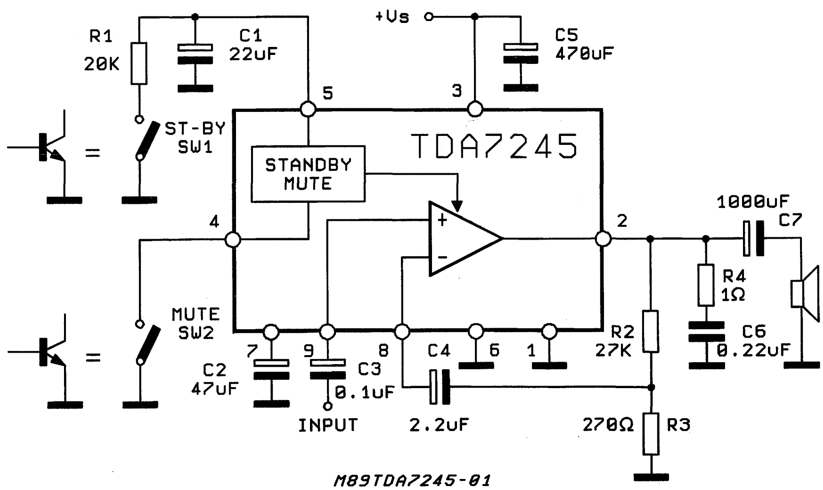
Powerdip 9+9

ORDERING NUMBER: TDA7245

DESCRIPTION

The TDA7245 is a monolithic integrated circuit in 9+9 POWERDIP package, intended for use as low frequency power amplifier in a wide range of applications in radio and TV sets.

Figure 1: Test and Application Circuit

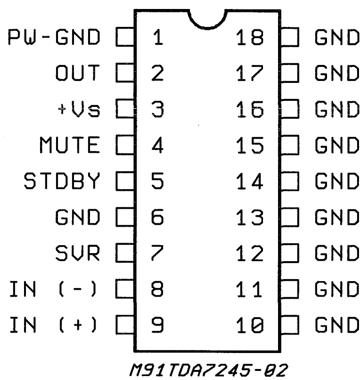


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	30	V
I_O	Output Peak Current (non repetitive t = 100μs)	3	A
I_O	Output Peak Current (repetitive, f > 20Hz)	2.5	A
P_{tot}	Power Dissipation at T_{amb} = 80°C at T_{case} = 70°C	1 6	W W
T_{stg}, T_j	Storage and junction Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance junction-case	Max	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance junction-ambient	Max	70	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb} = 25°C, f = 1kHz; unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		12		30	V
V_O	Quiescent Output Voltage	V_S = 24V		11.6		V
I_d	Quiescent Drain Current	V_S = 14V V_S = 28V		17 21	 35	mA mA
P_O	Output Power	d = 1%, f = 1KHz V_S = 14V, R_L = 4Ω V_S = 18V, R_L = 8Ω d = 10%, f = 1KHz V_S = 14V, R_L = 4Ω V_S = 18V, R_L = 8Ω Music Power (*) V_S = 24V, d = 10%, R_L = 4Ω	 4 	 4 4 5 5 12		 W W W W W
d	Harmonic Distortion	V_S = 14V, R_L = 4Ω, P_O = 50mW to 3W f = 1KHz f = 10KHz V_S = 18V, R_L = 8Ω, P_O = 50mW to 3.5W f = 1KHz f = 10KHz V_S = 22V, R_L = 16Ω, P_O = 50mW to 3W f = 1KHz f = 10KHz		 0.15 0.8 0.12 0.5 0.08 0.4	 0.5	 % % % % % %
R_I	Input Impedance	f = 1kHz	30			kΩ
BW	Small signal bandwidth (-3dB)	P_O = 1W; R_L = 4Ω V_S = 14V	50 to 40,000			Hz
G_V	Voltage Gain (open loop)	f = 1kHz		75		dB
G_V	Voltage Gain (closed loop)	f = 1kHz	39	40	41	dB
e_N	Total Input Noise	B = 22 - 22,000Hz R_s = 50Ω R_s = 1kΩ R_s = 10kΩ		 1.7 2 3	 6	 mV μV μV
S/N	Signal to Noise Ratio	V_S = 18V; R_L = 8Ω P_O = 5W; R_S = 10KΩ		86		dB
SVR	Supply Voltage Rejection	V_S = 16.5V; R_L = 8Ω; f = 100Hz R_s = 10kΩ; V_r = 0.5Vrms	40	50		dB
T_{sd}	Thermal shut-down Junction Temperature			150		°C

MUTE FUNCTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_m	Pin 4 DC Voltage	Mute SW Open (play)		6.4		V
ATT_m	Muting Attenuation	f = 100Hz to 10kHz	60	65		dB

ELECTRICAL CHARACTERISTCS (Continued)

STAND-BY FUNCTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{st\text{-}by}$	Pin 5 DC Voltage	Mute SW Open (play)		6.4		V
$I_{st\text{-}by}$	Pin 5 Current	Mute SW Closed (st-by)		160	280	µA
$ATT_{st\text{-}by}$	Stand-by Attenuation	f = 100Hz to 10kHz	70	90		dB
V_t	Stand-by Threshold (pin 5)			3.8		V
$I_{d\ st\text{-}by}$	Stand-by Current	V_S = 14V		1	3	mA

Note (*):

MUSIC POWER CONCEPT

MUSIC POWER is (according to the IEC clauses n.268-3 of Jan 83) the maximal power which the amplifier is capable of producing across the rated load resistance (regardless of non linearity) 1 sec after the application of a sinusoidal input signal of frequency 1KHz.

According to this definition our method of measurement comprises the following steps:
1) Set the voltage supply at the maximum operating value -20%
2) Apply a input signal in the form of a 1KHz tone burst of 1 sec duration; the repetition period of the signal pulses is > 60 sec
3) The output voltage is measured 1 sec from the start of the pulse
4) Increase the input voltage until the output signal show a THD = 10%
5) The music power is then $V^2_{out}/R1$, where V_{out} is the output voltage measured in the condition of point 4) and R1 is the rated load impedance

The target of this method is to avoid excessive dissipation in the amplifier.

Figure 2: Schematic Diagram

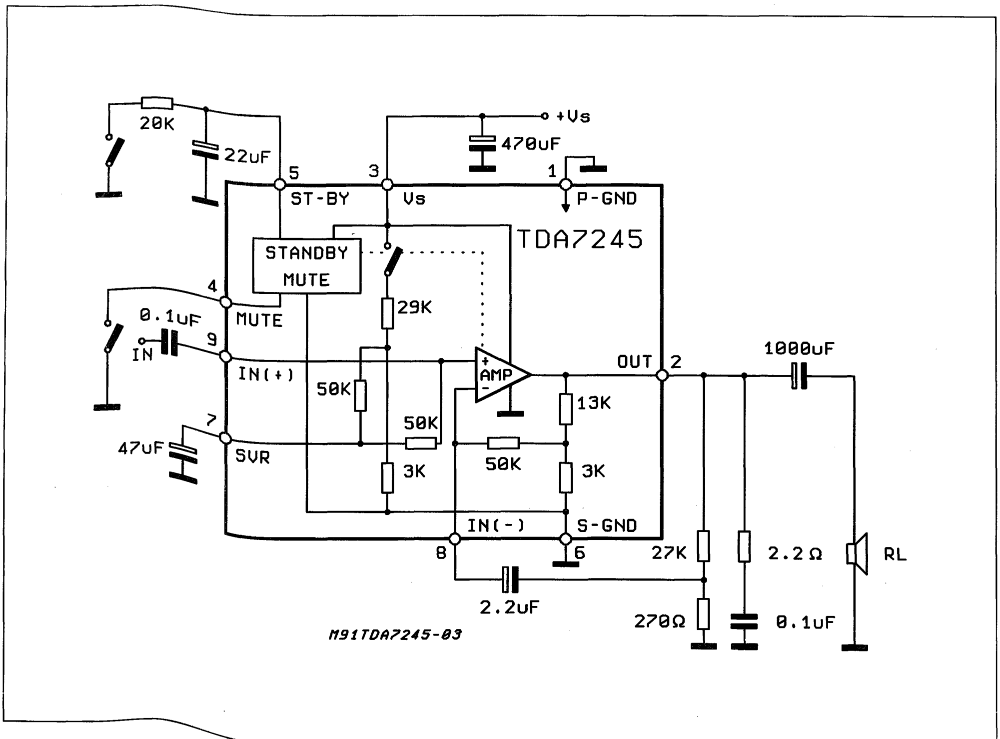
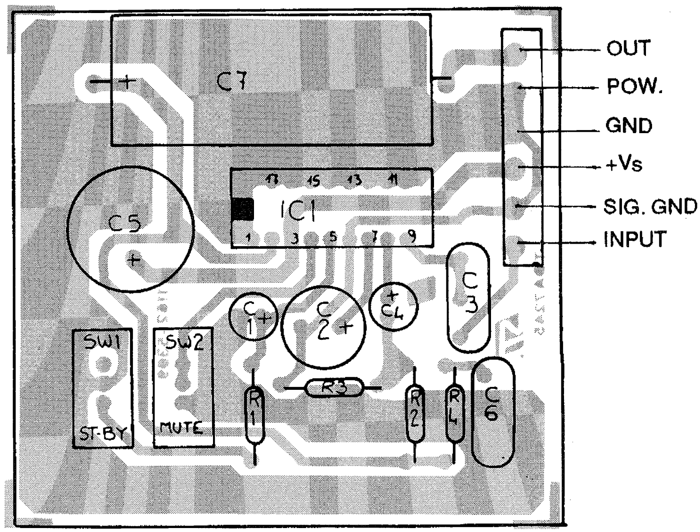


Figure 3: P.C. Board and Components Layout of the Circuit of fig 2 (1:1 scale)



APPLICATION SUGGESTIONS

The recommended values of the external components are those shown on the application circuit of fig.1. Different values can be used. The following table can help the dsigner.

Component	Rec. Value	Purpose	Larger than Rec. Value	Smaller than Rec. Value
R1	20KΩ	St-By Biasing	Incorrect St-By Function	Worse POP and Shorter Delay at St-By Insertion
R2(*)	27KΩ	Feedback Resistors	Increase of Gain	Decrease of Gain
R3(*)	270Ω		Decrease of Gain	Increase of Gain
R4	1Ω	Frequency Stability	Danger of Oscillations	
C1	22µF	St-By Capacitor	Longer ON/OFF Delay Time at St-By IN/OUT	Worse POP and Shorter Delay at St-By insertion
C2	47µF	SVR Capacitor	Worse Turn-On POP by V_S and St-By	Degradation of SVR
C3	0.1µF	Input Capacitance		Higher Low Frequency Cut-off
C4	2.2µF	Inverting Input DC Decoupling		Higher Low Frequency Cut-off
C5	470µF	Supply Voltage		Danger of Oscillations
C6	0.22µF	Frequency Stability	Danger of Oscillations	
C7	1000µF	Output DC Decoupling		Higher Low Frequency Cut-off

(*) The value of closed loop gain ($G_V = 1 + R2/R3$) must be higher than 25dB.

Figure 4: DC Output Voltage vs. Supply Voltage

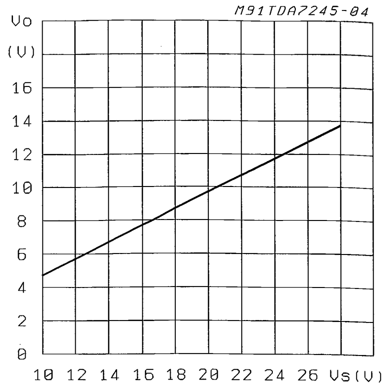


Figure 5: I_D vs. Supply Voltage

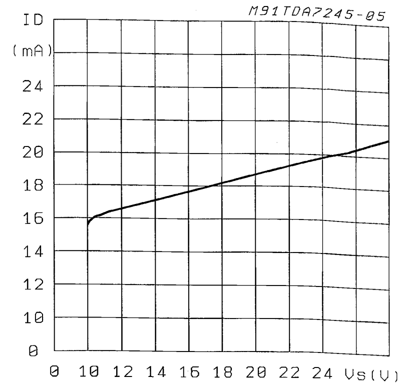


Figure 6: Output Power vs. Supply Voltage

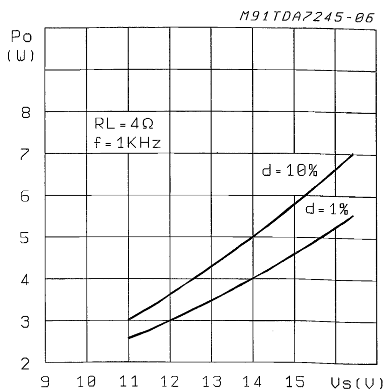


Figure 7: Output Power vs. Supply Voltage

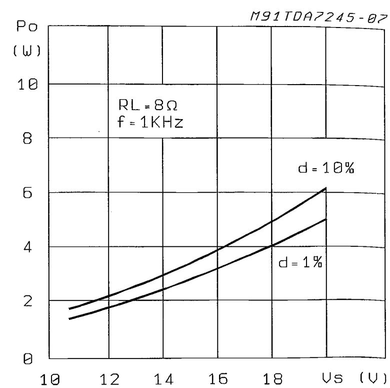


Figure 8: Output Power vs. Supply Voltage

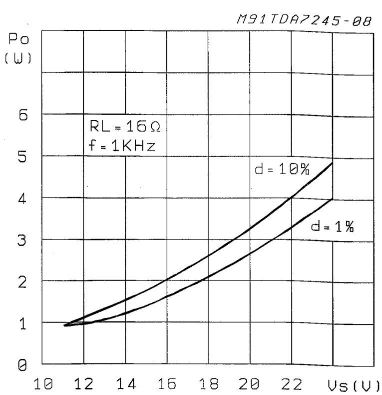


Figure 9: Distortion vs. Output Power

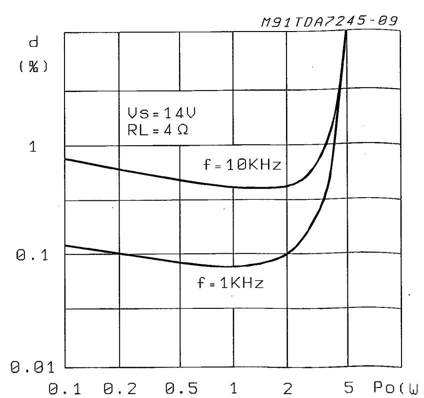


Figure 10: Distortion vs. Output Power

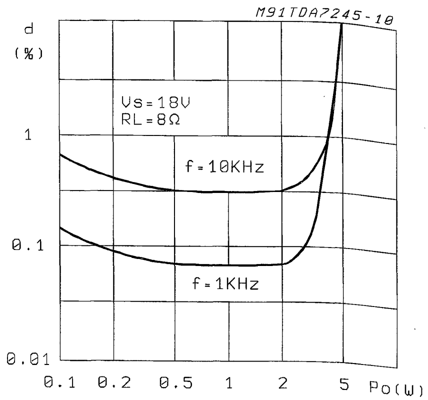


Figure 11: Distortion vs. Output Power

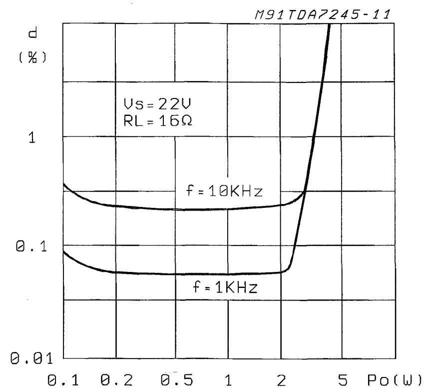


Figure 12: Supply Voltage Rejection vs. Frequency (play)

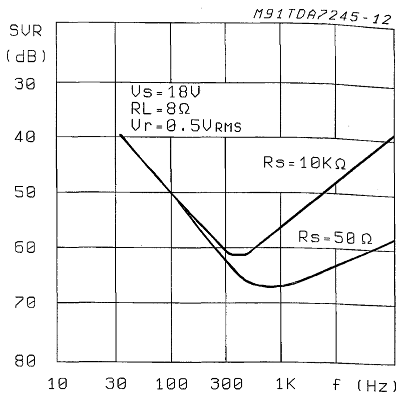


Figure 13: Power Dissipation & Efficiency vs. Output Power

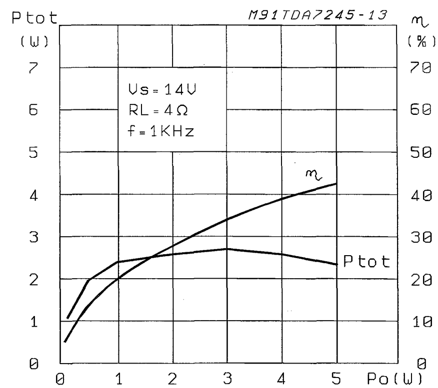


Figure 14: Power Dissipation & Efficiency vs. Output Power

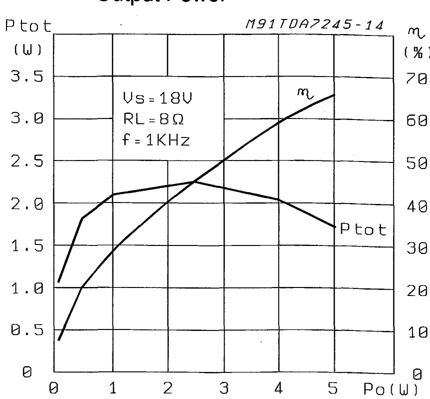


Figure 15: V_{pin5} ($=V_{pin4}$) vs. Supply Voltage

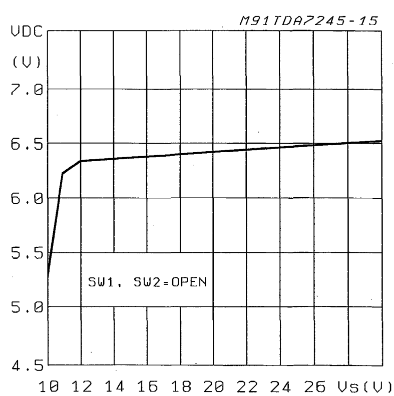


Figure 16: I_{pin4} (muting) vs. Supply Voltage

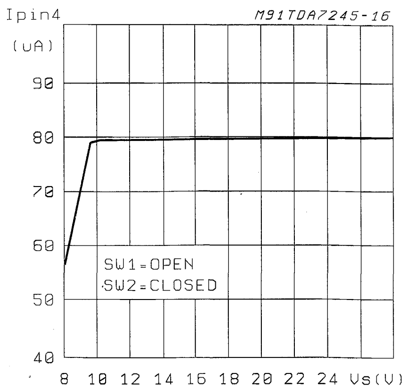


Figure 17: I_{pin5} (St-By) vs. Supply Voltage

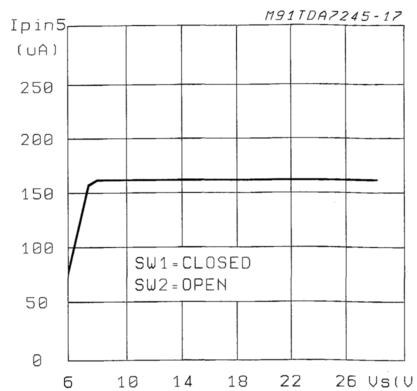


Figure 18: Quiescent Current (St-By) vs. Supply Voltage

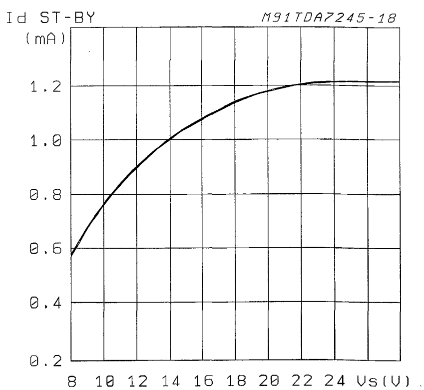


Figure 19: Output Attenuation vs. V_{pin5}

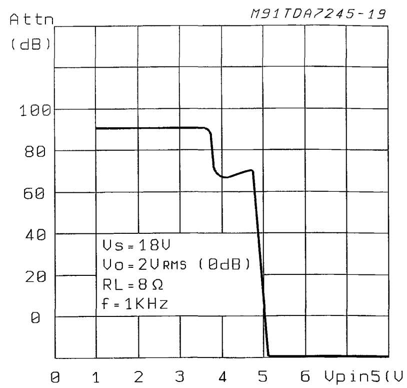
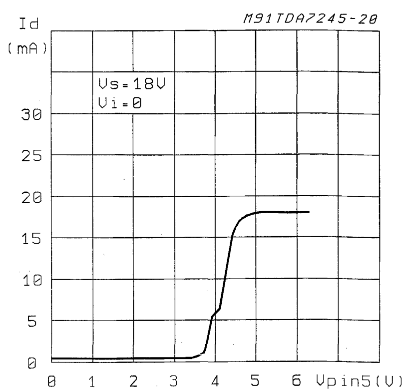


Figure 20: Quiescent Current vs. V_{pin5}



MUTING / STAND- BY

The muting function allows to inhibit the output signal through an external control signal.

It can be used in many cases, when a temporary inhibition of the output signal is requested, for example:

- in switch-on condition, to avoid preamplifier power-on transients
- during switching at the input stages
- during the receiver tuning.

The stand-by function is very useful and permits a complete turn ON/OFF of the device through a low power signal, which can be provided by a µP.

THERMAL SHUTDOWN

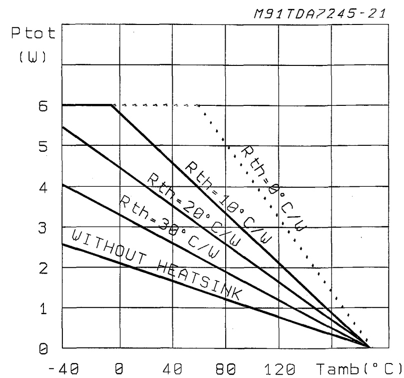
The presence of a thermal limiting circuit offers the following advantages:

1)An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily tolerated since the Tj cannot be higher than 150°C.

2)The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
If for any reason, the junction temperature increase up to 150°C, the thermal shutdown simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the junction-ambient thermal resistance. Fig. 21 shows this dissipable power as a function of ambient temperature for different thermal resistance.

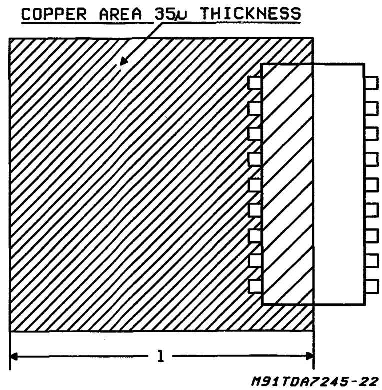
Figure 21: Maximum Allowable Power Dissipation vs. Ambient Temperature



MOUNTING INSTRUCTIONS

The TDA7245 is assembled in the POWERDIP, in which 9 pins (from 10 to 18) are attached to the frame and remove the heat produced by the chip. Figure 22 shows a PC Board copper area used as a Heatsink (l = 65mm). The Thermal Resistance Junction-Ambient is 35°C.

Figure 22: Example of Heatsink using PC Board Copper (l = 65mm)



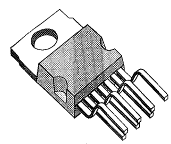
SGS-THOMSON MICROELECTRONICS

TDA7246

10W AUDIO AMPLIFIER WITH MUTING AND STAND-BY

PRODUCT PREVIEW

- MUTING/STAND-BY FUNCTIONS
- SUPPLY VOLTAGE UP TO 30V
- RMS OUTPUT POWER = 10W typ.
  (@ V_S = 24V, R_L = 8Ω, d = 10%)
  MUSIC POWER = 20Ω typ (R_L = 4W, d = 10%)
- HIGH SUPPLY VOLTAGE REJECTION
- THERMAL SHUTDOWN



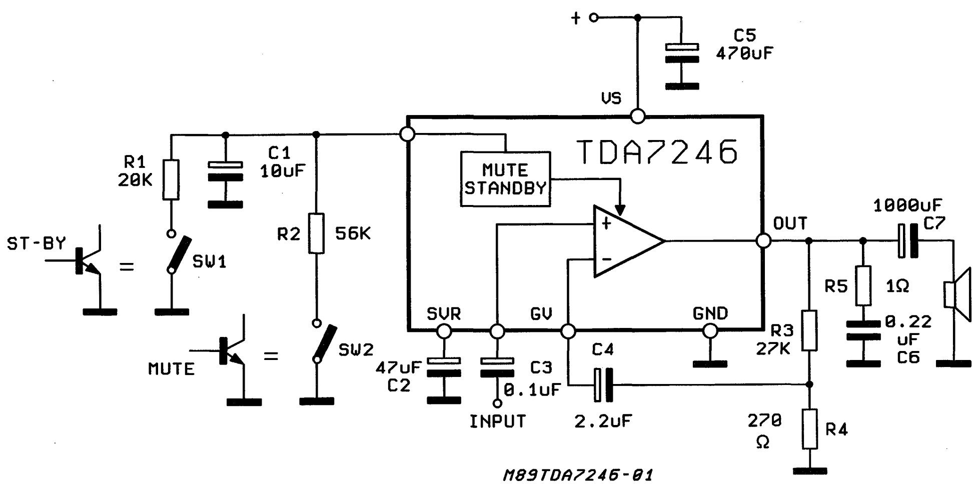
Heptawatt

ORDERING NUMBER: TDA7246

DESCRIPTION

The TDA7246 is a monolithic integrated circuit in HEPTAWATT package, intended for use as low frequency power amplifier in a wide range of applications in radio and TV sets.

TEST AND APPLICATION CIRCUIT

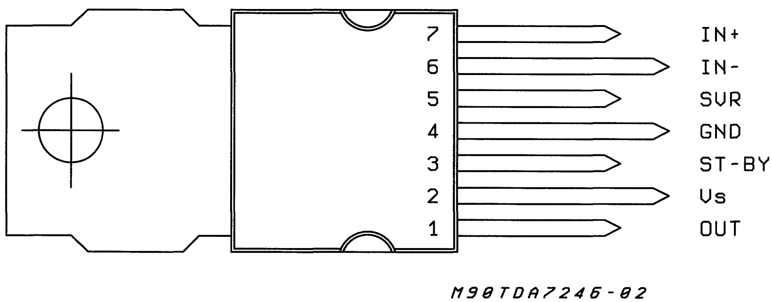


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	30	V
I_O	Output Peak Current (non repetitive t = 100µs)	3	A
I_O	Output Peak Current (repetitive, f = ≥ 20Hz)	2.5	A
P_{tot}	Power Dissipation at T_{case} = 70°C	20	W
T_{stg}, T_j	Storage and junction Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance junction-case	Max	4	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb} = 25°C, V_S = 22V, f = 1kHz; unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		12		30	V
V_O	Quiescent Output Voltage	V_S = 24V		11.6		V
I_d	Quiescent Drain Current	V_S = 24V		20	35	mA
P_O	Output Power	Music Power, IEC268-3 Rules V_S = 26V, R_L = 4Ω, d = 10% d = 10%, rms values V_S = 22V, R_L = 4Ω V_S = 24V, R_L = 8Ω d = 1%, rms values V_S = 22V, R_L = 4Ω V_S = 24V, R_L = 8Ω	 12	 20 14 10 11 8		 W W W W W
d	Total Harmonic Distortion	V_S = 22V, R_L = 4Ω, P_O = 50mW to 9W V_S = 24V, R_L = 8Ω, P_O = 50mW to 6W		0.1 0.1	0.5	% %
R_I	Input Resistance	f = 1kHz	30			kΩ
BW	Small signal bandwidth (-3dB)	P_O = 1W; R_L = 4Ω	40 to 40,000			Hz
G_V	Voltage Gain (open loop)	f = 1kHz		75		dB
G_V	Voltage Gain (closed loop)	f = 1kHz; PO = 1W; R_L = 4Ω	39	40	41	dB
e_N	Total Input Noise (*)	R_g = 50Ω R_g = 1kΩ R_g = 10kΩ		1.7 2 3	 6	mV µV µV
SVR	Supply Voltage Rejection	R_L = 4Ω; f_{ripple} = 100Hz R_g = 10kΩ; V_{ripple} = 0.5Vrms	40	50		dB
T_{sd}	Thermal shut-down Junction Temperature			150		°C

*) B = 22Hz to 22kHz

MUTE/STAND-BY FUNCTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ATT_M	Muting Attenuation	f = 100Hz to 10kHz P_O = 2W, R_L = 4Ω	60	65		dB
$I_{pin3\text{-}M}$	Pin3 current @ Mute	SW2 closed, SW1 open		80		µA
$ATT_{ST\text{-}BY}$	Stand-by Attenuation	f = 100Hz to 10kHz P_O = 2W, R_L = 4Ω	70	90		dB
$VT_{ST\text{-}BY}$	Stand-by Threshold (pin3)			3.8		V
$I_{pin3\text{-}ST\text{-}BY}$	Pin3 Current @ STAND-BY	SW1 closed		160	280	µA
$I_{d\text{-}ST\text{-}BY}$	Drain Current @ STAND-BY	SW1 closed		1	3	mA
V_{pin3}	Pin3 DC Voltage	SW1,2 open		6.3		V

MUTE/STAND-BY SETTING

SW1	SW2	MODE
OPEN	OPEN	PLAY
OPEN	CLOSED	MUTING
CLOSED	X	STAND-BY

Figure 1: Output Power vs. Supply Voltage

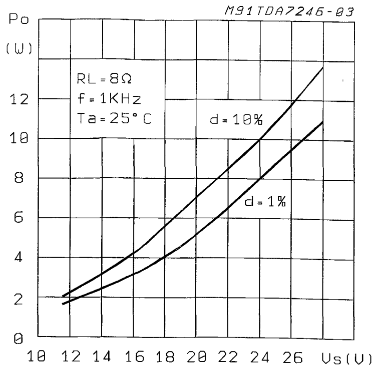


Figure 2: Output Power vs. Supply voltage

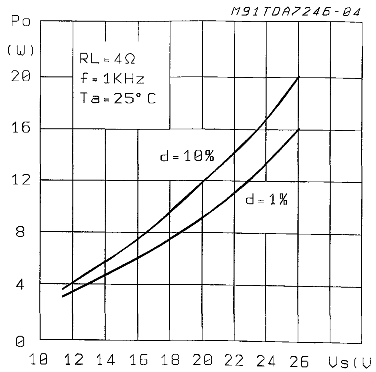


Figure 3: Distortion vs. Output power

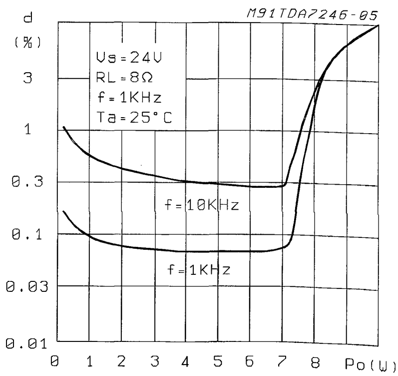


Figure 4: Distortion vs. Output Power

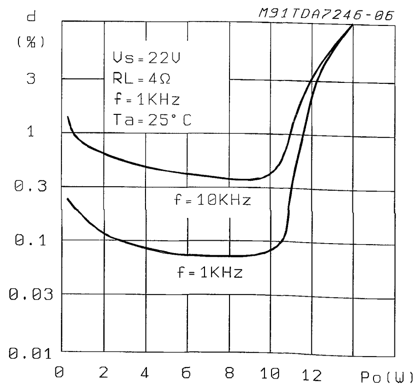


Figure 5: Supply Voltage Rejection vs. Frequency

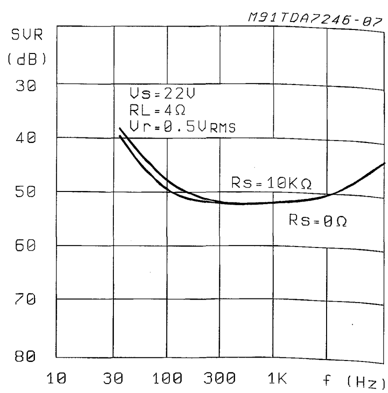


Figure 6: Qiescent Current vs. Suply Voltage

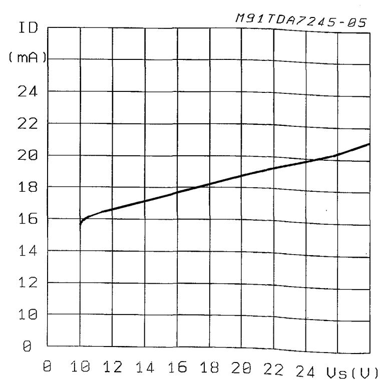


Figure 7: Power Dissipation and Efficiency vs. Output Power

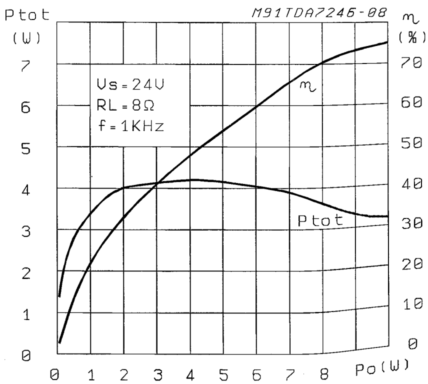


Figure 8: Power Dissipation and Efficiency vs. Output Power

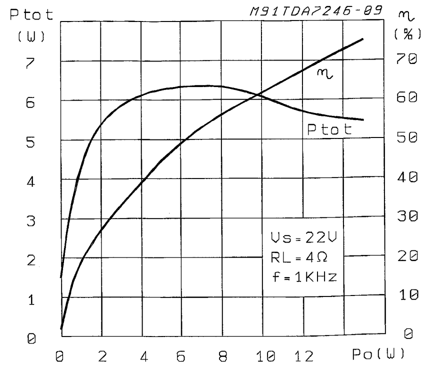


Figure 9: Attenuation vs. Vpin3

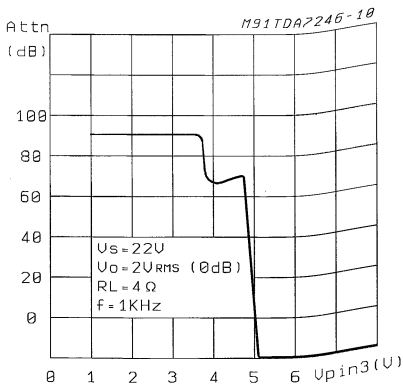


Figure 10: Maximum Allowable Power Dissipation vs. Ambient Temperature

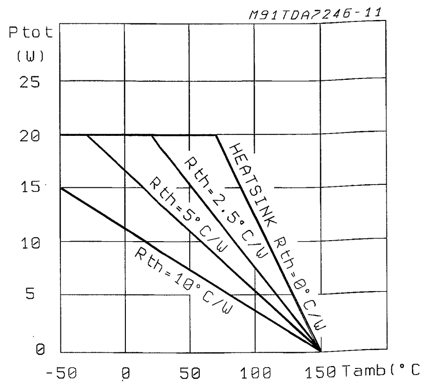


Figure 11: Application Circuit

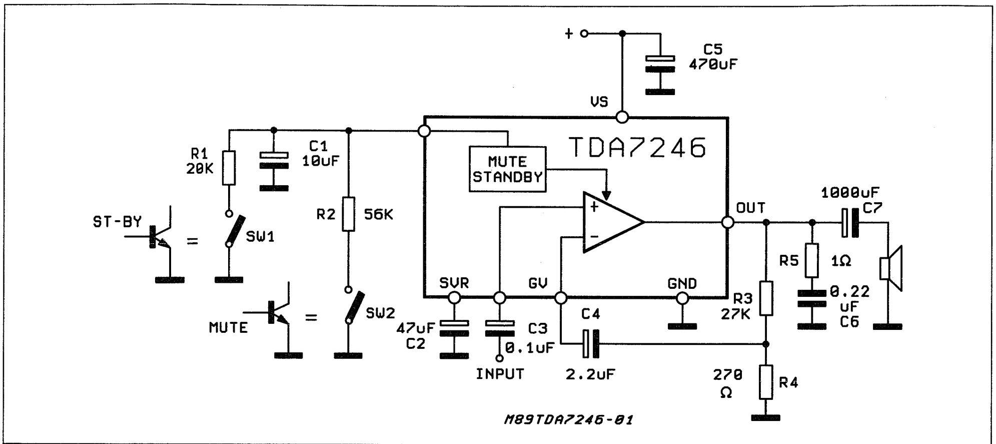
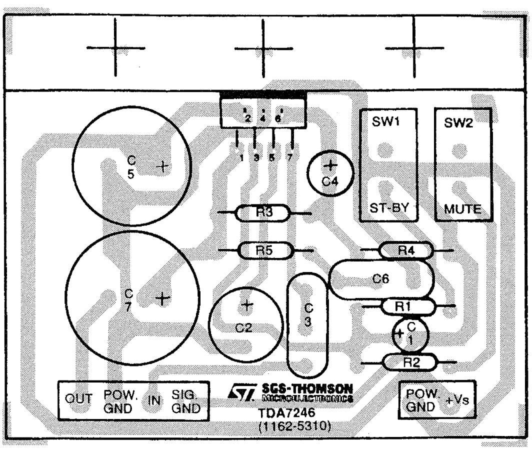


Figure 12: P.C. Board and Component Layout of the Circuit of Figure 11 (1:1 scale)



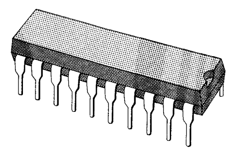
SGS-THOMSON
MICROELECTRONICS

TDA7250

60W HI-FI DUAL AUDIO DRIVER

- WIDE SUPPLY VOLTAGE RANGE: 20 TO 90V (± 10 TO ± 45V)
- VERY LOW DISTORTION
- AUTOMATIC QUIESCENT CURRENT CONTROL FOR THE POWER TRANSISTORS WITHOUT TEMPERATURE SENSE ELEMENTS
- OVERLOAD CURRENT PROTECTION FOR THE POWER TRANSISTORS
- MUTE/STAND-BY FUNCTIONS
- LOW POWER CONSUMPTION
- OUTPUT POWER 60W/8Ω AND 100W/4Ω

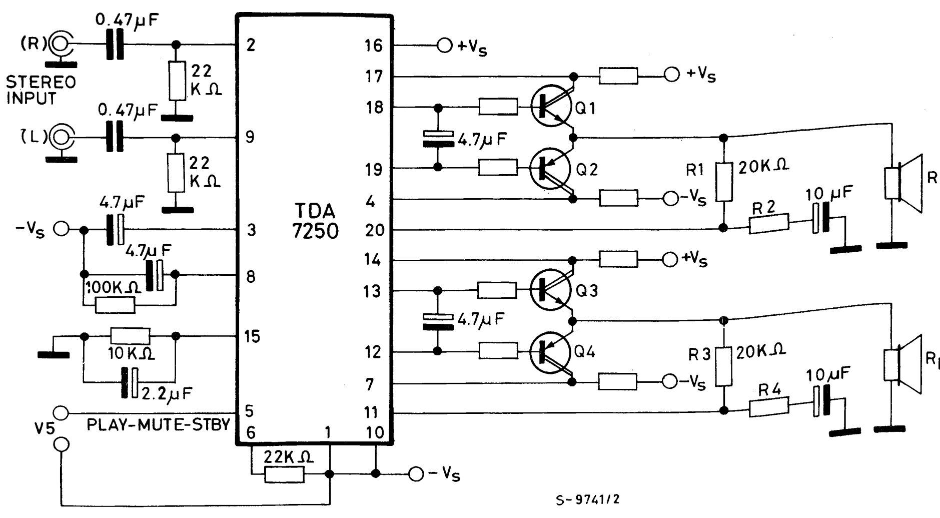
The TDA7250 stereo audio driver is designed to drive two pair of complementary output transistor in the Hi-Fi power amplifiers.



DIP-20 Plastic
(0.4)

ORDERING NUMBER: TDA7250

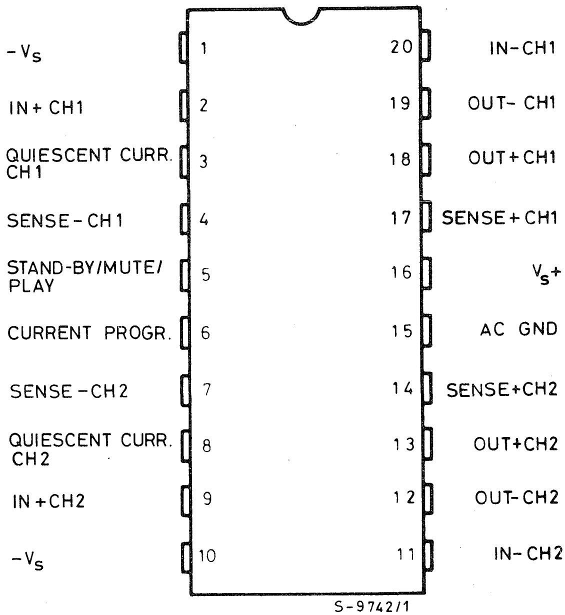
APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	100	V
P_{tot}	Power dissipation at $T_{amb} = 60°C$	1.4	W
T_j, T_{stg}	Storage and junction temperature	-40 to +150	°C

CONNECTION DIAGRAM
(Top view)



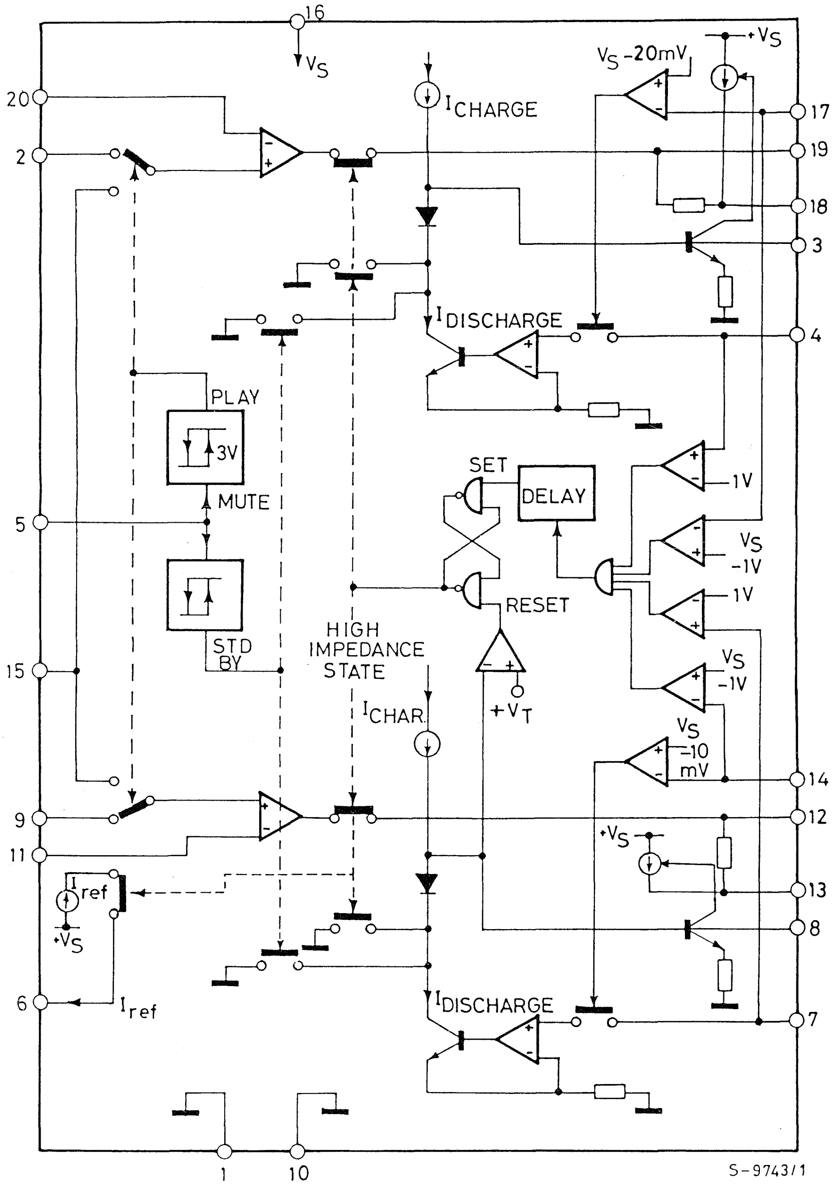
THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	65	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	V_s- POWER SUPPLY	Negative supply voltage.
2	NON-INV. INP. CH. 1	Channel 1 input signal.
3	QUIESC. CURRENT CONTR. CAP. CH 1	This capacitor works as an integrator, to control the quiescent current to output devices in no-signal conditions on channel 1.
4	SENSE (-) CH. 1	Negative voltage sense input for overload protection and for automatic quiescent current control.
5	ST. BY / MUTE / PLAY	Three-functions terminal. For V_{IN} = 1 to 3V, the device is in MUTE and only quiescent current flows in the power stages;- for $V_{IN} < 1V$, the device is in STAND-BY mode and no quiescent current is present in the power stages; - for $V_{IN} > 3V$, the device is fully active.
6	CURRENT PROGRAM	High impedance power-stages monitor.
7	SENSE (-) CH. 2	Negative voltage sense input for overload protection and for automatic quiescent current control.
8	QUIESC. CURRENT CONTR. CAP. CH. 2	This capacitor works as an integrator, to control the quiescent current to output devices in no-signal conditions on channel 2. If the voltage at its terminals drops under 250mV, it also resets the device from high-impedance state of output stages.
9	NON-INV. INP. CH. 2	Channel 2 input signals.
10	V_s- POWER SUPPLY	Negative supply voltage.
11	INVERT. INP. CH. 2	Feedback from output (channel 2).
12	OUT (-) CH. 2	Out signal to lower driver transistor of channel 2.
13	OUT (+) CH. 2	Out signal to higher driver transistor of channel 2.
14	SENSE (+) CH. 2	Positive voltage sense input for overload protection and for automatic quiescent current control.
15	COMMON AC GROUND	AC input ground in MUTE condition.
16	V_s+ POWER SUPPLY	Positive supply voltage.
17	SENSE (+) CH. 1	Positive voltage sense input for overload protection and for automatic quiescent current control.
18	OUT (+) CH. 1	Out signal to high driver transistor of channel 1.
19	OUT (-) CH. 1	Out signal to low driver transistor of channel 1.
20	INVERT. INP. CH. 1	Feedback from output (channel 1).

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = ± 35V, play mode, unless otherwise specified)

	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			± 10		± 45	V
I_d	Quiescent drain current	Stand-by mode			8		mA
		Play mode			10	14	
I_b	Input bias current				0.2	1	μA
V_{os}	Input offset voltage				1	± 10	mV
I_{os}	Input offset current				100	200	nA
G_v	Open loop voltage gain	f = 100Hz			90		dB
		f = 10KHz			60		
e_N	Input noise voltage	R_G = 600Ω B = 20Hz to 20KHz			3		μV
SR	Slew rate				10		V/μs
d	Total harmonic distortion	G_v = 26dB	f = 1KHz		0.004		%
		P_o = 40W	f = 20KHz		0.03		
V_{opp}	Output voltage swing				60		V_{pp}
P_o	Output power (*)	V_s = ± 35V V_s = ± 30V V_s = ± 35V	R_L = 8Ω R_L = 8Ω R_L = 4Ω		60 40 100		W
I_o	Output current				± 5		mA
SVR	Supply voltage rejection	f = 100Hz			75		dB
C_s	Channel separation	f = 1KHz			75		dB

MUTE / STANDBY / PLAY FUNCTIONS

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_i	Input current (pin 5)			0.1		μA
V_{th}	Comparator standby/mute threshold (**)		1.0	1.25	1.5	V
H	Hysteresis standby/mute			200		mV
V_{th}	Comparator mute/play threshold (**)		2.4	3.0	3.6	V
H	Hysteresis mute/play			300		mV
	Mute attenuation	f = 1KHz		60		dB
V_i	Input voltage max. (Pin 5)		12 (**)			V

(*) Application circuit of fig. 1 f = 1KHz; d = 0.1%; G_v = 26dB
(**) Referred to $-V_S$

ELECTRICAL CHARACTERISTICS (continued)

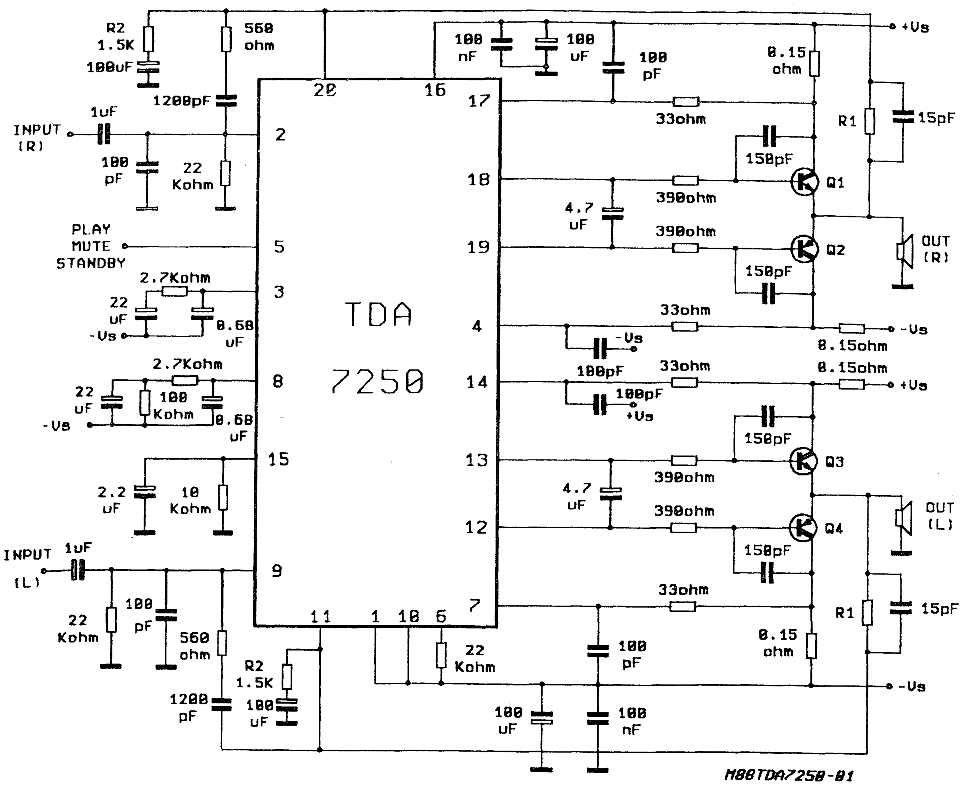
CURRENT SURVEY CIRCUITRY

	Comparator reference	to $+V_S$ to $-V_S$	0.8 0.8	1 1	1.4 1.4	V V
t_d	Delay time		10			µs

QUIESCENT CURRENT CONTROL

	Capacitor current	Charge Discharge	30 250	60 500		µA µA
	Comparator reference	to $+V_S$ to $-V_S$	10	20 10	25	mV mV

Fig. 1 - Application circuit with Power Darlingtons



NOTE: Q1/Q2 = Q3/Q4 = TIP 142/TIP 147
GV = 1+R1/R2

Fig. 2 - Output power vs. supply voltage

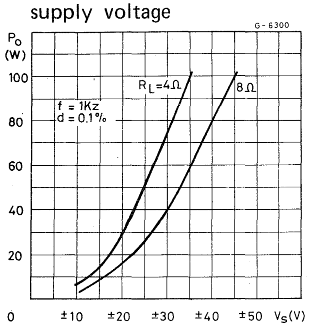


Fig. 3 - Distortion vs. output power (*)

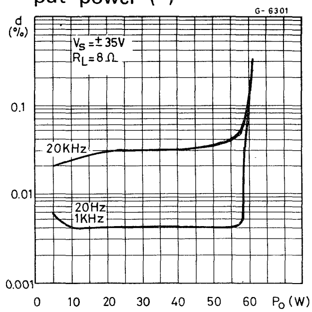


Fig. 4 - Channel separation

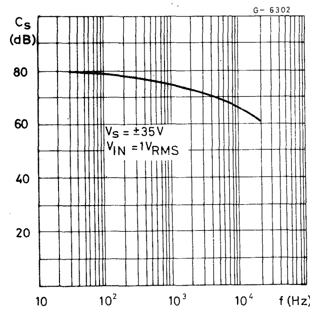


Fig. 5 - Supply voltage rejection vs. frequency

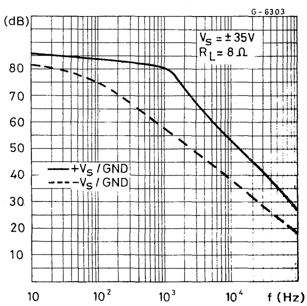


Fig. 6 - Quiescent current vs. supply voltage

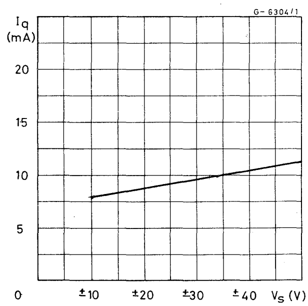


Fig. 7 - Quiescent current vs. T_{amb}

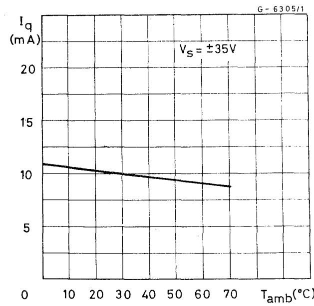


Fig. 8 - Total dissipated power vs. output power (*)

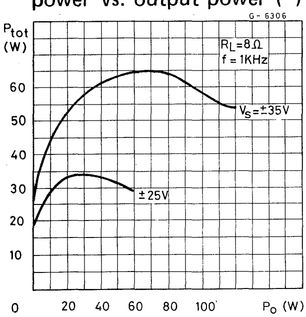


Fig. 9 - Efficiency vs. output power (*)

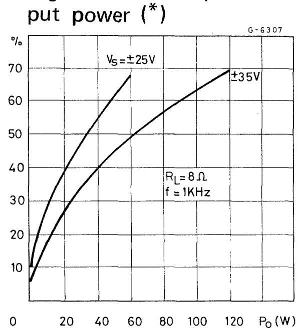
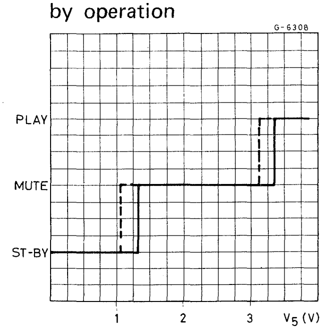


Fig. 10 - Play-mute stand-by operation



(*) Complete circuit

Fig. 11 - Application circuit using power transistors

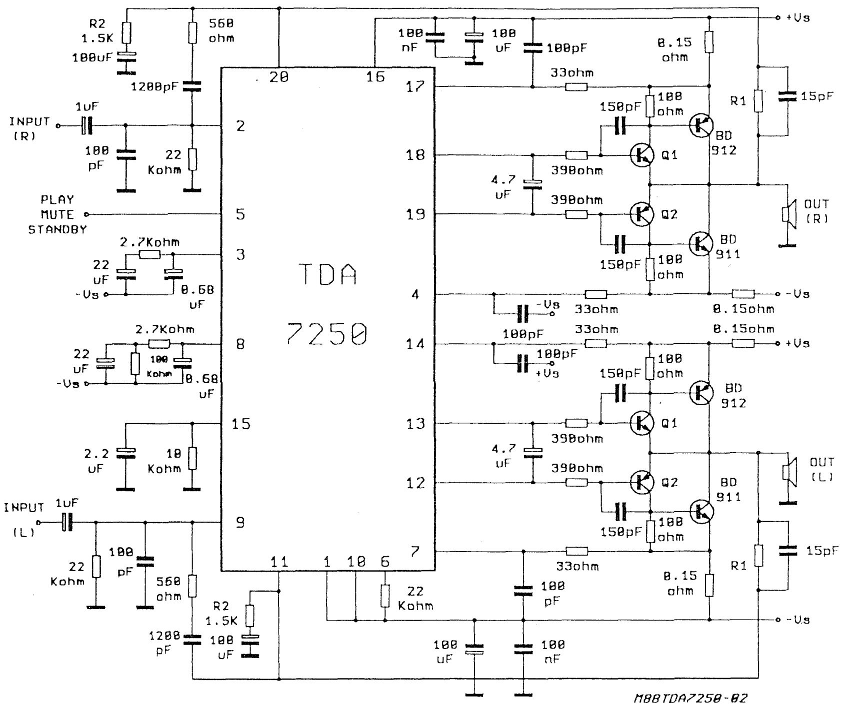


Fig. 12 - Suggested transistor types for various loads and powers.

$R_L = 8\,\Omega$

15W	30W	50W	70W
BDX 53/54A	BDX 53/54B	BDW 93/94B	TIP 142/147

$R_L = 4\,\Omega$

30W	50W	90W	130W
BDW 93/94A	BDW 93/94B	BDV 64/65B	MJ 11013/11014

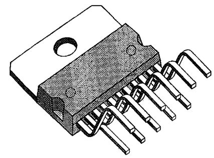
SGS-THOMSON MICROELECTRONICS

TDA7256

30W BRIDGE FULLY PROTECTED CAR RADIO AMPLIFIER

PRELIMINARY DATA

- NO AUDIBLE POP DURING MUTE AND STANDBY OPERATIONS
- MUTING TTL COMPATIBLE
- VERY LOW STANDBY CONSUMPTION
- PROGRAMMABLE TURN ON DELAY
- DIFFERENTIAL INPUT
- SHORT CIRCUIT PROTECTIONS: RL SHORT - OUT TO GROUND - OUT TO Vs
- OTHER PROTECTIONS:
  - Load dump voltage surge
  - Loudspeaker DC current
  - Very inductive load
  - Overrating temperature
  - Open ground

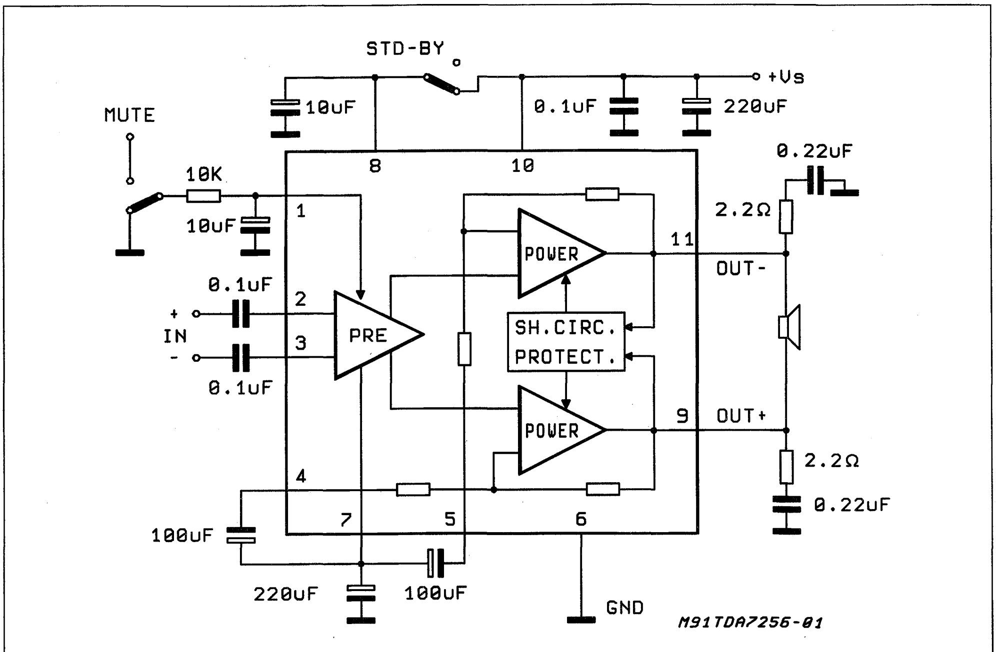


Multiwatt-11
ORDERING NUMBER: TDA7256

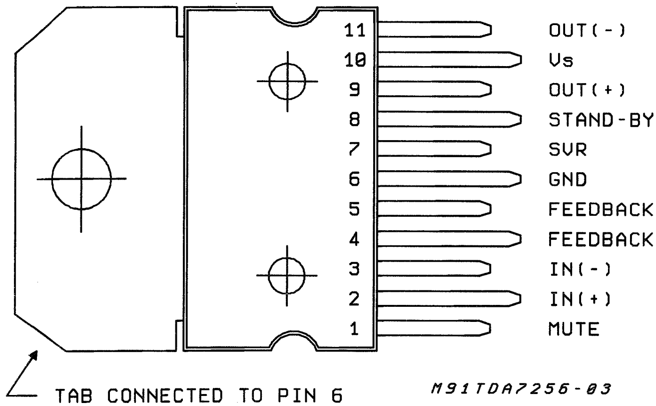
DESCRIPTION

The TDA7256 is a class AB fully protected bridge power amplifier, designed for car radio applications. The high current capability allows to drive low impedance loads (up to 2Ω). The differential inputs availability makes it particularly suitable for boosters and active loudspeakers applications.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Operating Supply Voltage	18	V
V_S	DC Supply Voltage	28	V
V_S	Peak Supply Voltage (for 50ms)	40	V
I_o	Output Peak Current (non repetiitive t = 0.1ms)	internally limited	
I_o	Output Peak Current Repetitive f > 10Hz	5.5	A
P_{tot}	Power Dissipation Tcase = 85°C	30	W
T_{stg}, T_J	Storage and Junction Temperature Range	-40 to +150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	2.2	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 14.4V, R_L = 4Ω, f = 1KHz; T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		8		18	V
I_q	Quiescent Drain Current			80	150	mA
R_i	Input Resistance		50			KΩ
CMR	Common Mode Rejection	f = 1KHz, V_{in} = 100mV		60		dB
V_{OS}	Output Offset Voltage				150	mV
P_o	Output Power	d = 10% R_L = 4Ω R_L = 3.2Ω R_L = 2Ω	18	22 26 30		W W W
d	Distortion	P_o = 0.1W to 13W		0.05	0.5	%
G_V	Voltage Gain (CL)			36		dB
e_N	Total Input Noise Voltage	R_g = 10KΩ, B = 22Hz to 22KHz		3	10	µV
SVR	Supply Voltage Rejection	R_s = 10KΩ, V_r = 1Vrms, f = 300Hz	45	60		dB
	Muting Attenuation	V_{ref} = 1Vrms, f = 100Hz to 10KHz	60			dB
	Muting-in Threshold Voltage	Pin 1	2.4			V
	Muting-out Threshold Voltage	Pin 1			0.8	V
	Stand-by Attenuation	Vref = 1Vrms	60			dB
	Stand-by Current Consumption				100	µA
T_{SD}	Thermal Shut-down Junction Temperature			145		°C

Figure 1: Test and Application Circuit

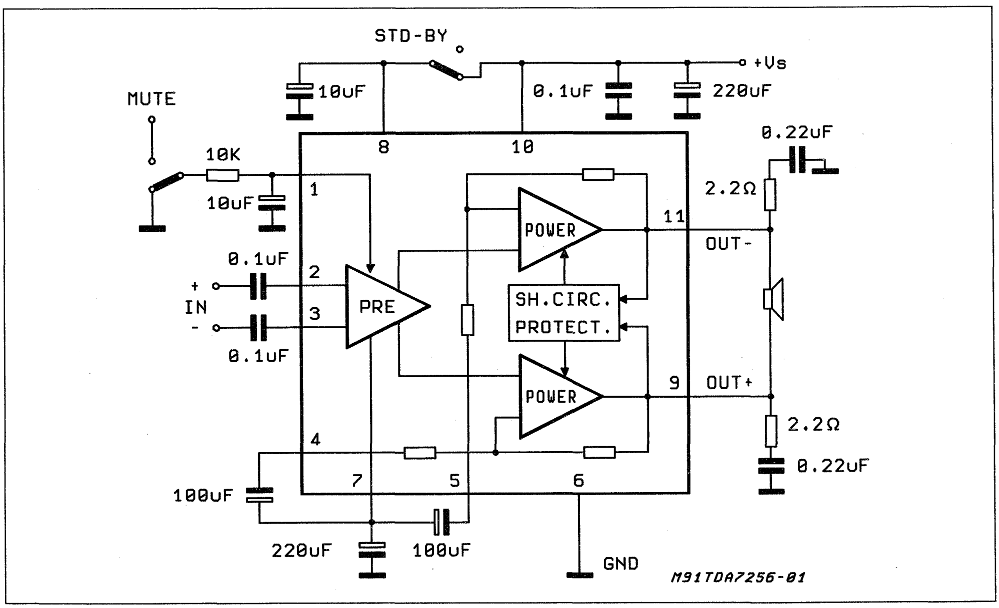


Figure 2: P.C. and Layout of the fig.1 (1:1 scale)

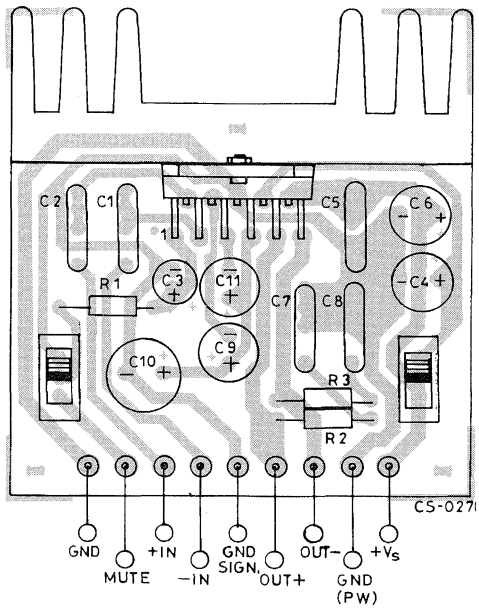


Figure 3: Drain Current vs. Supply Voltage

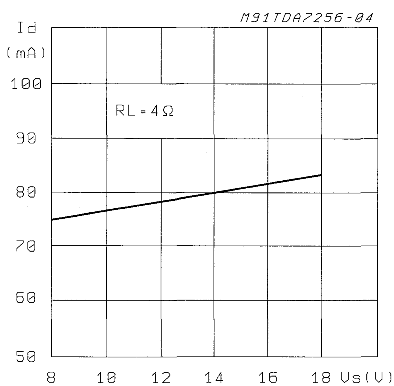


Figure 4: Output Power vs. Supply Voltage

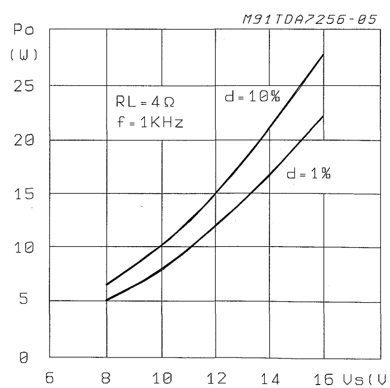


Figure 5: Output Power vs. Supply Voltage

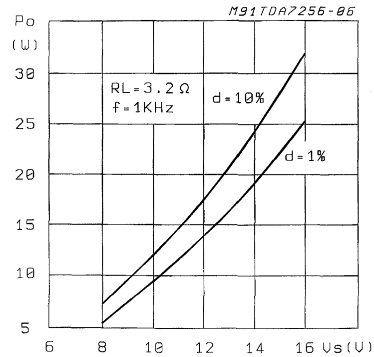


Figure 6: Output Power vs. Supply Voltage

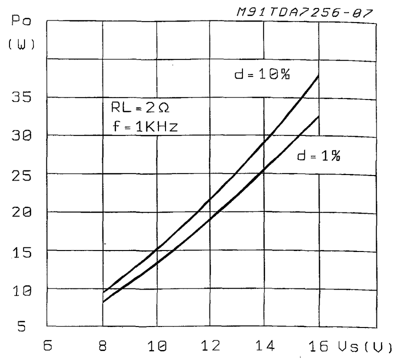


Figure 7: Distortion vs. Output Power

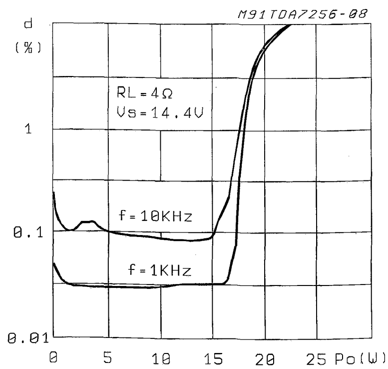


Figure 8: Distortion vs. Output Power

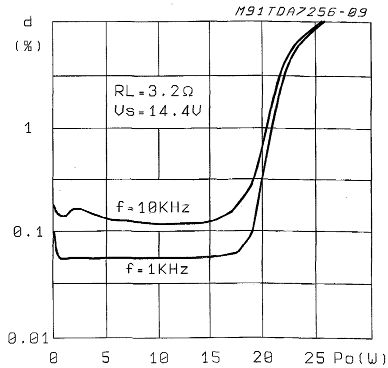


Figure 9: Distortion vs. Output Power

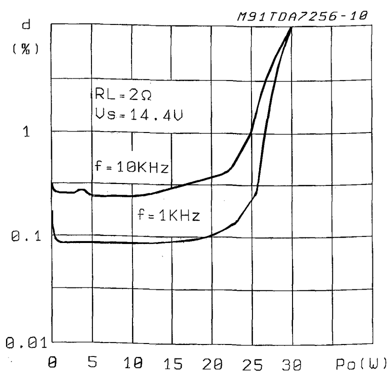


Figure 10: Distortion vs. Frequency

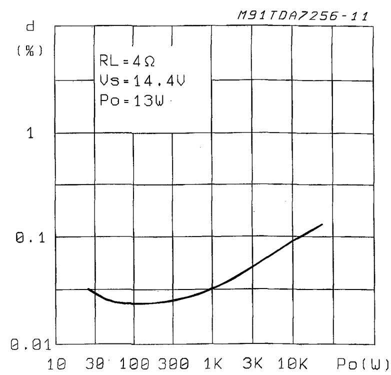


Figure 11: Distortion vs. Frequency

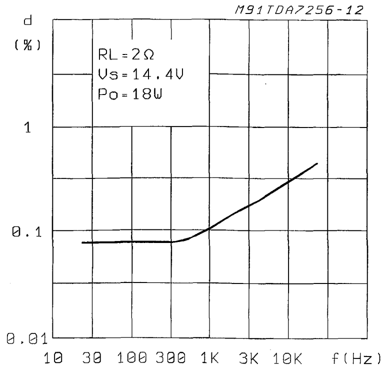


Figure 12: SVR vs. Frequency

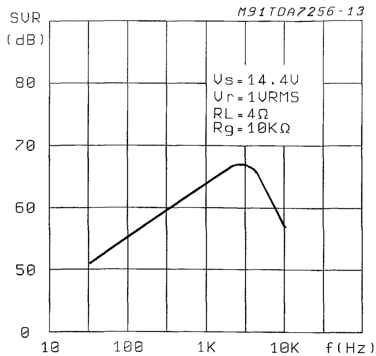


Figure 13: CMRR vs. Frequency

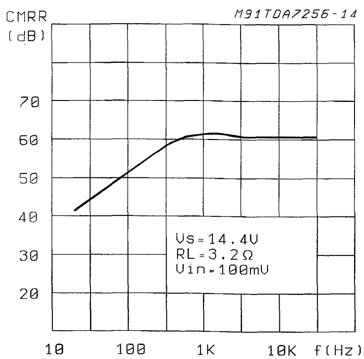


Figure 14: Power Dissipation & Efficiency vs. Output Power

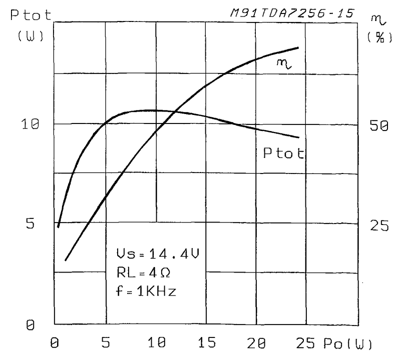


Figure 15: Power Dissipation & Efficiency vs. Output Power

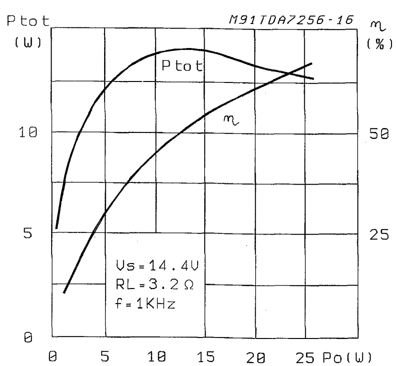
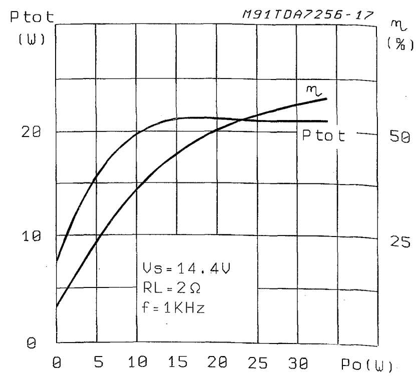


Figure 16: Power Dissipation & Efficiency vs. Output Power



CIRCUIT DESCRIPTION

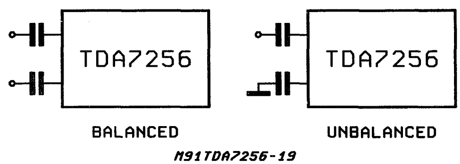
INPUT STAGE

The input stage is a differential type preamplifier stage with two independent inputs and two outputs in phase opposition.

It is designed for particular linearity characteristics in order to have output amplitude large enough (1VPP) yet maintaining low distortion.

The voltage gain of the stage is 6 dB.The possibility to use the differential input allows the system immunity to common-mode noise in case of long wire connections (fig. 17)

Figure 17: Balanced -Unbalanced Input

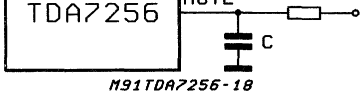


MUTE

The mute circuit (TTL compatible) acts at preamplifier level and disables the inputs without changing the DC voltage values. In such a way the operation is fully popless.The use of a RC network produces a soft reduction of the audio signal providing the best effect from the acoustic point of view (fig 18).

The mute circuit is also activated during turn-on/turn-off operations when the voltage at stand-by pin is lower than about 2 volt

Figure 18: Soft Muting



TURN-ON

The TDA7256 is fully popless at turn-on thanks to a delay circuit which keeps the output low during the capacitors charge transient.

The delay-time is given by the following formula:

$$T_o = 800\ C10 + 600\ (C9 + C11)\left(\frac{C10}{C9 + C11} + 1\right)$$

TURN-OFF

The ground compatible structures and the choice of a soft turn-off circuit ensure a fully popless operation.

OUTPUT STAGE

It is a power stage designed in a way of being able to drive loads up to 2 ohm in bridge configuration without bootstrap capacitors (22 W with R_L=4 ohm , 30W with R_L=2 ohm).

SVR

The noise coming from the car environment are essentially inside the bandwith from 300 Hz to 6 KHz.

The ripple rejection circuit which utilizes also the gain capacitors C11,C9 ensures in this frequency range a rejection typ. of 60dB.

SHORT CIRCUIT PROTECTION

The short circuit protection circuits intervene in the following cases:

- s.c. between one output and ground
- s.c. between one output and +Vs
- s.c. between the outputs

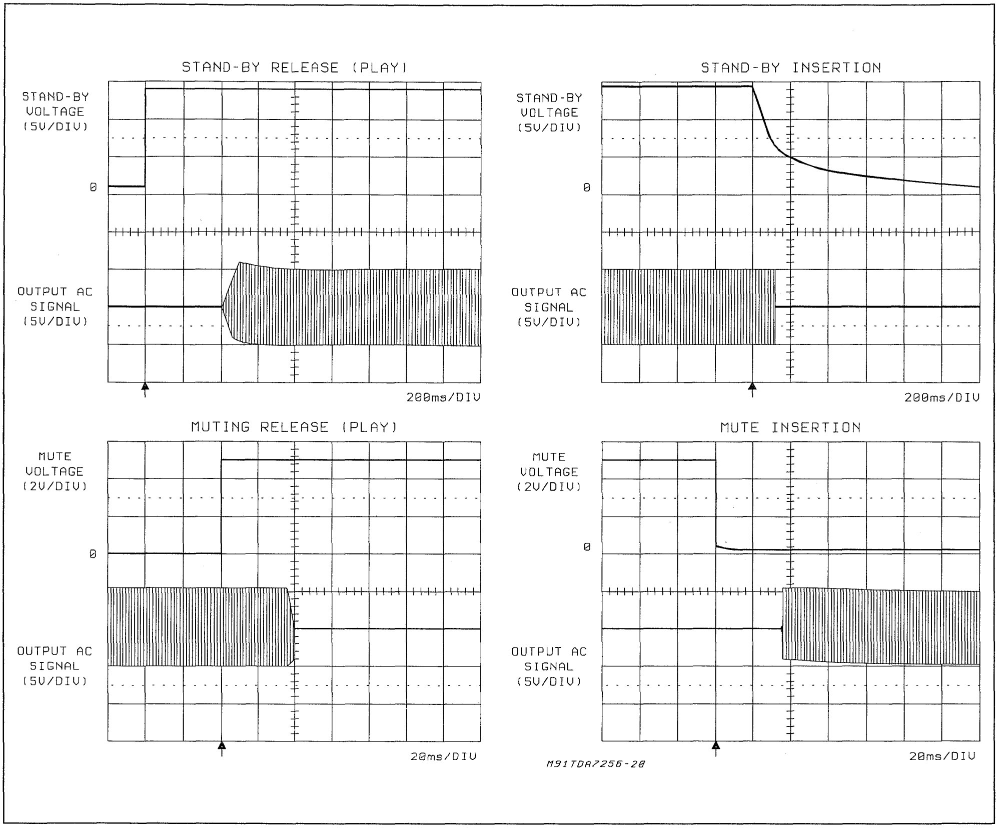
In the first two cases they stop the current in both the final stages,allowing also the loudspeaker protection.In the last case the current is limited, thus avoiding the load point to reach the SOA of the output transistors.

STAND-BY

In stand-by condition the current generators are disabled:the current drops to a very low value (few µA). Also this function is fully popless.

Fig. 19 shows the silent transients of turn-on and turn-off operations through both the mute and the stand-by pins.

Figure 19: Silent Transients Through the Mute and Stand-by pins.



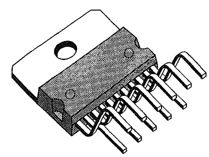
SGS-THOMSON MICROELECTRONICS

TDA7262

20+20W STEREO AMPLIFIER WITH STAND-BY

ADVANCE DATA

- WIDE SUPPLY VOLTAGE RANGE
- HIGH OUTPUT POWER
  28+28W TYP. MUSIC POWER
  20+20W @ THD = 10%, $R_L = 4\Omega$, $V_S = 28V$
- HIGH CURRENT CAPABILITY (UP TO 3.5A)
- STAND-BY FUNCTION
- AC SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION

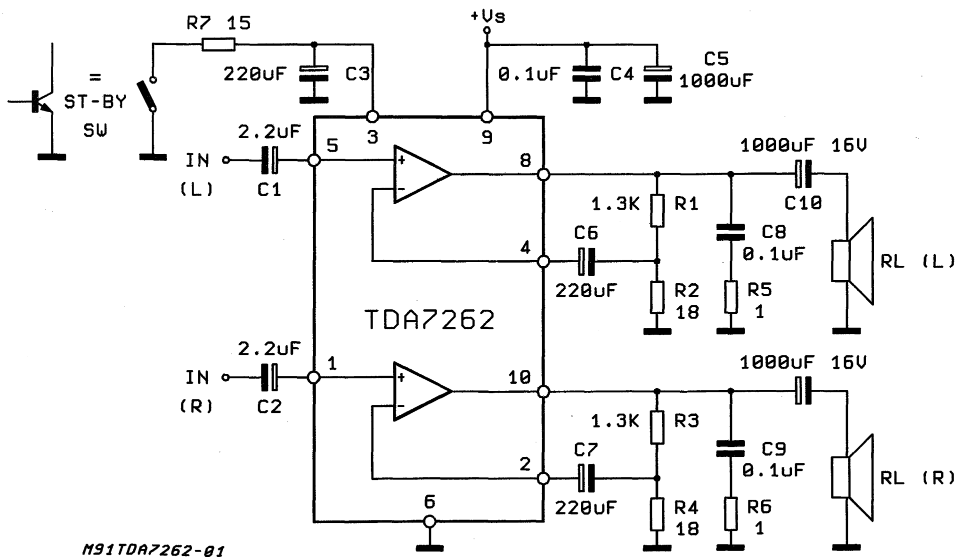


Multiwatt-11
ORDERING NUMBER: TDA7262

DESCRIPTION

The TDA7262 is class AB dual Hi-Fi Audio power amplifier assembled in Multiwatt package, specially designed for high quality stereo application as Hi-Fi music centers and TV sets.

Figure 1: Stereo Application Circuit with Stand-By

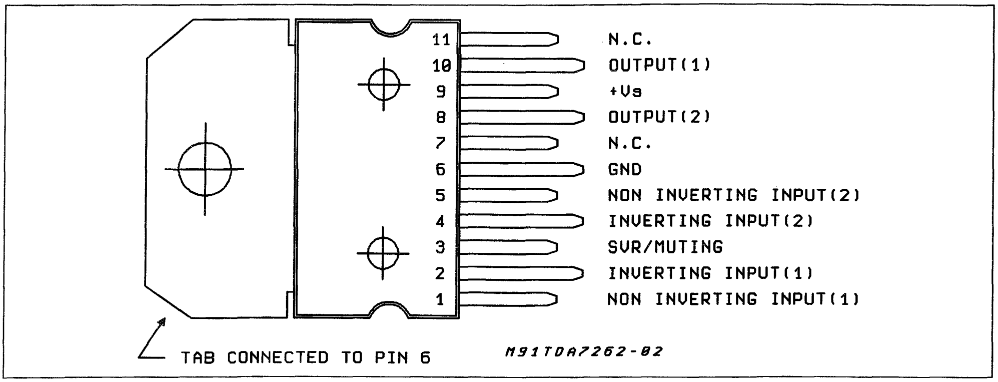


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

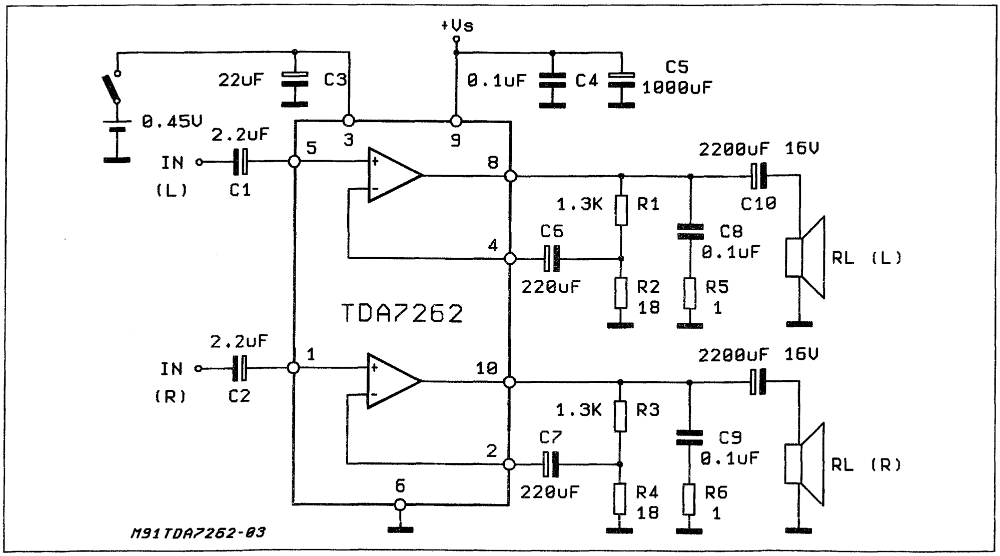
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	35	V
I_O	Output Peak Current (repetitive f > 20Hz)	3.5	A
I_O	Output Peak Current (non repetitive, t > 100µs)	4.5	A
P_{tot}	Power Dissipation (T_{case} = 70°C)	30	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

PIN CONNECTION



TEST CIRCUIT



THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	2.5	°C/W

ELECTRICAL CHARACTERISTICS

(Refer to the stereo test circuit, V_S = 28V; f = 1KHz; T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		8		32	V
V_O	Quiescent Output Voltage	V_S = 32V		15.5		V
I_d	Total Quiescent Current	V_S = 28V V_S = 32V		65 70	 120	mA mA
P_O	Output Power (each channel)	Music Power STD rules (T = 1s) V_S = 32V; d = 10%; R_L = 4Ω		28		W
		d = 10% R_L = 4Ω R_L = 8Ω	 10	 22 13		 W W
		d = 1% R_L = 4Ω R_L = 8Ω		 18 10		 W W
d	Total Harmonic Distortion	f = 100Hz to 10KHz P_O = 0.1 to 14W; R_L = 4Ω P_O = 0.1 to 8W; R_L = 8Ω		 0.2 0.1		 % %
CT	Cross Talk	R_L = 4Ω R_S = 100Ω f = 1KHz f = 10KHz		 60 50		 dB dB
V_i	Input Saturation Voltage	(Vrms)	300			mV
R_i	Input Resistance	f = 1KHz; non inverting Input	70	200		KΩ
f_L	Low Frequency roll-off (-3dB)	R_L = 4Ω		40		Hz
f_H	High Frequency roll-off (-3dB)	R_L = 4Ω		80		KHz
G_V	Closed Loop Voltage Gain	f = 1KHz	35.5	36	36.5	dB
ΔG_V	Closed Loop Gain match			0.5		dB
e_N	Total Input Noise Voltage	A Curve; R_S = 10KΩ		1.5		µV
		f = 22Hz to 22KHz; R_S = 10KΩ		2.5	8	µV
SVR	Supply Voltage Rejection (each channel)	R_S = 0 to 10KΩ; f_r = 100Hz V_r = 0.5V		55		dB
T_j	Thermal Shutdown Junction Temperature			145		°C

STAND-BY FUNCTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_3	Stand-By Threshold	V_S = 32V	0.45	0.9		V
A_M	Stand-By Attenuation	V_S = 32V; V_3 < 0.45V	60	100		dB
I_M	Stand-By Quiescent Current	V_S = 32V; V_3 < 0.45V		3	5	mA

APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of Figure 1. Different values can be used; the following table can help the designer.

Component	Recomm. Value	Purpose	Larger than	Smaller than
R1 and R3	1.3KΩ	Close loop gain setting (*)	Increase of gain	Decrease of gain
R2 and R4	18Ω		Decrease of gain	Increase of gain
R5 and R6	1Ω	Frequency stability	Danger of oscillations	
C1 and C2	2.2μF	Input DC decoupling	higher turn-on delay	- worse turn-ON pop - higer low freq. cutoff. Increase of noise
C3	22μF (**)	- Ripple rejection - Stand-by time constant	Increase of the Switch-on time	- Degradation of SVR - worse turn-OFF pop by stand-by
C4	100nF	Supply setting		Danger of oscillations
C5	1000μF	Supply setting		worse turn-OFF pop
C6 and C7	220μF	Feedback input DC decoupling		
C8 and C9	0.1μF	Frequency stability		Danger of oscillations
C10 and C11	1000μF to 2200μF	Output DC decoupling		Higher low-frequency cut-off

(*) Closed loop gain must be higher than 26dB.
(**) 220μF in case of stand-by utilization.

Figure 2: Ouput Power vs. Supply Voltage

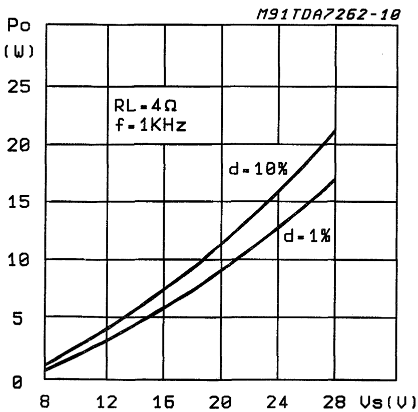


Figure 3: Ouput Power vs. Supply Voltage

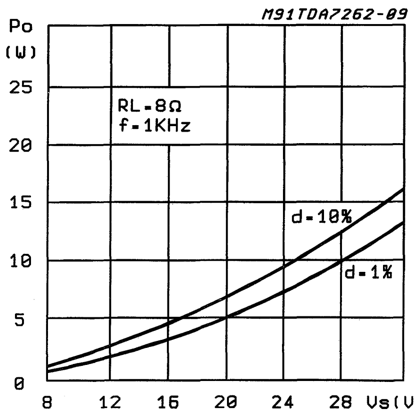


Figure 4: Distortion vs. Ouput Power

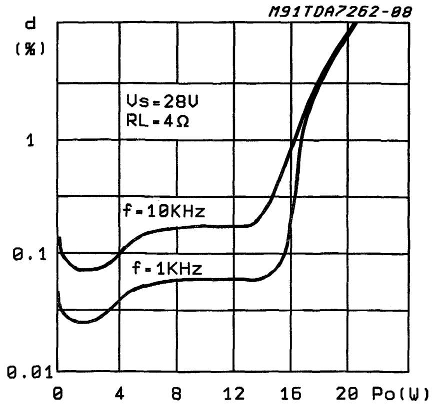


Figure 5: Distortion vs. Ouput Power

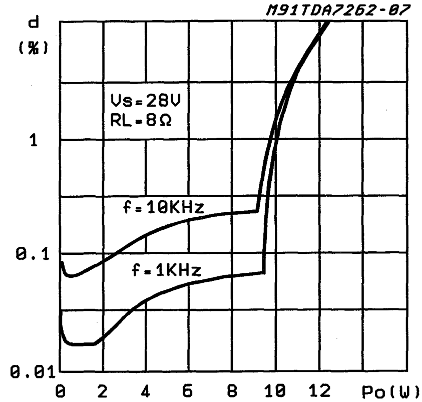


Figure 6: Quiescent Current vs. Supply Voltage

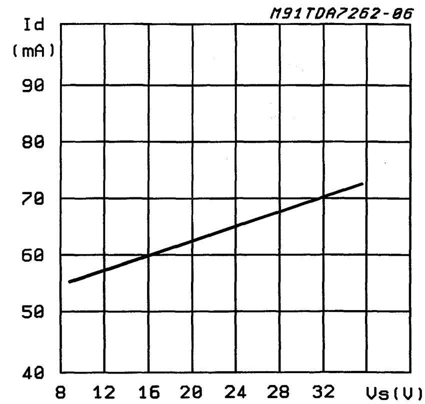


Figure 7: Supply Voltage Rejection vs. Frequency

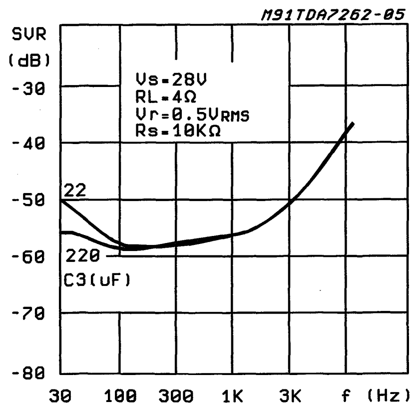


Figure 8: Output Attenuation vs. Vpin 3

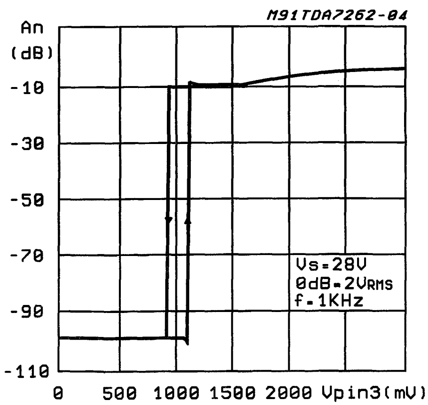


Figure 9: Total Power Dissipation & Efficiency vs. Output Power

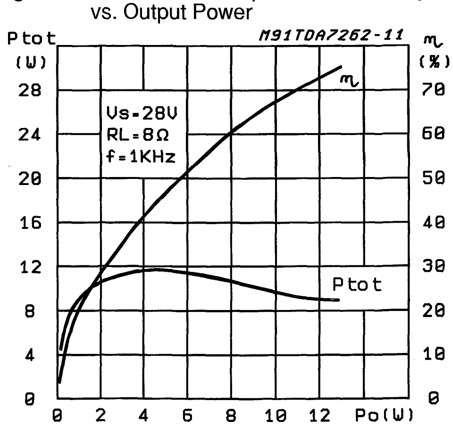


Figure 11: Total Power Dissipation & Efficiency vs. Output Power

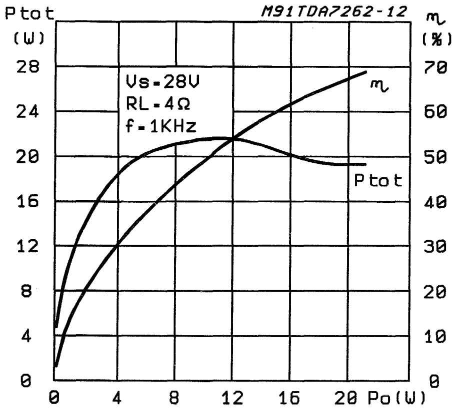
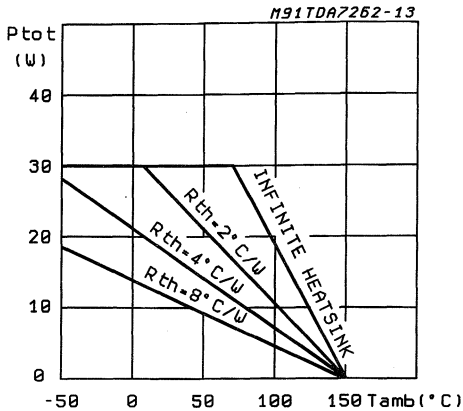


Figure 12



BUILD-IN PROTECTION SYSTEMS

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature; all that happens is that P_O (and therefore Ptot) and I_O are reduced. The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Figure 12 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Short circuit (AC Conditions)

The TDA7262 can withstand accidental short circuits across the speaker made by a wrong connection during normal play operation.

MOUNTING INSTRCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

Thanks to the MULTIWATT package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

TDA7271
TDA7272

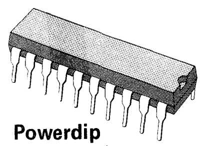
HIGH PERFORMANCE MOTOR SPEED REGULATOR

- TACHIMETRIC SPEED REGULATION WITH NO NEED FOR AN EXTERNAL SPEED PICK-UP
- V/I SUPPLEMENTARY PREREGULATION
- DIGITAL CONTROL OF DIRECTION AND MOTOR STOP
- SEPARATE SPEED ADJUSTMENT
- 5.5V TO 18V OPERATING SUPPLY VOLTAGE
- 1A PEAK OUTPUT CURRENT
- OUTPUT CLAMP DIODES INCLUDED
- SHORT CIRCUIT CURRENT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION (40V)

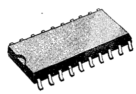
The TDA7211/12 are high performance motor speed controllers for small power DC motors as used in cassette players.

Using the motor as a digital tachogenerator itself the performance of true tacho controlled systems is reached.

A dual loop control circuit provides long term stability and fast settling behaviour.



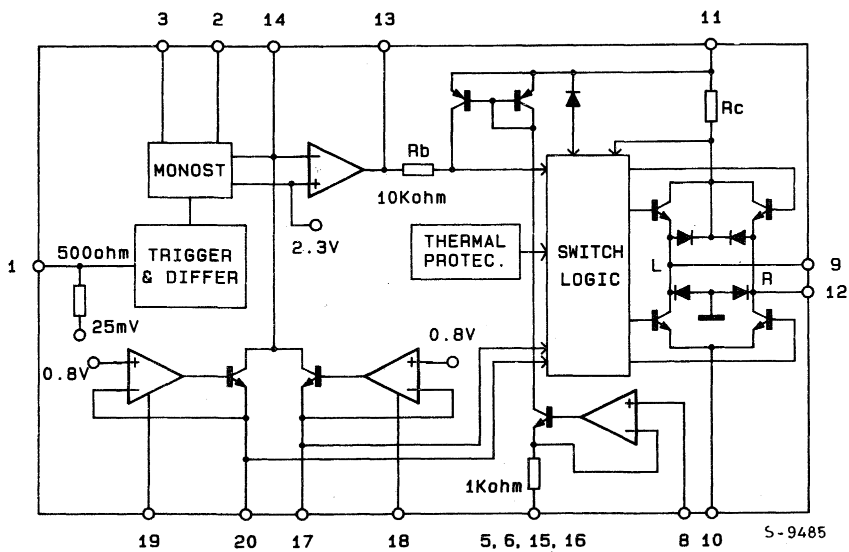
Powerdip (16 + 2 + 2)



SO-20

ORDERING NUMBER: TDA7272 (DIP)
TDA7211 (SO)

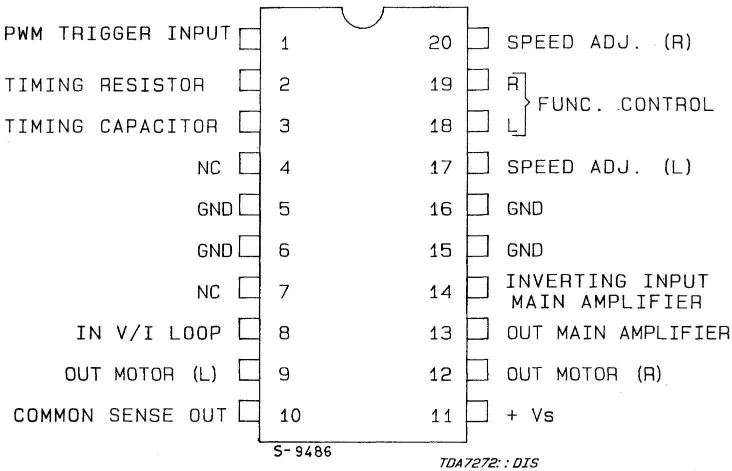
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SO	DIP	Unit
V_s	DC Supply voltage	24	24	V
V_s	Dump voltage (300ms)	40	40	V
I_o	Output current	internally limited		
P_{tot}	Power dissipation at $T_{pins} = 90°C$	4	4.3	W
	$T_{amb} \doteq 70°C$	0,7(*)	1	W
T_{stg}	Storage temperature	−40 to 150		°C

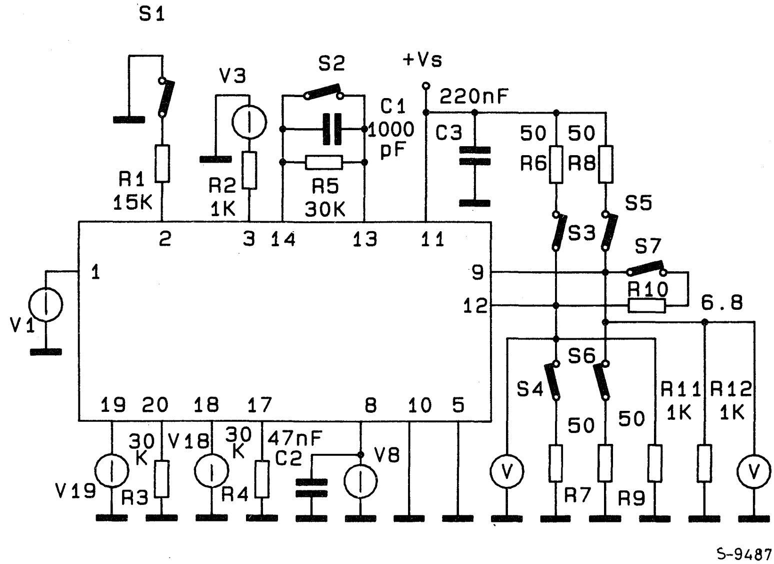
(*) at $T_{amb} = 90°C$

CONNECTION DIAGRAM
(Top view)



THERMAL DATA			DIP	SO	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient	max	80	85	°C/W
$R_{thj-pins}$	Thermal resistance junction-pins	max	14	15	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_S = 13.5V unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating supply voltage		5.5		18	V
I_S	Supply current	No load		5	12	mA

OUTPUT STAGE

I_O	Output current pulse		1			A
I_O	Output current continuous		250			mA
$V_{10-9, 12}$	Voltage drop	I_O = 250mA		1.2	1.5	V
$V_{11-9, 12}$	Voltage drop	I_O = 250mA		1.7	2	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
MAIN AMPLIFIER						
R_{14}	Input resistance		100			KΩ
I_b	Bias current			50		nA
V_{OFF}	Offset voltage			1	5	mV
V_R	Reference voltage	Internal at non inverting input		2.3		V
CURRENT SENSE AMPLIFIER V/I LOOP						
R_8	Input resistance		100			KΩ
G_L	Loop gain			9		
TRIGGER AND MONOSTABLE STAGE						
$V_{IN\ 1}$	Input allowed voltage		-0.7		3	V
$R_{IN\ 1}$	Input resistance			500		Ω
$V_{T\ Low}$	Trigger level			0		V
$V_{T\ B}$	Bias voltage (pin 1)		15	20	25	mV
$V_{T\ H}$	Trigger histeresis			10		mV
$V_{2\ REF}$	Reference voltage		750	800	850	mV
SPEED PROGRAMMING, DIRECTION CONTROL LOGIC AND CURRENT SOURCE PROGRAMMING						
$V_{18,\ 19\ Low}$	Input Low level				0.7	V
$V_{18,\ 19\ High}$	Input High level		2			V
$I_{18,\ 19}$	Input current	$0 < V_{18,\ 19} < V_S$		2		μA
$V_{17,\ 20\ REF}$	Reference voltage		735	800	865	mV

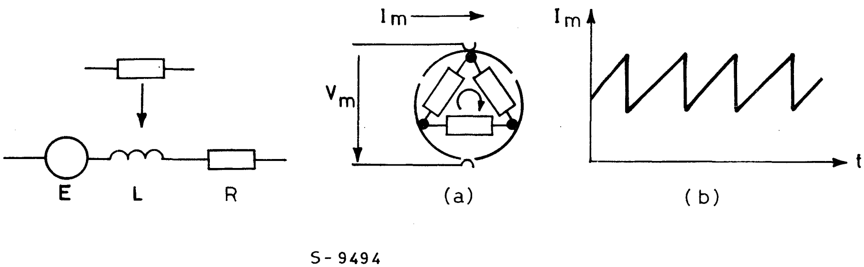
OPERATING PRINCIPLE

The TDA7272 novel applied solution is based on a tachometer control system without using such extra tachometer system. The information of the actual motor speed is extracted from the motor itself. A DC motor with an odd number of poles generates a motor current which contains a fixed number of discontinuities within each rotation. (6 for the 3 pole motor example on Fig. 1)

Deriving this inherent speed information from the motor current, it can be used as a replacement of a low resolution AC tachometer system. Because the settling time of the control loop is limited on principle by the resolution in time of the tachometer, this control principle offers a poor reaction time for motors with a low number of poles. The realized circuit is extended by a second feed forward loop in order to improve such system by a fast auxiliary control path.

This additional path senses the mean output current and varies the output voltage according to the voltage drop across the inner motor resistance. Apart from a current averaging filter, there is no delay in such loop and a fast settling behaviour is reached in addition to the long term speed motor accuracy.

Fig. 1 - Equivalent of a 3 pole DC motor (a) and typical motor current waveform (b)



BLOCK DESCRIPTION

The principle structure of the element is shown in Fig. 2. As to be seen, the motor speed information is derived from the motor current sense drop across the resistors R_S; capacitor CD together with the input impedance of 500Ω at pin 1 realizes a high pass filter.

This pin is internally biased at 20mV, each negative zero transition switches the input comparator. A 10mV hysteresis improves the noise immunity.

The trigger circuit is followed by an internal delay time differentiator.

Thus, the system becomes widely independent of the applied waveform at pin 1, the differentiator triggers a monostable circuit which provides a constant current duration. Both, output current magnitude and duration T, are adjustable by external elements CT and RT.

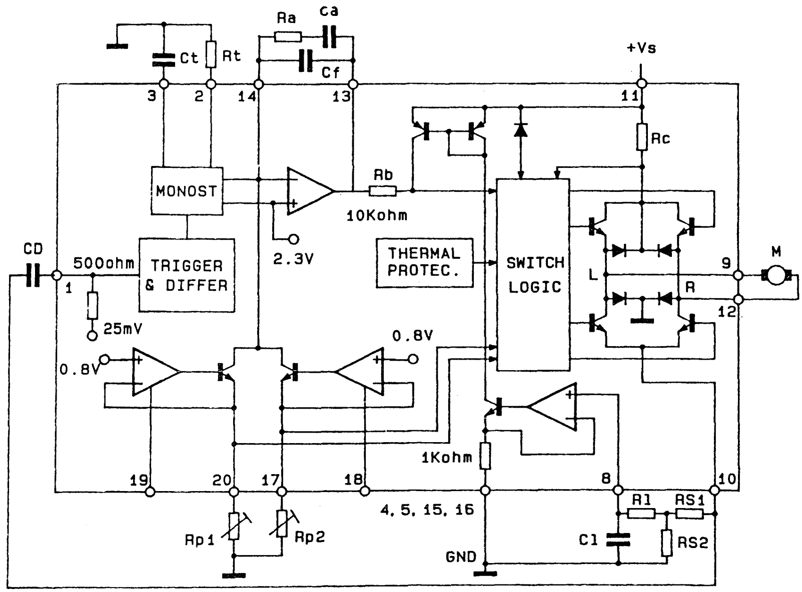
The monostable is retriggerable; this function prevents the system from fault stabilization at higher harmonics of the nominal frequency.

The speed programming current is generated by two separate external adjustable current sources. A corresponding digital input signal enables each current source for left or right rotation direction. Resistor RP1 and RP2 define the speed, the logical inputs are at pin 18 and 19.

At the inverting input (pin 14) of the main amplifier the reference current is compared with the pulsed monostable output current.

For the correct motor speed, the reference current matches the mean value of the pulsed monostable current. In this condition the charge of the feedback capacitor becomes constant.

Fig. 2 - Block diagram



S-9524

The speed n of a k pole motor results:

$$n = \frac{10{,}435}{C_T\ K\ R_P}$$

and becomes independent of the resistor RT which only determines the current level and the duty cycle which should be 1 : 1 at the nominal speed for minimum torque ripple.

The second fast loop consists of a voltage to current converter which is driven at pin 8 by the low pass filter R_L, C_L. The output current at this stage is injected by a PNP current mirror into the inner resistor R_B. So the driving voltage of the output stage consists of the integrator output voltage plus the fast loop voltage contribution across R_B.

The power output stage realizes different modes depending on the logic status at pin 18 and 19.

- Normal operation for left and right mode: each upper TR of the bridge is used as voltage follower whereas the lower acts as a switch.
- Stop mode where the upper half is open and the lower is conductive.
- High impedance status where all power elements are switched-off.

The high impedance status is also generated when the supply voltage overcomes the 5V to 20V operating range or when the chip temperature exceeds 150°C.

A short circuit protection limits the output current at 1.5A. Integrated diodes clamp spikes from the inductive load both at V_{CC} and ground.

The reference voltages are derived from a common bandgap reference. All blocks are widely supplied by an internal 3.5V regulator which provides a maximum supply voltage rejection.

PIN FUNCTION AND APPLICATION INFORMATION

Pin 1

Trigger input. Receives a proper voltage which contains the information of the motor speed. The waveform can be derived directly by the motor current (Fig. 3). The external resistor generates a proper voltage drop. Together with the input resistance at pin 1 [R_{IN} (1) = 500Ω] the external capacitor C_D realize a high pass filter which differentiates the commutation spikes of the motor current. The trigger level is 0V.

The biasing of the pin 1 is 20mV with a hysteresis of 10mV. So the sensing resistance must be chosen high enough in order to obtain a negative spike of the least 30mV on pin 1, also with minimum variation of motor current:

$$R_S \geqslant \frac{30mV}{\Delta I_{MOT}\ min.}$$

Such value can be too much high for the preregulation stage V-I and it could be necessary to split them into 2 series resistors $R_S = R_{S1} + R_{S2}$ (see fig. 4) as explained on pin 8 section.

Fig. 3

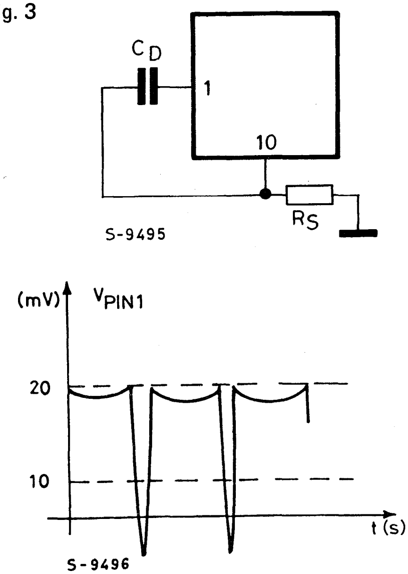
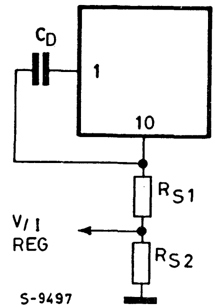


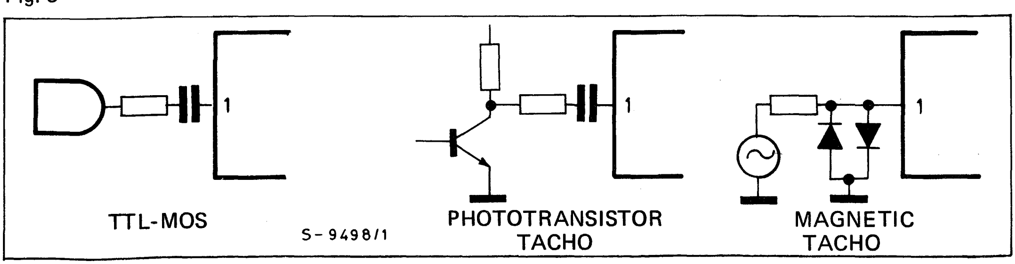
Fig. 4



The information can be taken also from an external tachogenerator. Fig. 5 shows various sources connections:

the input signal mustn't be lower than -0.7V.

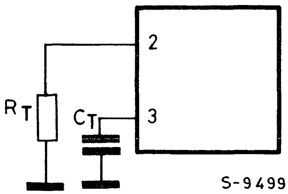
Fig. 5



Pin 2

Timing resistor. An internal reference voltage ($V2 = 0.8V$) gives possibility to fix by an external resistor (R_T), from this pin and ground, the output current amplitude of the monostable circuit, which will be reflected into the timing capacitor (pin 3); the typical value would be about 50μA.

Fig. 6



Pin 3

Timing capacitor. A constant current, determined by the pin 2 resistor, flowing into a capacitor between pin 3 and ground provides the output pulse width of the monostable circuit, the max voltage at pin 3 is fixed by an internal threshold: after reaching this value the capacitor is rapidly discharged and the pulse width is fixed to the value:

$$T_{on} = 2.88\ R_T\ C_T \quad \text{(Fig. 6)}$$

Pin 4

Not connected.

Pin 5

Ground. Connected with pins 6, 15, 16.

Pin 6

Ground. Connected with pins 5, 15, 16.

Pin 7

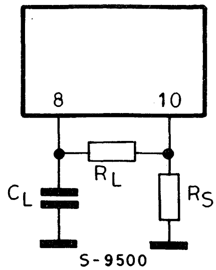
Not connected.

Pin 8

Input V/I loop. Receives from pin 10, through a low pass filter, the voltage with the information of the current flowing into the motor and produces a negative resistance output:

$$R_{out} = -9\ R_S \quad \text{(Fig. 7)}$$

Fig. 7



For compensating the motor resistance and avoiding instability:

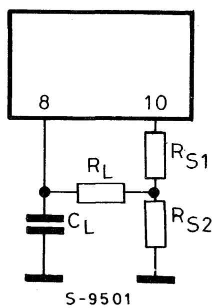
$$R_S \leqslant \frac{R_{MOTOR}}{9}$$

The optimization of the resistor R_S for the tachometric control must not give a voltage too high for the V/I stage: one solution can be to divide in two parts, as shown in Fig. 8, with:

$$R_{S2} = \frac{R_M}{10} \text{ and } R_{S1} + R_{S2} \geqslant$$

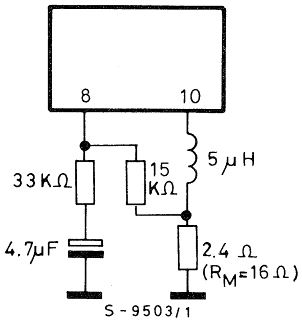
$$\geqslant \frac{30mV}{\Delta\ I\ mot\ min} \quad \text{(see pin 1 sect.)}$$

Fig. 8



The low pass filter R_L, C_L must be calculated in order to reduce the ripple of the motor commutation at least 20dB. Another example of possible pins 10-8 connections is showed on Fig. 9. A choke can be used in order to reduce the radiation.

Fig. 9



Pin 9

Output motor left. The four power transistors are realized as darlington structures. The arrangement is controlled by the logic status at pins 18 and 19.

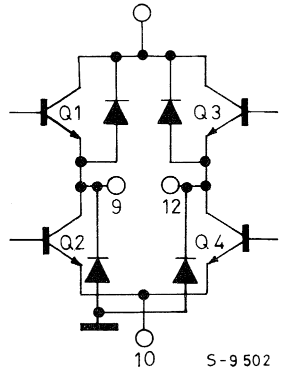
As before explained (see block description), in the normal left or right mode one of the lower darlington becomes saturated whereas the other remains open. The upper half of the bridge operates in the linear mode.

In stop condition both upper bridge darlingtons are off and both lower are on. In the high output impedance state the bridge is switched completely off.

Connecting the motor between pins 9 and 12 both left or right rotation can be obtained. If only one rotation sense is used the motor can be connected at only one output, by using only the upper bridge half. Two motors can be connected each at the each output: in such case they will work alternatively (See Application Section).

The internal diodes, together with the collector substrate diodes, protect the output from inductive voltage spikes during the transition phase (Fig. 10)

Fig. 10



Pin 10

Common sense output. From this pin the output current of the bridge configuration (motor current) is fed into R_S external resistor in order to generate a proper voltage drop.

The drop is supplied into pin 1 for tachometric control and into pin 8 for V/I control (See pin 1 and pin 8 sections).

Pin 11

Supply voltage.

Pin 12

Output motor right. (See pin 9 section)

Pin 13

Output main amplifier. The voltage on this pin results from the tachometric speed control and feeds the output stage.

The value of the capacitor C_F (Fig. 11), connected from pins 13 and 14, must be chosen low enough in order to obtain a short reaction time of the tachometric loop, and high enough in order to reduce the output ripple.

A compromise is reached when the ripple voltage (peak-to-peak) V_{ROP} is equal to 0.1 V_{MOTOR}:

$$C_F = 2.3 \frac{C_T}{V_{RIP}} \left(1 - \frac{R_T}{R_P}\right)$$

with $V_{RIP} = \dfrac{V_{FEM} + I_{MOT} \cdot R_{MOT}}{10}$ and with duty cycle = 50%. (See pin 2-3 section)

Fig. 11

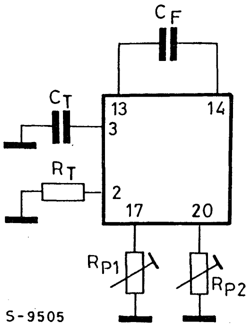
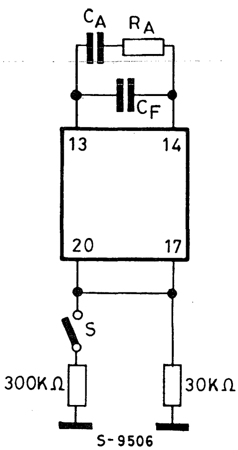


Fig. 12



In order to compensate the behaviour of the whole system regulator-motor-load (considering axis friction, load torque, inertias moment of the motor of the load. etc.) a RC series network is also connected between pins 13 and 14 (Fig. 12). The value of C_A and R_A must been chosen experimentally as follows:

– Increase of 10% the speed with respect to the nominal value by connecting in parallel to R_P a resistor with value about 10 time larger.

– Vary the R_A and C_A values in order to obtain at pin 13 a voltage signal with short response time and without oscillations. Fig. 13 shows the step response at pin 13 versus R_A and C_A values.

Fig. 13

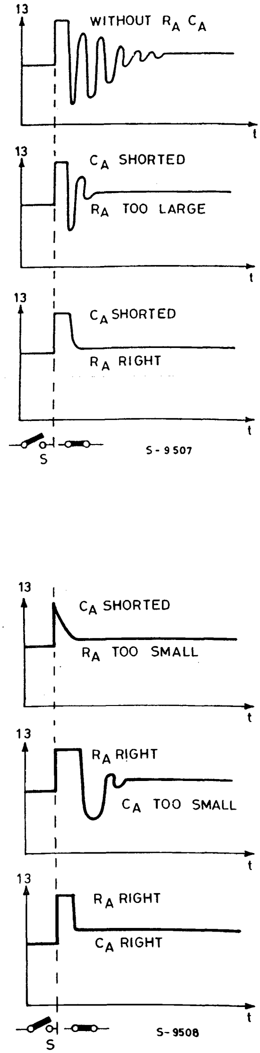


Fig. 14

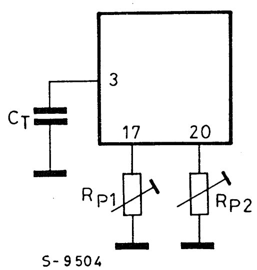
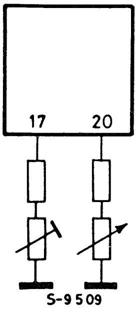


Fig. 15



Pin 14

Inverting input of main amplifier. In this pin the current reference programmed at pins 20, 17 is compared with the current from the monostable (stream of rectangular pulses).

In steady-state condition (constant motor speed) the values are equal and the capacitor C_F voltage is constant.

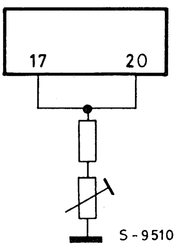
This means for the speed n (min -1) :

$$n = \frac{10.435}{C_T \;\; k \;\; R_P}$$

where "k" is the number of collector segments. (poles)

The non inverting input of the main amplifier is internally connected to a reference voltage (2.3V).

Fig. 16



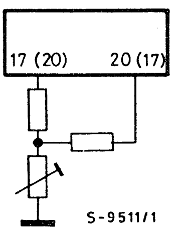
Pin 15

Ground.

Pin 16

Ground.

Fig. 17



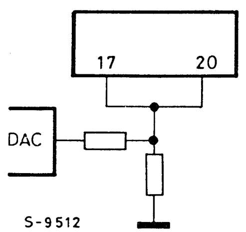
Pin 17

Left speed adjustment. The voltage at this pin is fixed to a reference value of 0.8V. A resistor from this pin and ground (Fig. 14) fixes the reference current which will be compared with the medium output current of the monostable in order to fix the speed of the motor at the programmed value. The correct value of R_P would be:

$$R_P = \frac{10.435}{C_T \cdot k \cdot n} =$$

n = motor speed, (min -1)
k = poles number

Fig. 18

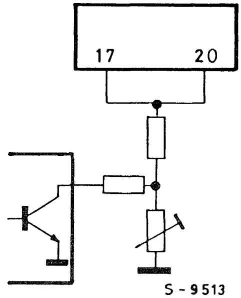


The control of speed can be done in different way:

- speed separately programmed in two senses of rotation (Figg. 14-15);
- only one speed for the two senses of rotation (Fig. 16);
- speeds of the two senses a bit different (i.e. for compensating different pulley effects) (Fig. 17);
- speed programmed with a DC voltage (Fig. 18) i.e. with DA converter;
- fast forward, by putting a resistor. In this case it is necessary that also at the higher speed for the duty cycle to be significatively less than 1 (see value of R_T, C_T on pin 2, pin 3 sections).

Fig. 19 shows the function controlled with a μP.

Fig. 19



Pin 18

Right function control. The voltages applied to this pin and to pin 19 determine the function, as showed in the table.

The typical value of the threshold (L-H) is 1.2V.

CONDITION		OUTPUT FUNCTION	OUTPUT VOLTAGE	
Pin 18	Pin 19		Pin 12	Pin 9
L	L	STOP	LOW	LOW
H	L	LEFT	LOW	REG
L	H	RIGHT	REG	LOW
H	H	OPEN	HIGH IMPEDANCE	

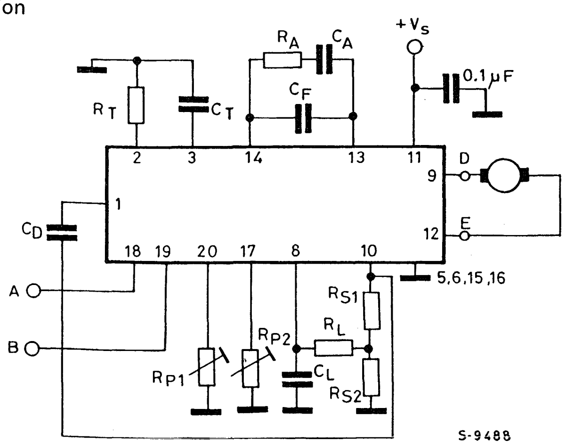
Pin 19

Left function control. (See pin 18 sect).

Pin 20

Right speed adjustment. (See pin 17 sect).

Fig. 20 - Typical application



SGS-THOMSON MICROELECTRONICS

Fig. 21 - Tacho only speed regulation

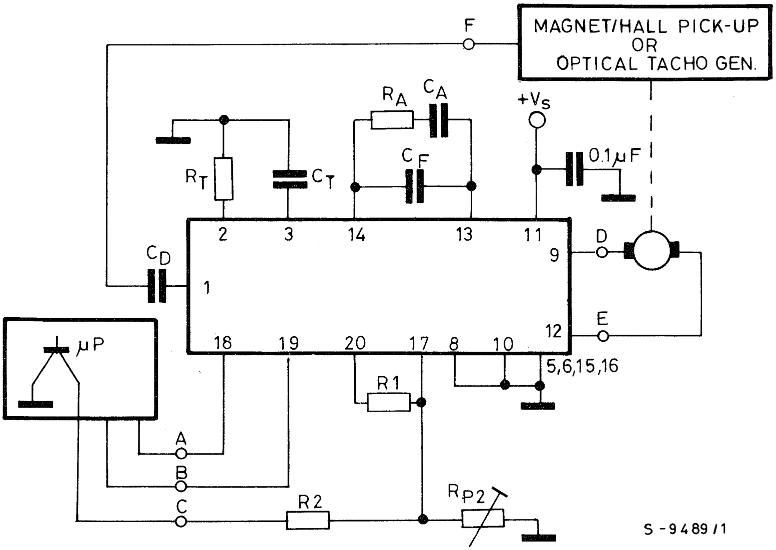


Fig. 22 - One direction reg. of one motor, or alternatively of two motors

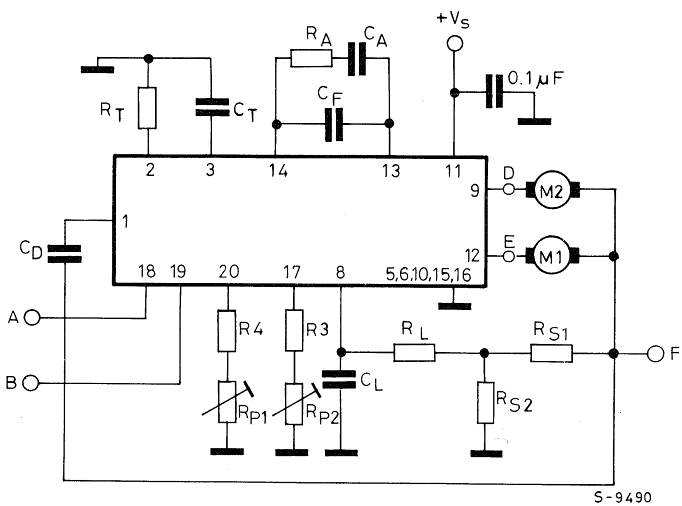
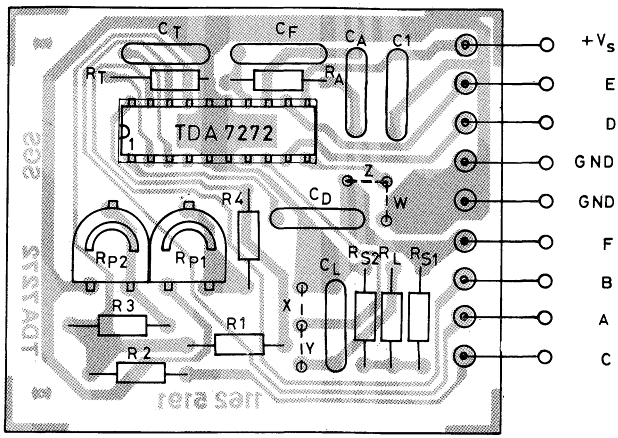


Fig. 23 - P.C. board and components layout of the circuits of Figg. 20, 21, 22



CS-0246

APPLICATION SUGGESTION (Fig. 20, 21, 22) - (For a 2000 r.p.m. 3 pole DC motor with $R_M = 16\Omega$)

Comp.	Recommended value	Purpose	If larger	If smaller	Allowed range	
					Min.	Max.
R_{S1}	1Ω	Current sensing tacho loop.		Tacho loop do not regulate.	0	
R_{S2}	1.5Ω	Curr. sensing V/I loop.	Instability may occur.	Motor regulator; undercompens.	0	$R_{MOT}/9$
R_L; C_L	22KΩ - 68nF	Spike filtering.	Slow V/I regulator response.	High output ripple.		
C_D	68nF	Pulse transf.			33nF	100nF
R_T; C_T	15KΩ - 47nF	Current source programming to obtain a 50% duty cycle.			6KΩ	30KΩ
R_{P1}; R_{P2}	47KΩ trim.	Set of speed.	Low speed.	High speed.	0	
C_F	Polyester 100nF	Optimization of integrator ripple and loop response time.	Lower ripple, slower tacho-regulator response.	Higher ripple, faster response.	10nF	470nF
R_A; C_A	220KΩ - 220nF	Fast response with no overshoot.	Depending on electromechanical system.		10KΩ 10nF	10MΩ 1μF

Fig. 24 - Speed regulation versus supply voltage (Circuit of Fig. 20)

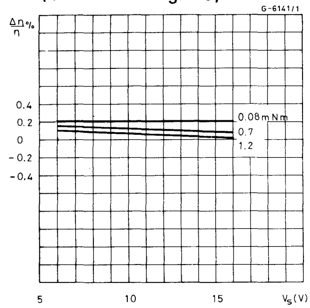
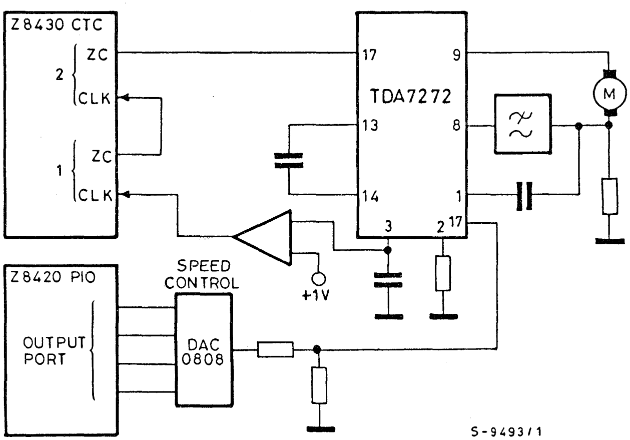


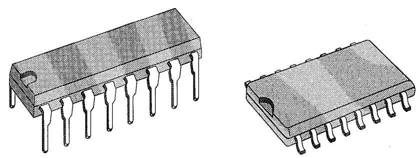
Fig. 25 - In connection with a presettable counter and I/O peripheral the TDA7272 controls the speed through a D/A converter



SINGLE CHIP STEREO CASSETTE PLAYBACK SYSTEM

ADVANCE DATA

- WIDE OPERATING SUPPLY VOLTAGE (1.8V to 7V)
- INPUT COUPLING WITHOUT CAPACITORS
- BUILT-IN DC STEREO VOLUME CONTROL
- BUILT-IN RIPPLE FILTERS
- LOW QUIESCENT CURRENT
- NO EXTERNAL BOUCHEROT CELL
- MAX OUTPUT CURRENT 70mA PEAK

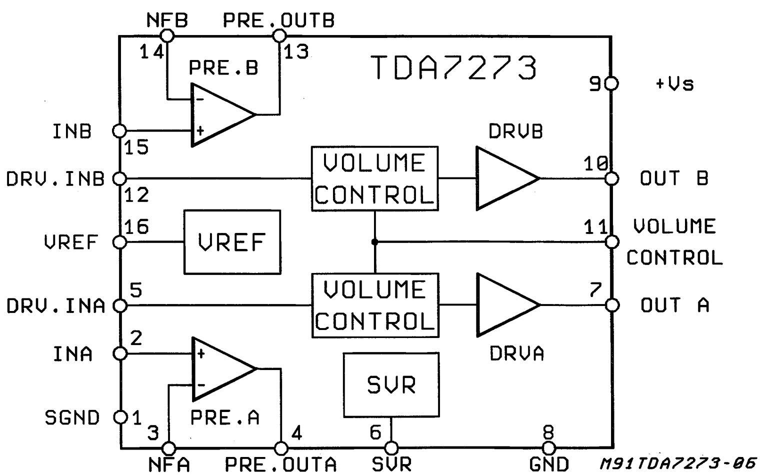


DIP-16	SO-16
ORDERING NUMBERS:	
TDA7273	TDA7273D

DESCRIPTION

The TDA7273 is a monolithic integrated circuit designed for portable cassette players market.
It comprises preamplifiers, DC volume control, and headphone drivers.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Supply Voltage	9	V
I_o	Output Current (max)	70	mA
T_{op}	Operating Temperature Range	-20 to 70	°C
T_{stg}, T_j	Storage & Junction Temperature Range	-40 to +150	°C

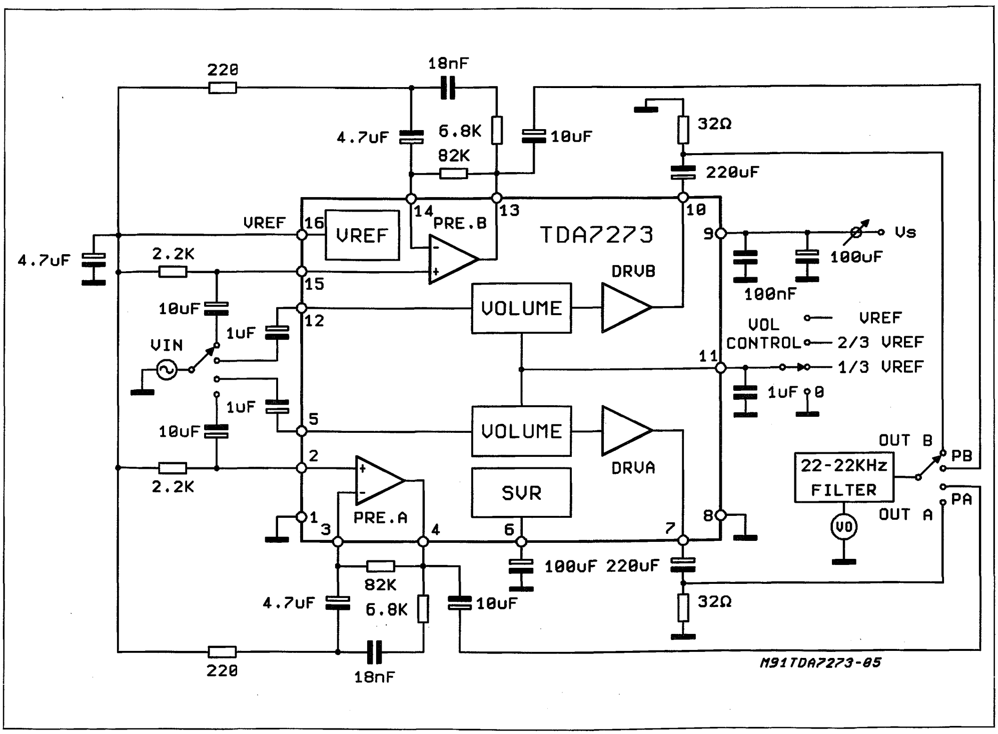
THERMAL DATA

Symbol	Description		DIP-16	SO-16	Unit
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	200	°C/W

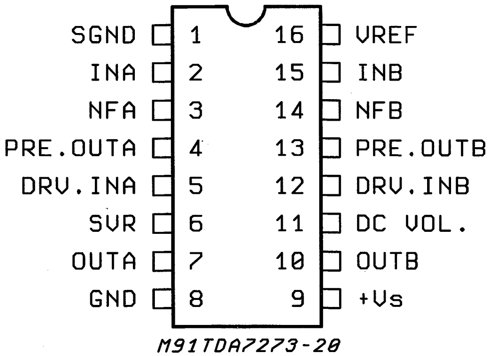
DC CHARACTERISTICS: T_{amb} = 25°C; V_S = 3V; R_L = 10KΩ (Preamplifier), R_L = 32Ω (Headphone); V_{IN} = 0; V_{OL} control = V_{ref}

Terminal No	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Terminal Voltage (V)	0	1.5	1.5	1.5	1.5	2.7	1.5	0	3	1.5	1.5	1.5	1.5	1.5	1.5	1.5

TEST CIRCUIT



PIN CONNECTION (Top view)



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 3V, f = 1KHz, R_L = 32Ω Vol. control = 2/3V_{ref} unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		1.8		7	V
I_d	Quiescent Current			14	20	mA
Vref	Reference Voltage		1.3	1.49	1.7	V

PREAMPLIFIER SECTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{VO}	Open Loop Gain			70		dB
G_V	Close Loop Gain		30	33	35	dB
V_o	Output Voltage	THD = 1%	600	850		mV
I_b	Bias Current			3		µA
THD	Total Harmonic Distortion	V_o = 330mVrms		0.05	0.25	%
C_t	Cross Talk	Rg = 2.2KΩ; V_o = 330mVrms		74		dB
E_N	Output Noise	Rg = 2.2KΩ; BW = 22Hz to 22KHz		100		µV
SVR	Ripple Rejection	R_g = 2.2KΩ V_R = 100mVrms f = 100Hz; C_{SVR} = 100µF	40	50		dB

HEADPHONE DRIVER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{o(DC)}$	DC Output Voltage			1.50		V
P_o	Output Power	THD = 10%;	15	30		mW
P_o	Transient Output Power	THD = 10% RL = 16Ω		50		mW
G_V	Close Loop Gain	P_o = 5mW	28	31	34	dB
THD	Total Harmonic Distortion	P_o = 5mW		0.2	1	%
C_t	Cross Talk	Rg = 10KΩ; P_o = 5mW	40	50		dB
SVR	Ripple Rejection	V_r = 100mVrms, f = 100Hz Vol. control = 1/3V_{ref} C_{SVR} = 100µF; R_g = 600Ω		47		dB
	Volume Control Range		66	75		dB

Figure 1: Application Circuit

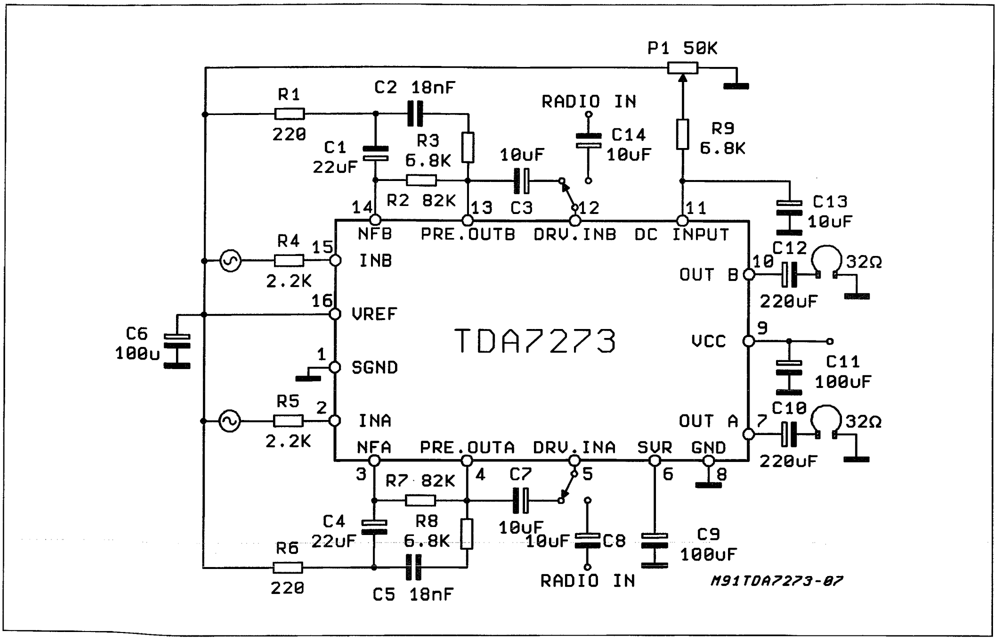
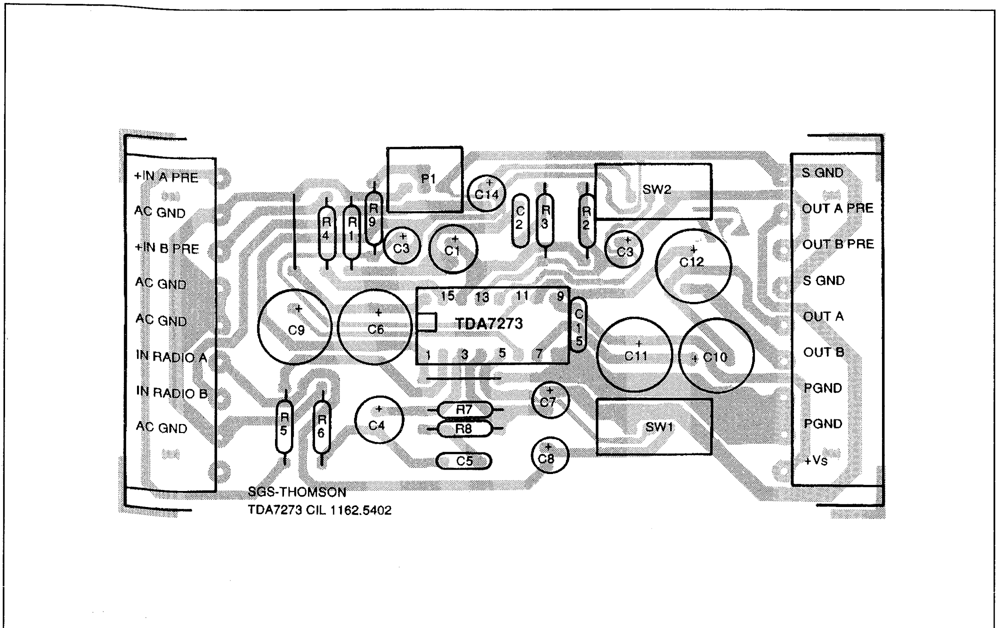


Figure 2: P.C. Board and Component Layout of the Circuit of Figure 1 (1:1 scale)



SGS-THOMSON MICROELECTRONICS

Figure 3: Supply Current vs. Supply Voltage (Preamplifier + Driver)

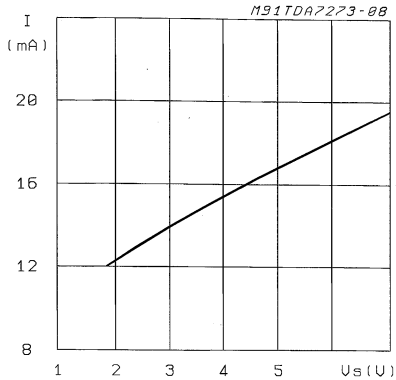


Figure 4: V_{ref}, vs. Supply Voltage (pin 16)

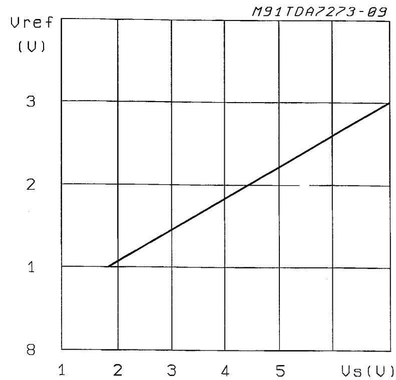


Figure 5: Closed Loop Gain vs. Frequency (V_S = 3V) (PREAMPLIFIER)

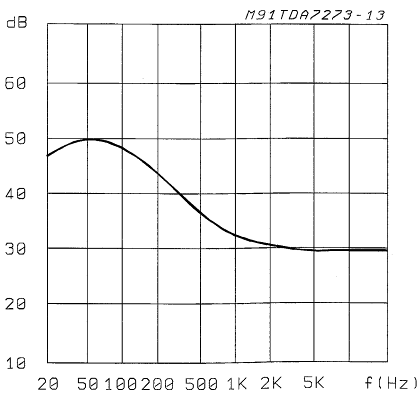


Figure 6: THD vs. Frequency (V_S = 3V, V_o =330mVrms, R_L = 10KΩ) (PREAMPLIFIER)

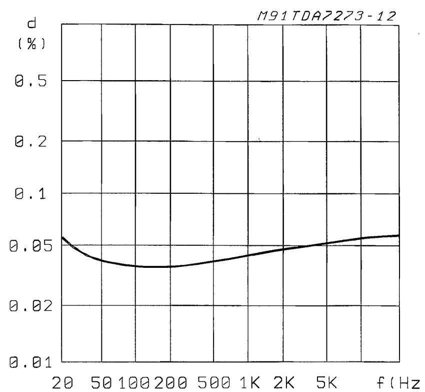


Figure 7: SVR vs. Frequency (PREAMPLIFIER)

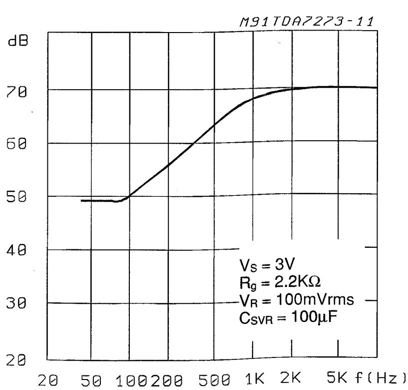


Figure 8: Quiescent Output Voltage vs. Supply Voltage (DRIVER)

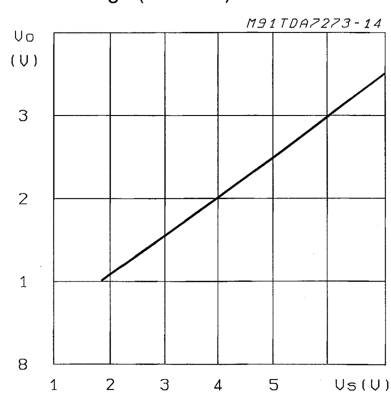


Figure 9: Closed Loop Gain vs Frequency (V_S = 3V, R_L = 32Ω) (DRIVER)

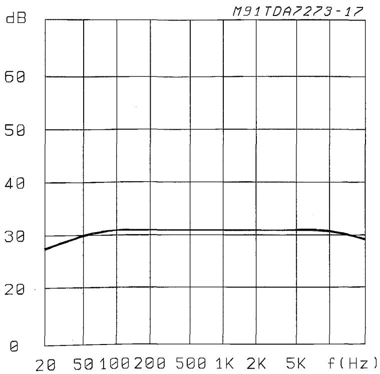


Figure 10: Output Power vs. Supply Voltage (V_{ol} = 2/3V_{ref}, R_L = 32Ω, THD = 10%, f = 1KHz) (DRIVER)

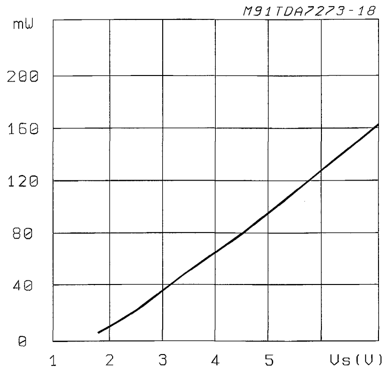


Figure 11: THD vs. Output Power (V_o = 2/3V_{ref}, V_S = 3V, R_L = 32Ω, f = 1KHz) (DRIVER)

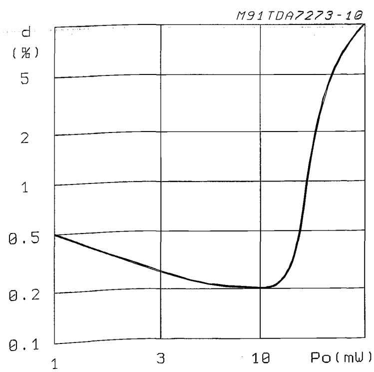


Figure 12: THD vs. Frequency (P_o = 5mW, V_S = 3V R_L = 32Ω) (DRIVER)

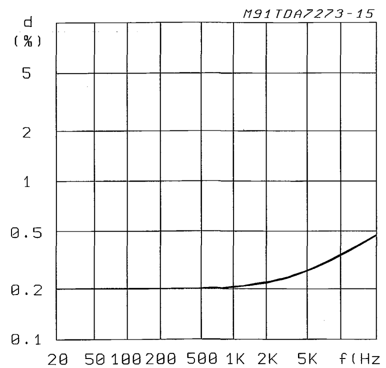


Figure 13: SVR vs. Frequency V_S = 3V (R_L = 32Ω, V_r = 100Vrms R_g = 600Ω, C_{SVR} = 100mV) (DRIVER)

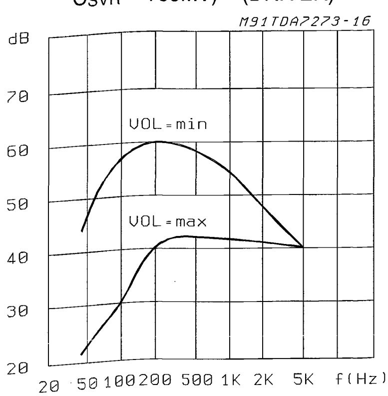
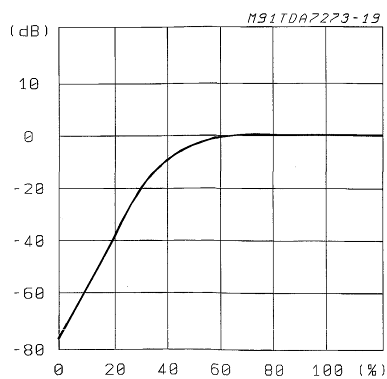


Figure 14: Volume Control (0dB = 10mW, V_S = 3V R_{vol} = 50KΩ, R_L = 32Ω, f = 1KHz) vs. Volume Setting (DRIVER)



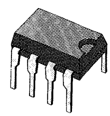
SGS-THOMSON MICROELECTRONICS

TDA7274

LOW-VOLTAGE DC MOTOR SPEED CONTROLLER

- WIDE OPERATING VOLTAGE RANGE (1.8 to 6V)
- BUILT-IN LOW-VOLTAGE REFERENCE (0.2V)
- LINEARITY IN SPEED ADJUSTMENT
- HIGH STABILITY VS. TEMPERATURE
- LOW NUMBER OF EXTERNAL PARTS

The TDA 7274 is a monolithic integrated circuit DC motor speed controller intended for use in microcassettes, radio cassette players and other consumer equipment. It is particulary suitable for low-voltage applications.



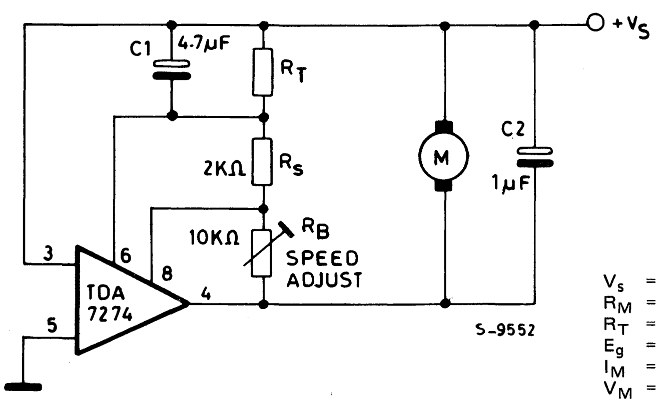
Minidip Plastic

ORDERING NUMBER: TDA 7274

ABSOLUTE MAXIMUM RATINGS

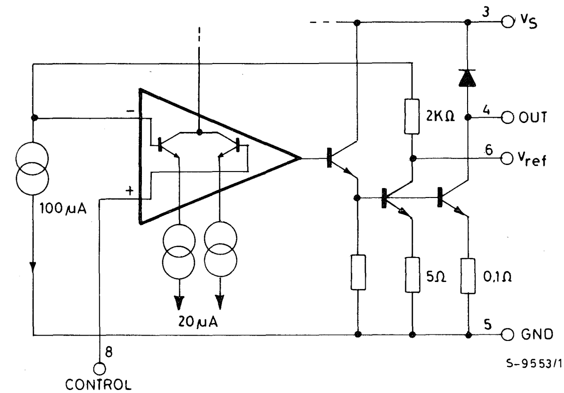
V_s	Supply voltage	6	V
I_M	Motor Current	700	mA
P_{tot}	Power dissipation at $T_{amb} = 25°C$	1.25	W
T_j, T_{stg}	Storage and junction temperature	-40 to +150	°C

APPLICATION CIRCUIT

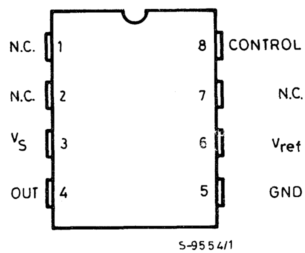


V_s = 3.0V
R_M = 4.9Ω
R_T = 220Ω
E_g = 1.65V
I_M = 100 mA
V_M = $R_M I_M + E_g$ = 2.14V

SCHEMATIC DIAGRAM



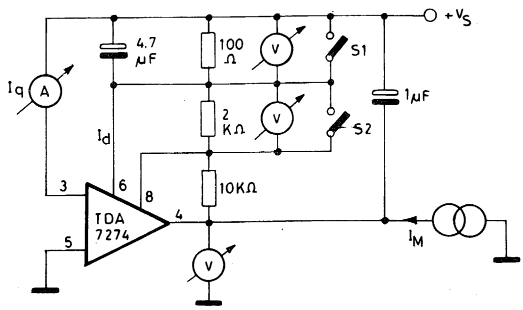
CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

Fig. 1 – Test circuit



ELECTRICAL CHARACTERISTICS (Refer to test circuit, $V_s = 3V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range		1.8		6	V
V_{ref}	Reference voltage	I_M = 100mA	0.18	0.20	0.22	V
I_q	Qiescent current			2.4	6.0	mA
I_d (Pin 6)	Quiescent current			120		µA
K	Shunt ratio	I_M = 100mA	45	50	55	–
V_{sat}	Residual voltage	I_M = 100mA		0.13	0.3	V
$\frac{\Delta V_{ref}}{V_{ref}} / \Delta V_s$	Line regulation	I_M = 100mA V_s = 1.8 to 6V		0.20		%/V
$\frac{\Delta K}{K} / \Delta V_s$	Voltage characteristic of shut ratio	I_M = 100mA V_s = 1.8 to 6V		0.80		%/V
$\frac{\Delta V_{ref}}{V_{ref}} / \Delta I_M$	Load regulation	I_M = 20 to 200mA		0.004		%/mA
$\frac{\Delta K}{K} / \Delta I_M$	Current characteristic of shut ratio	I_M = 20 to 200mA		-0.03		%/mA
$\frac{\Delta V_{ref}}{V_{ref}} / \Delta T_{amb}$	Temperature characteristic of reference voltage	I_M = 100mA T_{amb} = -20 to +60°C		0.04		%/°C
$\frac{\Delta K}{K} / \Delta T_{amb}$	Temperature characteristic of shut ratio	I_M = 100mA T_{amb} = 20 to +60°C		0.02		%/°C

Fig. 2 - Quiescent current vs. supply voltage

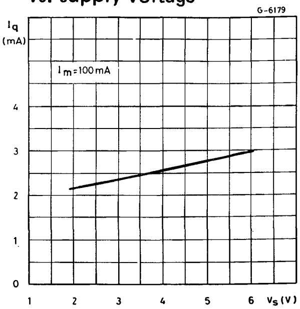


Fig. 3 - Reference voltage vs. supply voltage

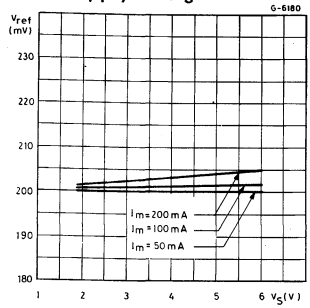


Fig. 4 - Shunt ratio vs. supply voltage

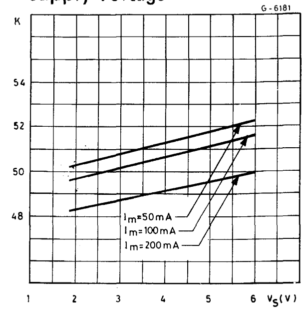


Fig. 5 - Reference voltage vs. load current

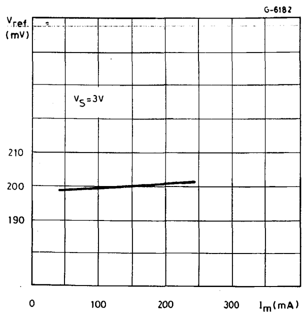


Fig. 6 - Shunt ratio vs. load current

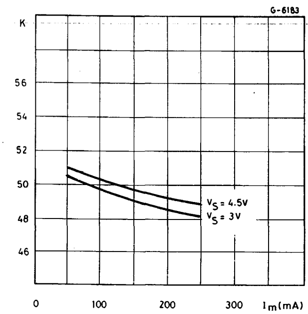


Fig. 7 - Minimum supply voltage (typical) vs. load current

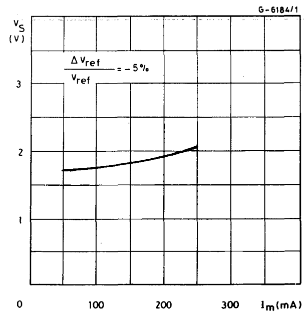


Fig. 8 - Saturation voltage vs. load current

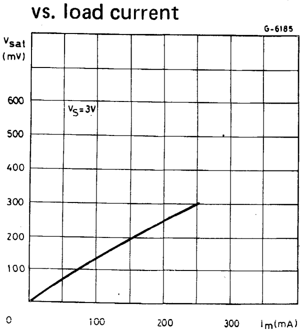


Fig. 9 - Quiescent current vs. ambient temperature

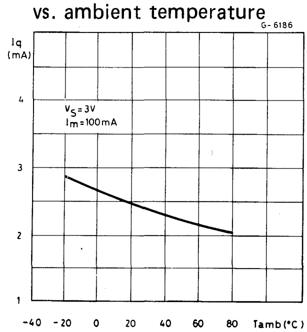


Fig. 10 - Reference voltage vs. ambient temperature

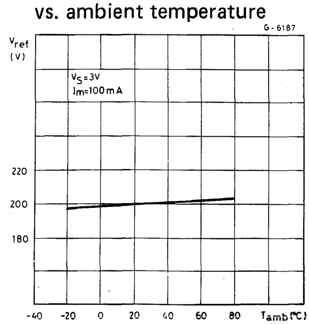
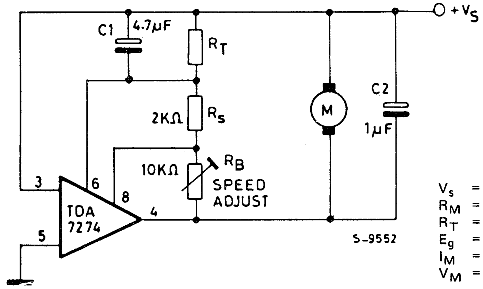


Fig. 11 - Application circuit



V_s = 3.0V
R_M = 4.9Ω
R_T = 220Ω
E_g = 1.65V
I_M = 100 mA
V_M = $R_M I_M + E_g$ = 2.14V

Fig. 12 - P.C. board and components layout of the circuit of fig. 11 (1 : 1 scale)

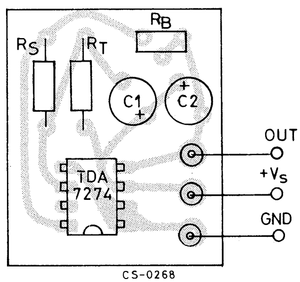


Fig. 13 - Speed variations vs. supply voltage

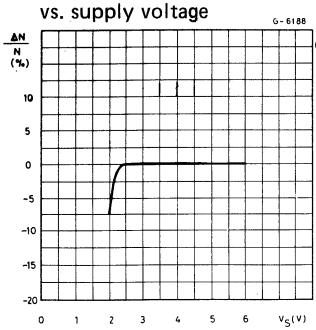


Fig. 14 - Speed variations vs. motor current

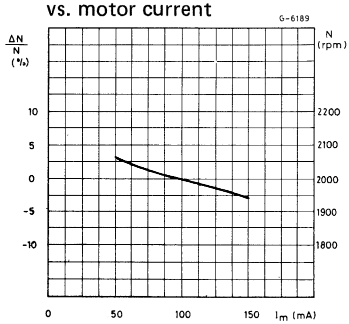
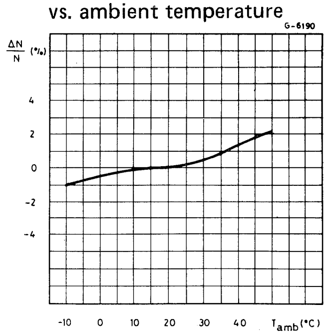
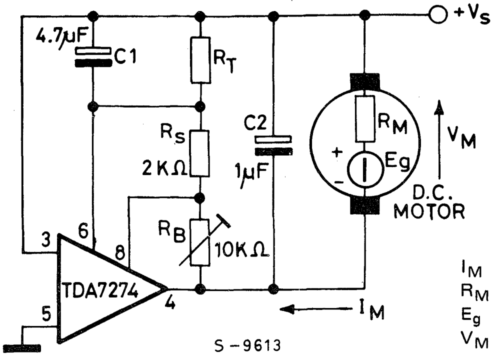


Fig. 15 - Speed variations vs. ambient temperature



APPLICATION INFORMATION

Fig. 16



I_M = Motor current at rated speed
R_M = Motor resistance
E_g = Back electromotive force
$V_M = I_M \cdot R_M + E_g$

$$E_g = R_T\, I_d + I_M \left(\frac{R_T}{K} - R_M\right) + V_{ref}$$

$$\left[1 + \frac{R_B}{R_S} + \frac{R_T}{R_S}\left(1 + \frac{1}{K}\right)\right]$$

R_S has to be adjusted so that the applied voltage V_M is suitable for a given motor, the speed is then linearly adjustable varing R_B.

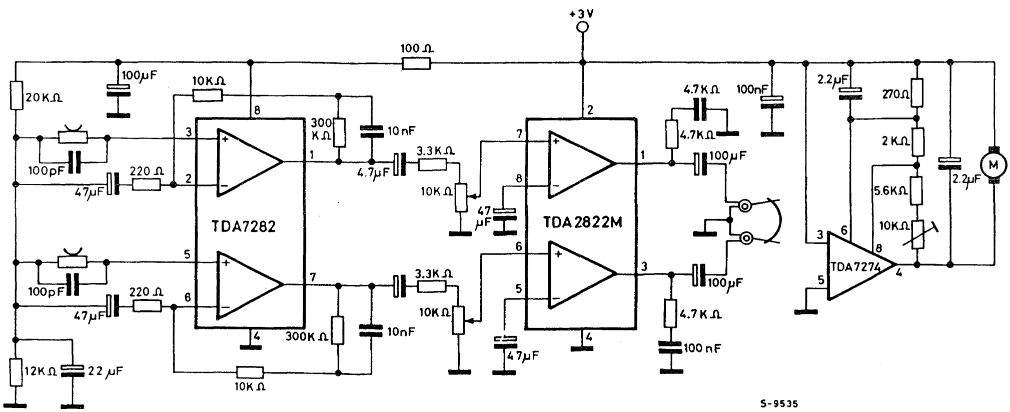
The value of R_T is calculated so that

$$R_{T\,(max.)} < K_{(min.)} \cdot R_{M\,(min.)}$$

If $R_{T\,(max.)} > K \cdot R_M$, instability may occur.

The values of C_1 (4.7 µF typ.) and C_2 (1 µF typ.) depend on the type of motor used. C_1 adjusts WOW and flutter of the system. C_2 suppresses motor spikes.

Fig. 17 - 3V stereo cassette miniplayer with motor speed control



SGS-THOMSON MICROELECTRONICS

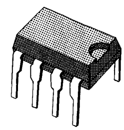
TDA7275A

MOTOR SPEED REGULATOR

ADVANCE DATA

- EXCELLENT VERSATILITY IN USE
- HIGH OUTPUT CURRENT (UP TO 1.5A)
- LOW QUIESCENT CURRENT
- LOW REFERENCE VOLTAGE (1.32V)
- EXCELLENT PARAMETERS STABILITY VERSUS AMBIENT TEMPERATURE
- START/STOP FUNCTION (TTL LEVELS)
- DUMP PROTECTION

The TDA7275A is a linear integrated circuit in minidip plastic package. It is intended for use as speed regulator for DC motors of record players, tape and cassette recorders.
The dump protection make it particularly suitable for car radio applications.



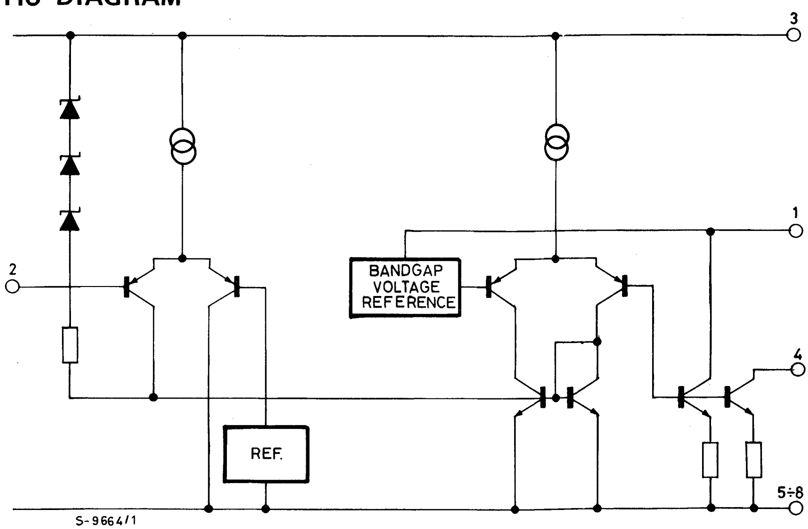
Minidip (4 + 4)

ORDERING NUMBER: TDA7275A

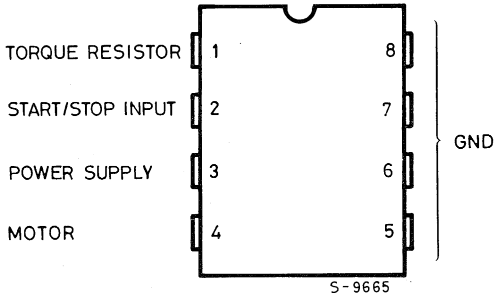
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	19	V
V_s	Peak supply voltage (for 50ms)	45	V
I_M	Maximum output current	1.5	A
T_{op}	Operating temperature range	-30 to 85	°C
P_{tot}	Total power dissipation T_{amb} = 70°C	1	W
	T_{pins} = 70°C	4	W

SCHEMATIC DIAGRAM



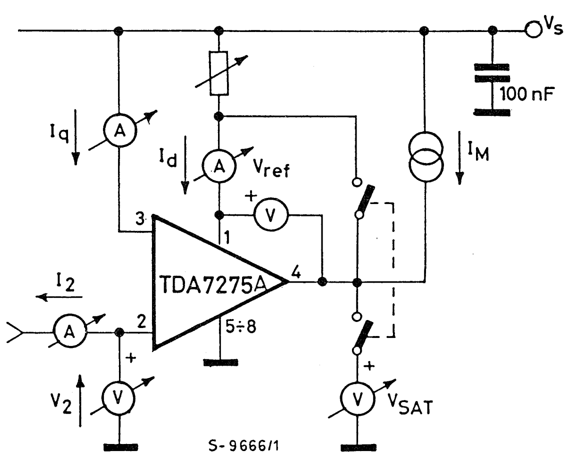
CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	20	°C/W

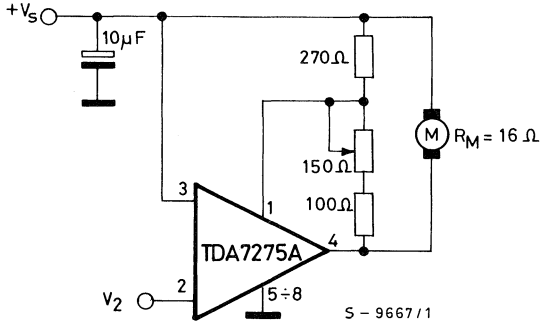
Fig. 1 - Test circuit



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 12V unless otherwise specified, refer to test circuit)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range		8		18	V
V_{ref}	Reference voltage	I_M = 0.1A	1.05	1.22	1.35	V
$I_q + I_d$	Total quiescent current	I_M = 0.1mA		2		mA
I_d	Quiescent current	I_M = 0.1mA		1		mA
I_{ms}	Starting motor current	$\frac{\Delta V_{ref}}{V_{ref}}$ = -50%	1			A
V_4	Saturation voltage	I_M = 0.5A		1.7	2	V
$K = I_M/I_T$	Reflection coefficient	I_M = 0.1A	18	20	22	
$\frac{\Delta K/\Delta V_s}{K}$		I_M = 0.1A V_s = 8V to 16V		0.5		%/V
$\frac{\Delta K/\Delta I_M}{K}$		I_M = 25 to 200mA		-0.05		%/mA
$\frac{\Delta K/\Delta T}{K}$		I_M = 0.1A T_{op} = -30 to 85°C		0.02		%/°C
$\frac{\Delta V_{ref}/\Delta V_s}{V_{ref}}$	Line regulation	V_s = 8V to 16V I_M = 0.1A		0.04		%/V
$\frac{\Delta V_{ref}/\Delta I_M}{V_{ref}}$	Load regulation	I_M = 25 to 200mA		-0.01		%/mA
$\frac{\Delta V_{ref}/\Delta T}{V_{ref}}$	Temperature coefficient	I_M = 0.1A T_{op} = -30 to 85°C		0.02		%/°C
V_2	Motor "Stop" (Acc. Following data or grounded)			1		V
I_2	Motor "Stop"	V_2 = 1V		-0.05		mA
V_2	Motor "Run" (Acc. following data or open			1.5		V
I_2	Motor "Run"	V_2 = 1.5V		-0.1		mA

Fig. 2 - Application circuit



- $R_{Ttyp.} = K_{typ.} \; R_{Mtyp.}$ if $R_T > K_{min} \; R_{Mmin}$ instability may accur.
- A diode across the motor could be necessary with certain kind of motor.

Fig. 3 - Quiescent current vs. supply voltage

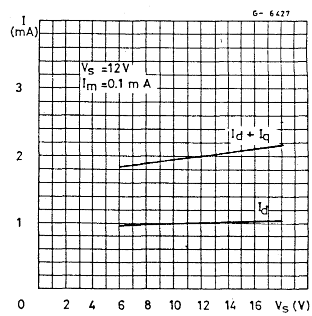


Fig. 4 - Speed variation vs. supply voltage

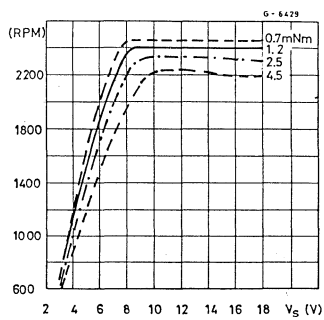
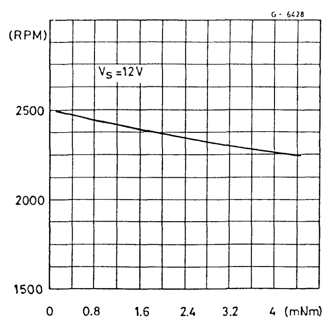


Fig. 5 - Speed variation vs. torque ($V_s = 12V$)

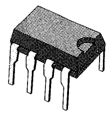


STEREO LOW VOLTAGE CASSETTE PREAMPLIFIER

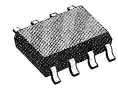
- LOW ON/OFF POP NOISE
- LOW OPERATING VOLTAGE
- VERY LOW DISTORTION

The TDA7282 is a monolithic integrated circuit intended for stereo cassette players.

The TDA7282 is assembled in 8 leads plastic minidip.



Minidip Plastic



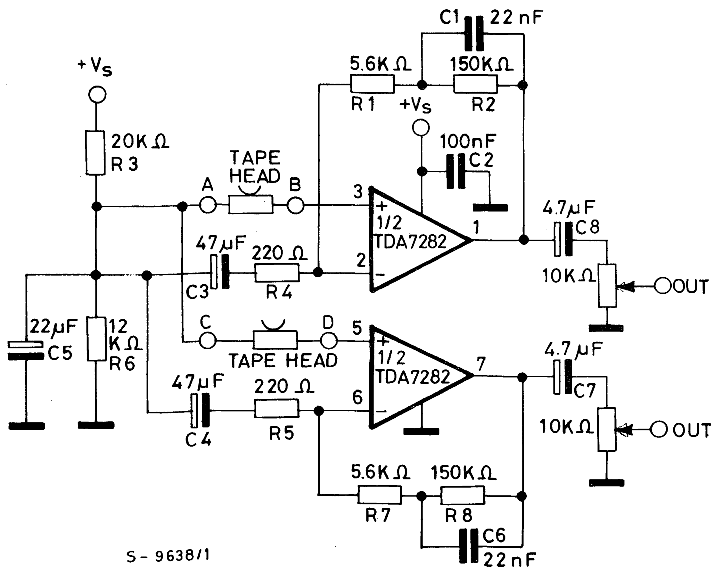
SO-8J

ORDERING NUMBER: TDA7282 (Minidip)
TDA7282D (SO.8)

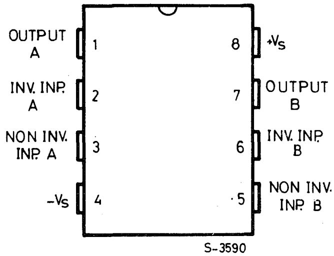
ABSOLUTE MAXIMUM RATINGS

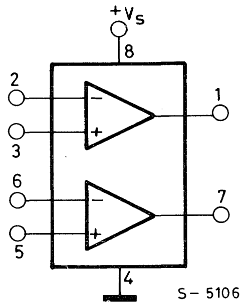
V_s	Supply voltage	10	V
T_{stg}, T_j	Storage and junction temperature	-40 to +150	°C
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	400	mW

STEREO PREAMPLIFIER FOR CASSETTE PLAYERS

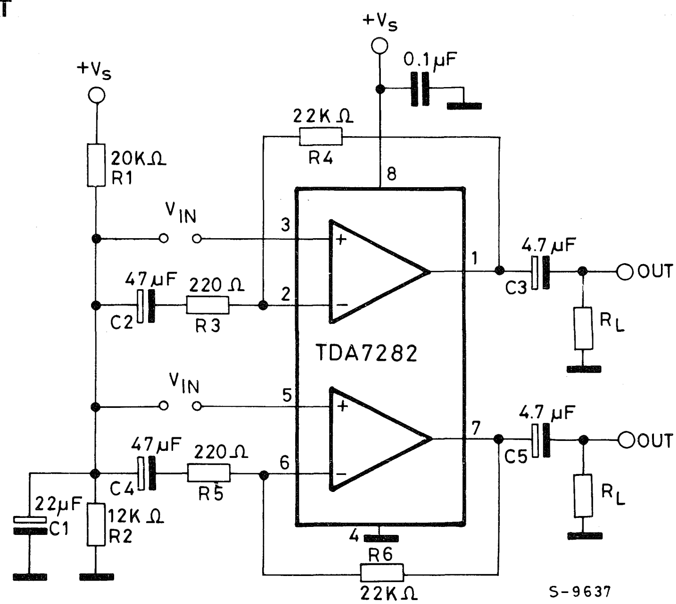


CONNECTION AND BLOCK DIAGRAM





TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 3V, T_{amb} = 25°C, f = 1KHz, G_v = 40dB, R_L = 10KΩ, R_s = 600Ω unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		1.8		9	V
I_d	Supply current			1.5	3	mA
I_b	Input bias current			280	500	nA
I_{os}	Input offset current			20		nA
V_{os}	Input offset voltage			0.5		mV
$V_{o\ DC}$	Quiescent voltage			1.1		V
V_o	Output voltage	THD = 1%	550	650		mV
THD	Total harmonic distortion f = 100Hz f = 1KHz f = 10KHz	V_o = 300mV		 0.08 0.07 0.1	 0.5	 % % %
G_v	Open loop voltage gain	f = 1KHz	68	80		dB
G_v	Closed loop gain			40		dB
	Channel balance			0.5		dB
e_N	Total input noise voltage	B_W = 22KHz to 22KHz		1.5		μV
C_S	Channel separation	f = 1KHz V_o = 30mV		65		dB
SVR	Supply voltage rejection	f = 100Hz	36	45		dB
R_{IN}	Input resistance			100		KΩ
R_o	Output resistance			15		Ω

APPLICATION INFORMATION

Fig. 1 – Stereo preamplifier for cassette players

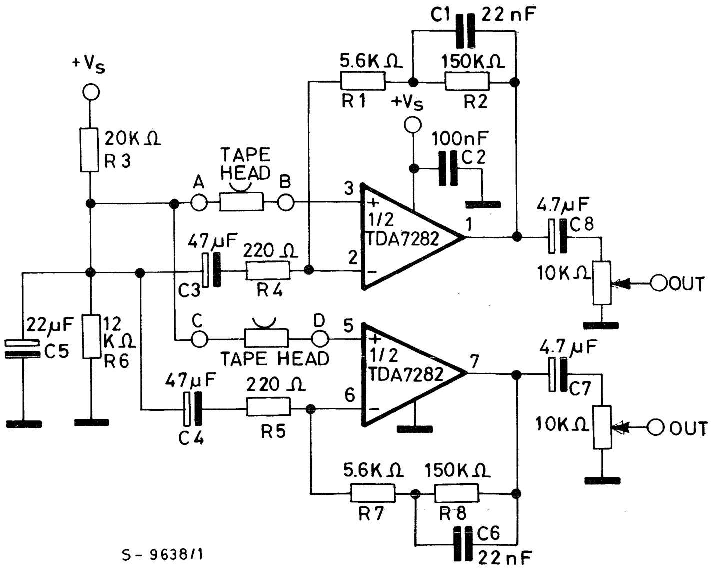
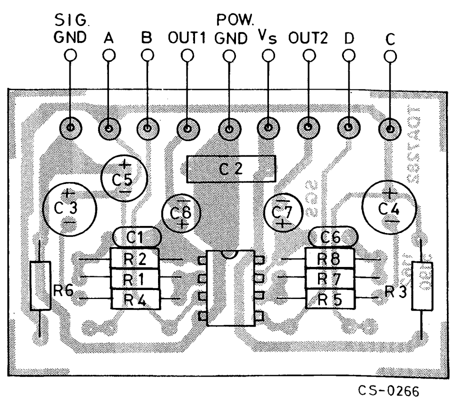


Fig. 2 – P.C and components layout of the circuit of Fig. 1 (1 : 1 scale)



APPLICATION INFORMATION (continued)

Fig. 3 - Quiescent current vs. supply voltage

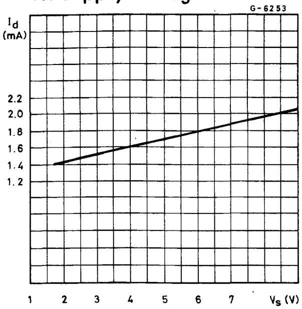


Fig. 4 - DC output voltage vs. supply voltage

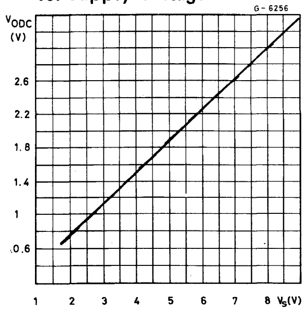


Fig. 5 - Input bias current vs. supply voltage

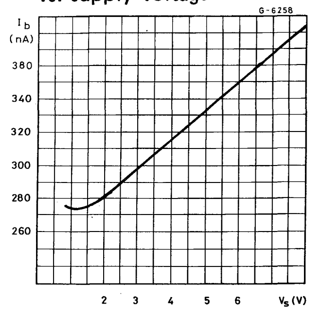


Fig. 6 - Distortion versus output level

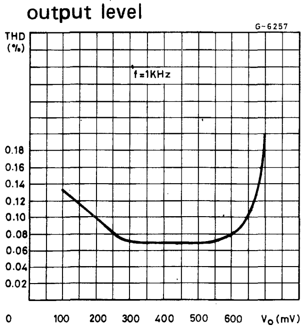


Fig. 7 - Distortion vs. frequency

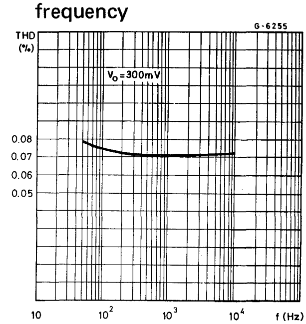


Fig. 8 - NAB response of the circuit of Fig. 1

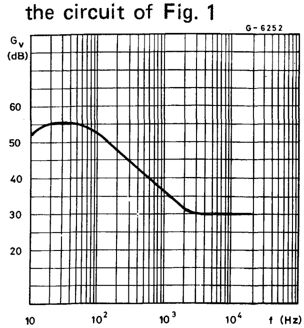


Fig. 9 - Supply voltage rejection vs. frequency

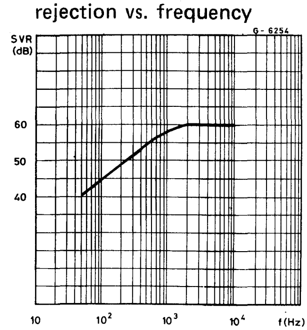
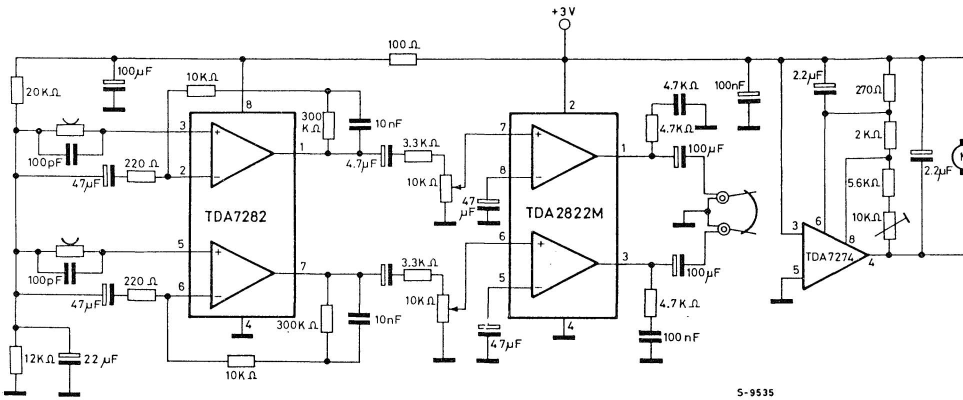


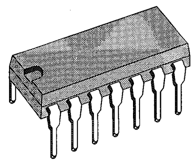
Fig. 10 - Stereo cassette player with motor speed control



RECORD/PLAYBACK CIRCUIT WITH ALC

ADVANCE DATA

- WIDE OPERATING SUPPLY VOLTAGE (3V to 12V)
- VERY LOW INPUT NOISE (V_I = 1.2μV)
- INTERNAL COMPENSATION FOR HIGH GAIN APPLICATION (DOUBLE SPEED RECORDING)
- BUILT-IN ALC CIRCUITRY
- GOOD SVR
- DC CONTROLLED SWITCHES FOR MUTE OR EQUALIZATION SWITCHING FUNCTIONS



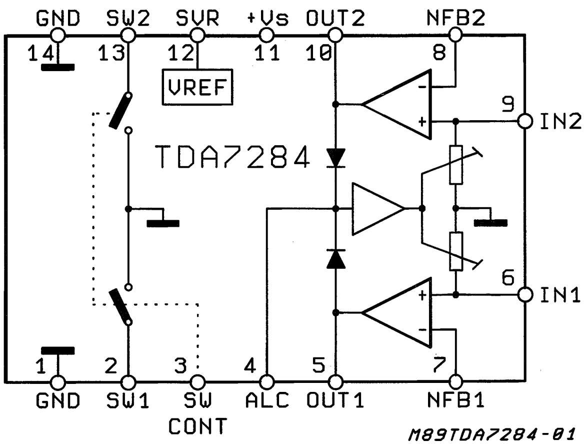
DIP-14

ORDERING NUMBER: TDA7284

DESCRIPTION

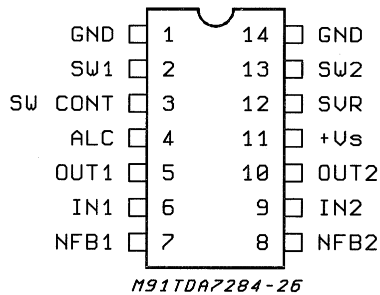
The TDA7284 is a monolithic integrated circuit in a DIP-14 designed for 6V, 9V and 12V AC/DC portable cassette equipment application.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	14	V
T_{OP}	Operating Temperature Range	-20 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature Range	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	120	°C/W

DC CHARACTERISTICS (T_{amb} = 25°; V_S = 6V; V_i = 0V; R_i = 10KΩ; ALC = OFF)

Terminal No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Terminal Voltage (V)	0	0	0	0	2.6	0	1.3	1.3	0	2.6	6	4.6	0	0

Figure 1: Test and Application Circuit

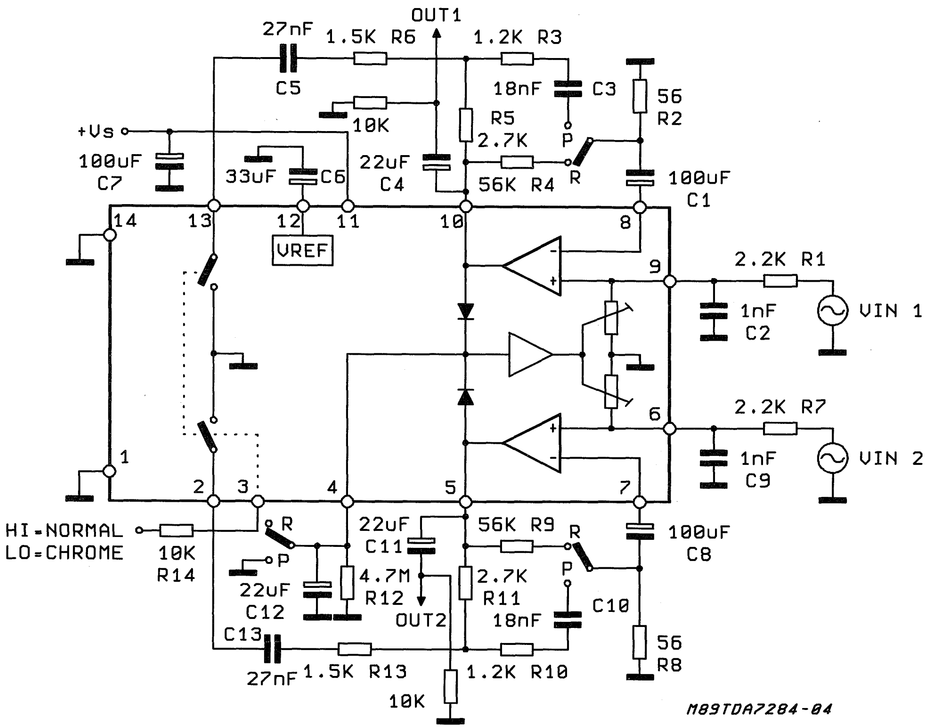
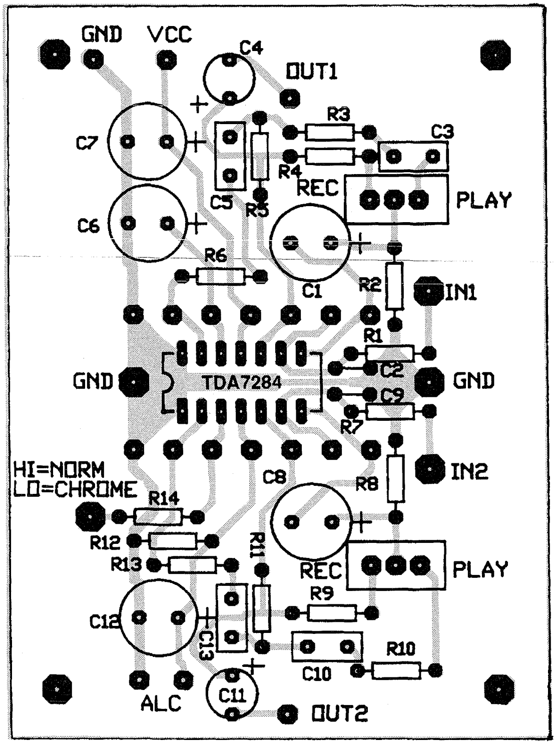


Figure 2: P.C. Board and Component Layout of the Circuit of Fig. 1 (1:1 scale).



SGS-THOMSON MICROELECTRONICS

ELECTRICAL CHARACTERISTICS (V_S = 6V, T_{amb} = 25°C unless otherwise specified refer to test circuit)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_S	Supply Voltage			3		12	V
I_d	Quiescent Current				4.5	8	mA
E_n	Input Noise	R_g = 2.2KΩ BW = 22Hz to 22kHz			1.2		µV
R_I	Input Resistance			30	50	70	KΩ
G_O	Open Loop Gain			65	78		dB
V_O	Output Voltage	THD ≤ 1%	ALC OFF ALC ON	1.2 0.7	1.8 0.9	 1.1	V_{rms} V_{rms}
THD	Total Harmonic Distortion	V_O = 1V_{rms} ALC = ON V_I = 100mV			0.1 0.3	0.5 1	% %
	ALC Range	ΔV_O = 3dB			47		dB
CB	Channel Balance	ALC ON			0	2	dB
SVR	Supply Voltage Rejection	f = 120Hz, C_{SVR} = 33µF V_R = 100mV, R_g = 10KΩ ALC = Off			50		dB
CS	Cross-talk	ALC OFF			70		dB
Pin 3	Turn Off Threshold	I_O = <1µA		0.8	1.3		V
Pin 3	Turn On Threshold				1.7	2.25	V
Pin 3	Turn On Saturation	R_L = 10KΩ			0.1	0.2	V

Figure 3: Drain Current vs. Supply Voltage

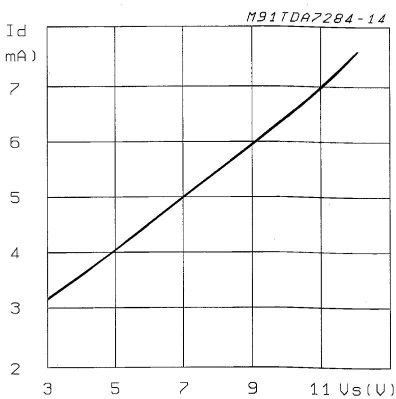


Figure 4: Recording Closed Loop Gain vs. Frequency

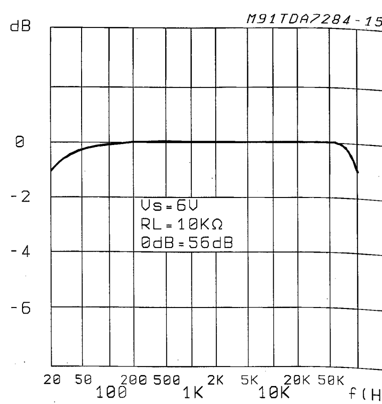


Figure 5: Playback Closed Loop Gain vs Frequency

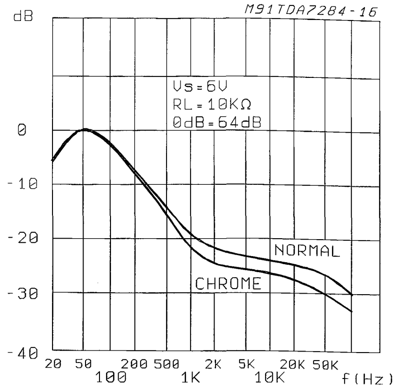


Figure 6: Normalized Output Voltage vs. Supply Voltage

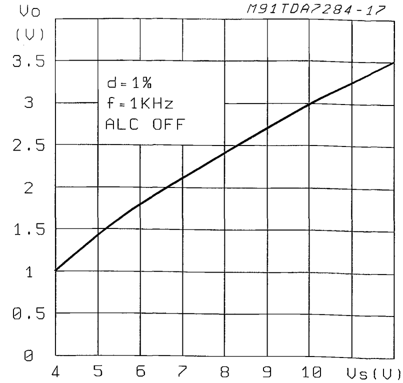


Figure 7: Output Voltage vs. Input Voltage

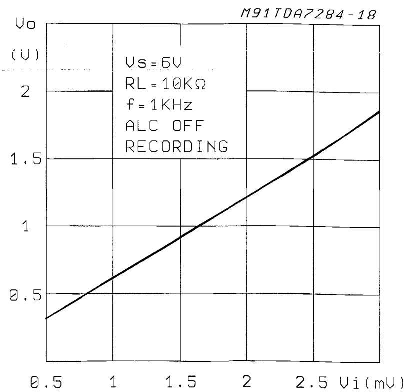


Figure 8: Output Voltage vs. Input Voltage

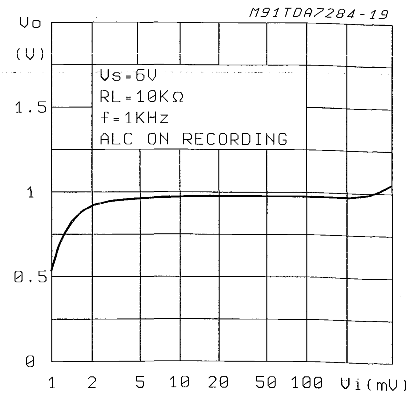


Figure 9: Output Voltage vs. Input Voltage

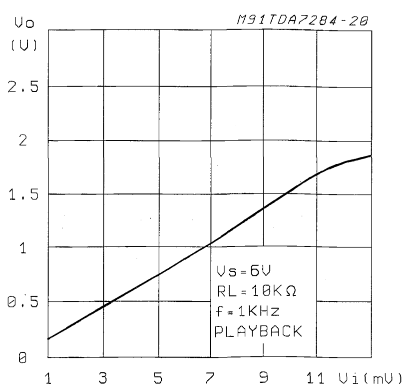


Figure 10: Distortion vs. Input Voltage

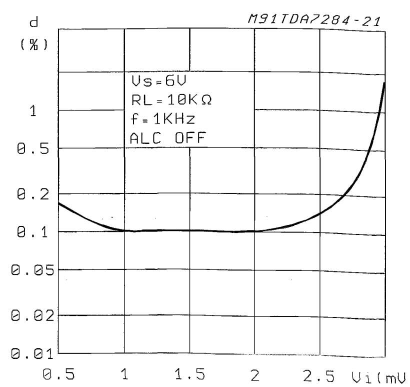


Figure 11: Distortion vs. Input Voltage

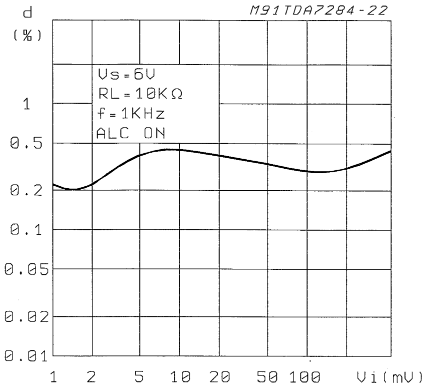


Figure 12: SVR vs. Frequency (ALC = Off)

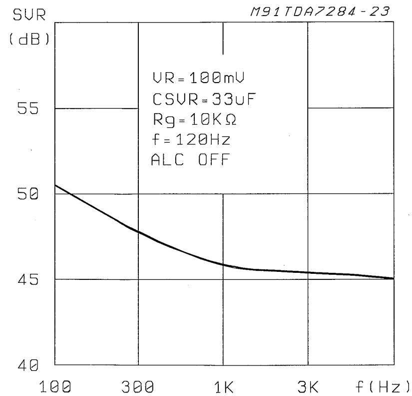


Figure 13: Crosstalk vs. Frequency (ALC = Off)

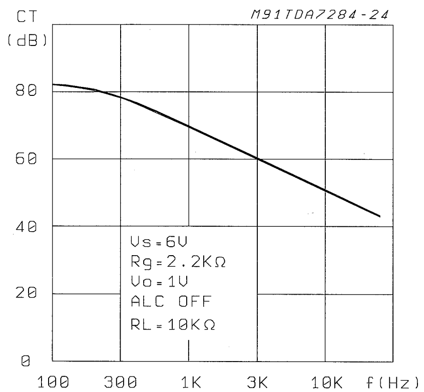
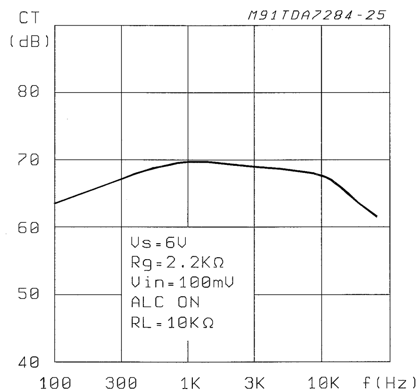


Figure 14: Crosstalk vs. Frequency (ALC = Off)



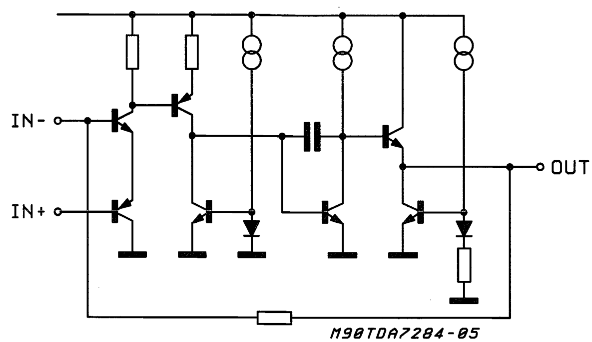
CIRCUIT DESCRIPTION

OPERATIONAL AMPLIFIER

The operational amplifier consists essentially of a very low noise input stage decoupled from the single-ended output stage by means of an emitter follower (fig. 15).

The compensations provided in order to have high gain bandwith product allowing the use for double speed recording application.

Figure 15

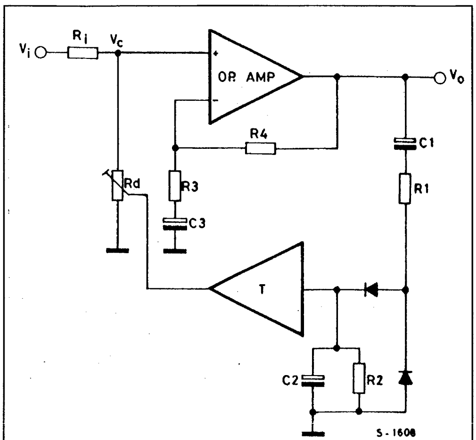


AUTOMATIC LEVEL CONTROL SYSTEM (ALC)

This system maintains the level of the signal to be recorded at a value which prevents saturation of the tape and which optimizes the signal to noise ratio even there are notable variations in the input signal.

Before presenting the ALC circuit of TDA7284 it is worth describing the operation of the automatic level control as a system.A diagram showing the basis of operation is given in fig.16.

Figure 16: Basic Diagram of the ALC stage



This consists of an amplifier (op-amp) having constant gain ($G_V = 1+R4/R3$),which in feedback transforms output signal level information (usually by means of a peak-to-peak detector) into a continuous voltage which drives the networks indicated by T and Rd.

The element T transforms the continuous voltage level into a signal capable of modifying the circuit conditions symbolized by variable resistor Rd.

The value assumed by the resistor Rd is a function of the output signal level Vo and is such that the voltage Vc at the input of the op-amp is constant,even variations of Vi are present.Obviously if Vo is less than a certain value the system is not controlled.

In this case :

$$V_I = V_C = V_O / G_V$$

(G_V is the gain of the op-amp)

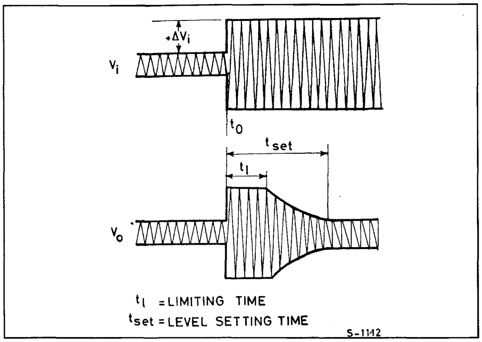
For the TDA7284 the value of V_o below which the system is not controlled is around 1 Vrms.

Let us now consider the speed of response of the system (when controlled) to positive and negative changes of the input signal i.e. the limiting time,the time for return to nominal level (1 Vrms) and the recovery time.

Limiting time, and time for return to nominal level.

Let us suppose that at certain moment T_o, the input signal increases by $+\Delta Vi$ as shown in fig. 17.

Figure 17: Limiting and Level Setting Time



Usually such an increase drives the op-amp into saturation and the time for which it remains in this condition is called the limiting time(T1).

T1 depends on the relationship between the external capacitances, the time constant T=R1 • C1, the supply voltage and the signal variation.

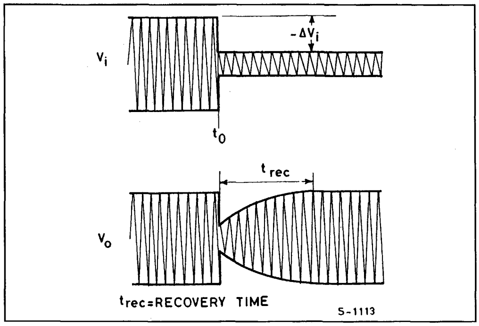
The criteria for choosing the length of T1 are the result of several compromises. In particular if T1 is too long, there will be audible distortion during playback (during T1 the output is a square wave),and if it is too short, the sensation of increased level will be lost while dynamic compression phenomena and instability may occur.

The time for return to nominal level is defined as the total time between the instant To and the instant in which the output reassumes the nominal value. This time (Ts) is roughly equal to 5 • T1.

On the basis of tests carried out it has been found that a musical signal with high dynamic range (ΔVl =+40 dB) is to be recorded, the best value of Ts is between 200 and 300ms.

Recovery time.
let us now suppose that at the instant To the input signal decreases of ΔVi (fig. 18).

Figure 18: Recovery Time



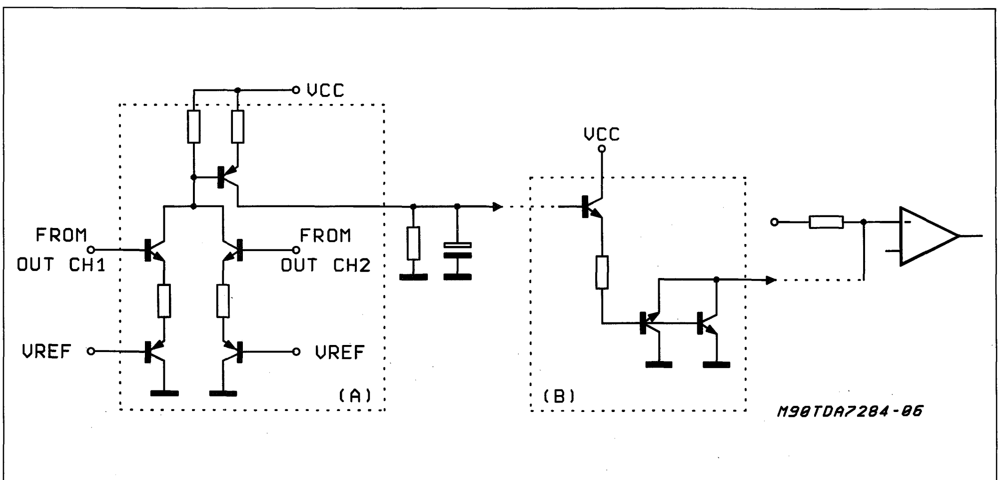
The recovery time (Trec) is defined as the time between the instant To and the instant in which the output signal returns to the nominal level.

This time depends essentially on the discharge time constant of R2 • C2 (see fig. 16) and on the size of the step -ΔVi. In this case too, if this time is too long the signal to noise ratio on the tape deriorates.

If it is too short the sensation of the low signal level is lost during playback.

The ALC system of the TDA7284
Fig. 16 becomes the following (fig. 19) where the

Figure 19



peak-to-peak detector of fig. 16 is now inside the broken line 1 while the system which allows a dinamic resistance varying with the DC voltage level (i.e. inversely proportional to the op-amp output signal),is inside the broken line 2.

It should be noted that the generator resistance Ri has no influence on the controlled voltage value Vc, although its value should be between 1 and 47 Kohm.

The lower limit is determined by the minimum dynamic resistance of 10 ohm and therefore to have a control range of 40 dB for the input signal, Ri must be greather than 1.5 Kohm.

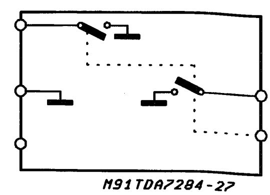
The upper limit results from the necessity to limit the attenuation of the signal by the input impedance of the op-amp.

Switches

Two DC-controlled switches are also included in the chip (fig. 20)

Fig. 19 shows the typical application circuit of the TDA7284 utilizing the equalization switch for normal or chrome tape playback equalization.The advantage is the components can be placed near

Figure 20



to the IC, while the tape selector switch can be at a remote location, hence reduce the chances of noise and oscillation due to components layout. Another advantage is that only one pole is needed for the tape selector switch as compared to the two poles needed by conventional circuits (one separate pole for each channel).

Fig. 22 shows the use of the switches to obtain the mute function.

Figure 21: Application Circuit with DC Switching of Normal/Chrome Tape Equalization

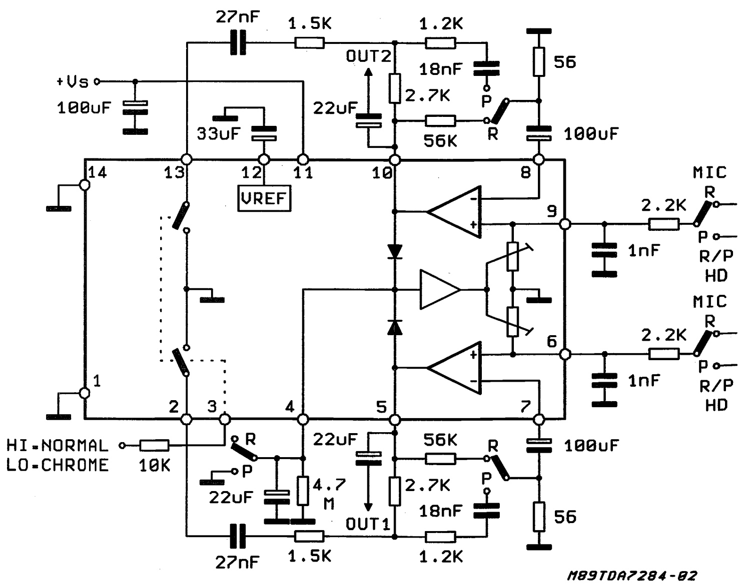
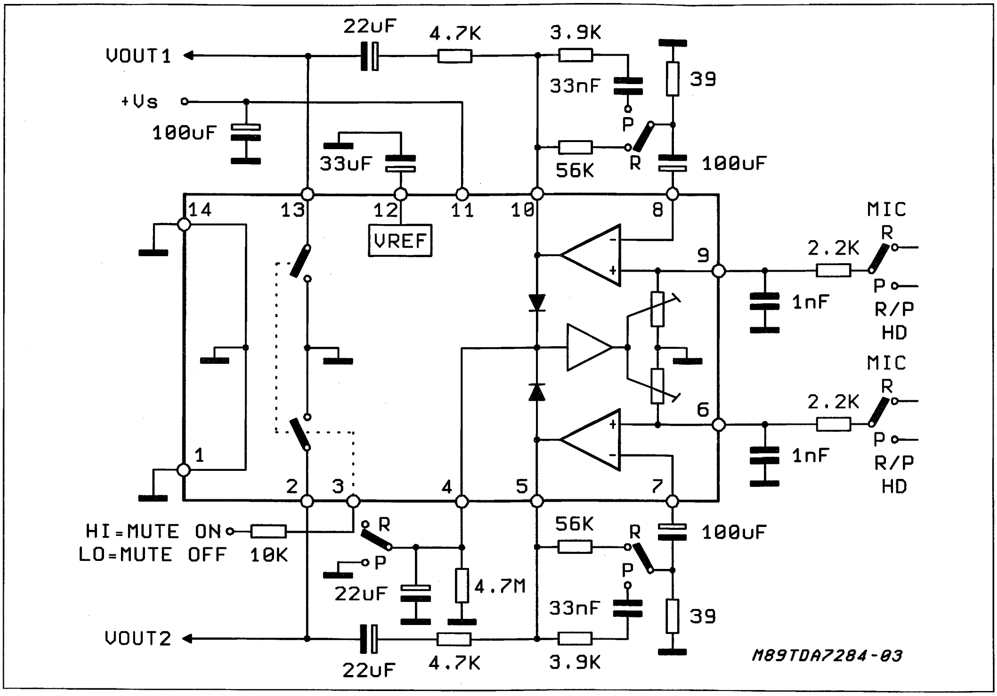


Figure 22: Application Circuit with Output Muting



SVR

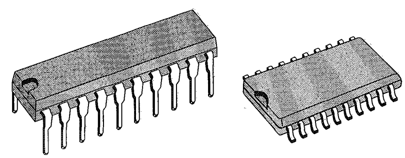
A refernce circuit is enclosed to provide a stable voltage and to supply a stable current to all current mirrors.

SVR capacitor is also connected to this block for good ripple rejection.

STEREO CASSETTE PLAYER AND MOTOR SPEED CONTROLLER

ADVANCE DATA

- WIDE OPERATING SUPPLY VOLTAGE (1.8V to 6V)
- HIGH OUTPUT POWER (30mW/32Ω/3V)
- LOW DISTORTION DC VOLUME CONTROL
- NO BOUCHEROT CELL
- LOW QUIESCENT CURRENT (15mA)
- NO INPUT CAPACITORS FOR PREAMPLIFIERS
- LOW MOTOR REFERENCE VOLTAGE (200mV)



DIP20 **SO20**

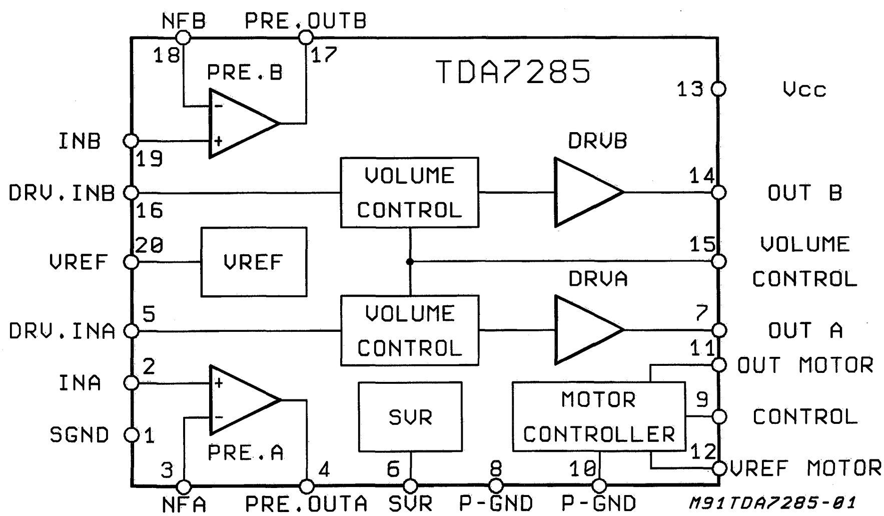
ORDERING NUMBERS:

TDA7285 TDA7285D

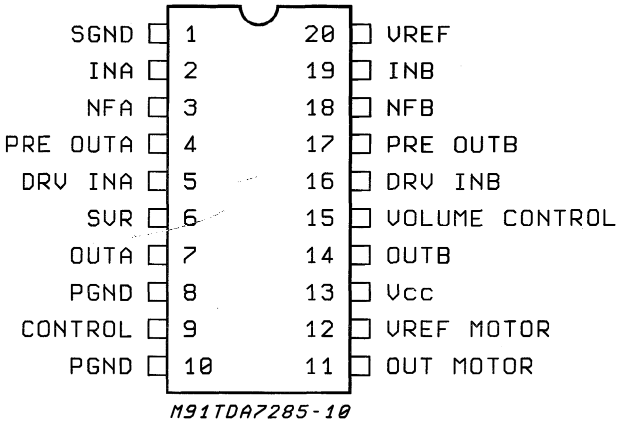
DESCRIPTION

The TDA7285 is a monolithic integrated circuit designed for the portable players market and assembled in a plastic DIP20 and SO20. The internal functions are: preamplifier, DC volume control, headphone driver and motor speed controller.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	8	V
I_{Omax}	Maximum Output Current	70	mA
$I_{m\ max}$	Maximum Motor Current	700	mA
P_{tot}	Total Power Dissipation T_{amb} = 90°C	0.9	W
T_{op}	Operating Temperature	-20 to +70	°C
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description	SO20	DIP20	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	150	100	°C/W

DC CHARACTERISTICS (T_{amb} = 25°C; V_S = 3V; R_L = 32Ω (Headphone) and R_L = 10KΩ (Preamplifier); V_i = 0; VOL. Control = V_{ref}).

Terminal No	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Term. Volt. (V)	0	1.5	1.5	1.5	1.5	2.7	1.4	0	2.8	0	1.6	3	3	1.4	1.5	1.5	1.5	1.5	1.5	1.5

ELECTRICAL CHARACTERISTICS (V_S = 3V; R_L = 32Ω, Vol. Control = 2/3 V_{ref} (pin 20); T_{amb} = 25°C; f = 1KHz; unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Range		1.8		6	V
I_d	Total Quiescent Drain Current			15	22	mA
PLAYBACK AMPLIFIER						
G_{vo}	Open Loop Gain			70		dB
G_v	Close Loop Gain			33		dB
V_O	Output Voltage	THD = 1%	600	750		mV
THD	Total Harmonic Distortion	V_O = 330mVrms		0.05	0.25	%
I_b	Bias Current			3		µA
C_t	Cross Talk	R_S = 2.2KΩ; V_O = 330mVrms		74		dB
e_n	Total Input Noise	R_S = 2.2KΩ; B = 22Hz to 22KHz		1.2		µV
SVR1	Ripple Rejection	R_S = 2.2KΩ; Vr = 100mVrms f = 100Hz; C_{SVR} = 100µF		50		dB
HEADPHONE DRIVER						
V_{DC}	Output DC Voltage			1.4		V
P_O	Output Power	THD = 10%	20	30		mW
P_{O1}	Transient Output Power	THD = 10% R_L = 16Ω		50		mW
G_V	Close Loop Gain	P_O = 5mW		31		dB
	Volume Control range		66	75		dB
THD	Total Harmonic Distortion	P_O = 5mW		0.3	1	%
C_t	Cross Talk	P_O = 5mW; R_S = 10KΩ		50		dB
SVR2	Ripple Rejection	R_S = 600Ω; Vr = 100mV f = 100Hz; C_{SVR} = 100µF		47		dB
MOTOR SPEED CONTROL						
V_{ref}	Motor Reference Voltage (pin 12)		0.18	0.20	0.22	V
K	Shunt Ratio	I_m = 100mA	45	50	55	-
V_{sat}	Residual Voltage	I_m = 100mA		0.13	0.30	V
$\frac{\Delta V_{ref}}{V_{ref}} / \Delta V_S$	Line Regulation	I_m = 100mA; V_S = 1.8 to 6V		0.20	0.8	%/V
$\frac{\Delta K}{K} / \Delta V_S$	Voltage Characteristics of Shunt Ratio	I_m = 100mA; V_S = 1.8 to 6V		0.80	3	%/V
$\frac{\Delta V_{ref}}{V_{ref}} / \Delta I_m$	Load Regulation	I_m = 30 to 200mA		0.015	0.08	%/mA
$\frac{\Delta K}{K} / \Delta I_m$	Current Characteristics of Shunt Ratio	I_m = 30 to 200mA		0.03	0.1	%/mA
$\frac{\Delta V_{ref}}{V_{ref}} / \Delta T_{amb}$	Temperature Characteristics of Reference Voltage	I_m = 100mA T_{amb} = -20 to +60°C		0.04		%/°C
$\frac{\Delta K}{K} / \Delta T_{amb}$	Temperature Characteristics of Shunt Ratio	I_m = 100mA T_{amb} = -20 to +60°C		0.02		%/°C

Figure 1: Test and Application Circuit

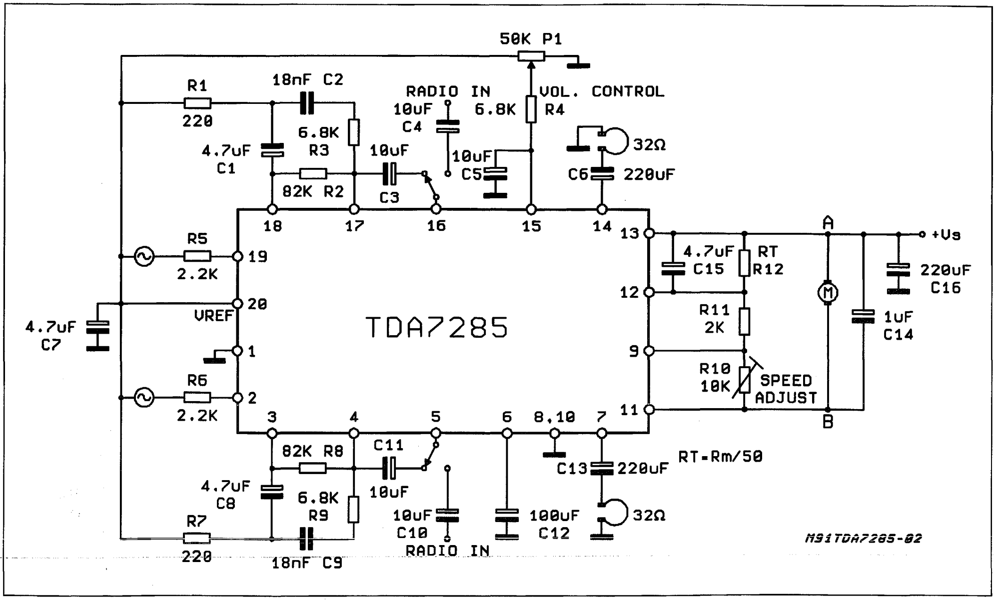


Figure 2: P.C. Board and Component Layout of the Circuit of Figure 2 (1:1 scale)

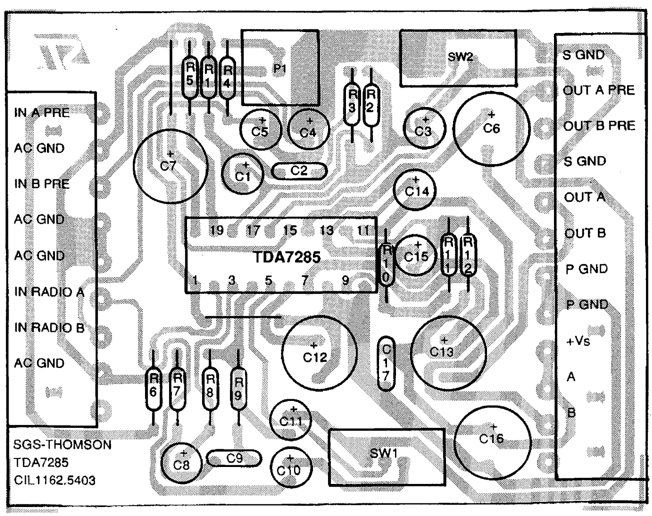


Figure 3: Quiescent Drain Current vs. Supply Voltage

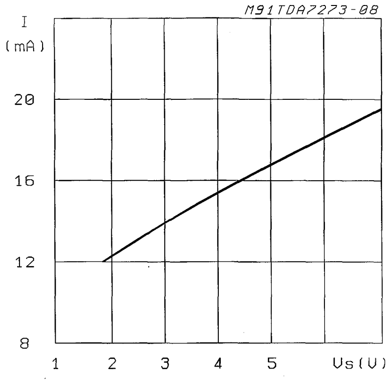


Figure 4: Reference voltage Vs/2 (pin 20) vs. Supply Voltage

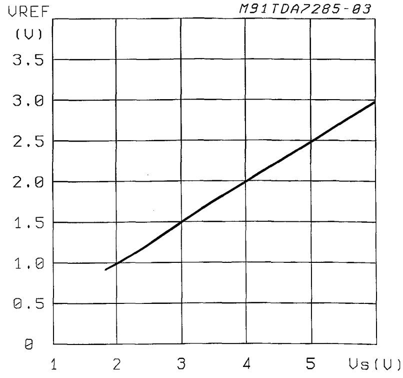


Figure 5: Closed Loop Gain vs. Frequency (PREAMPLIFIER)

Figure 6: Distortion vs. Frequency (PREAMPLIFIER)

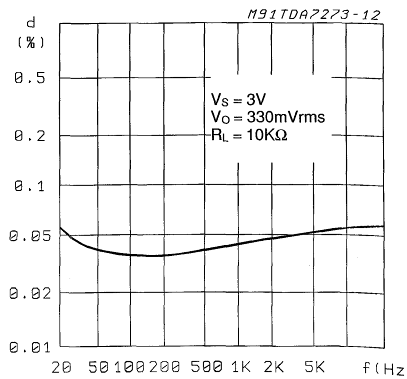


Figure 7: Supply Voltage Rejection vs. Frequency (PREAMPLIFIER)

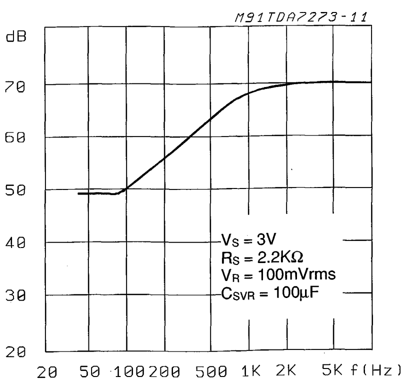


Figure 8: Quiescent Output Voltage vs. Supply Voltage (DRIVER)

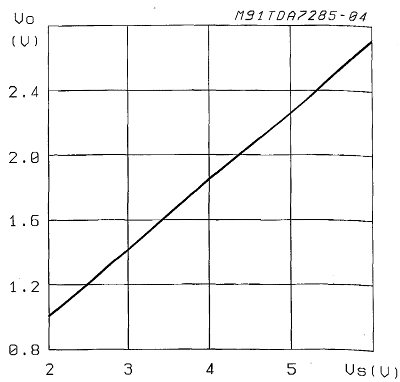


Figure 9: Closed Loop Gain vs. Frequency (DRIVER)

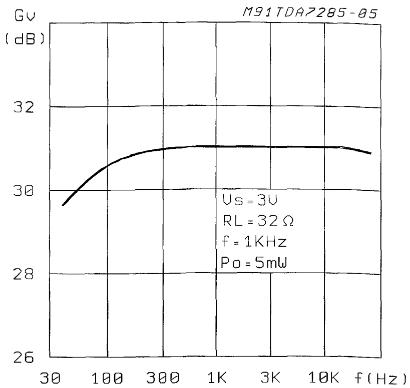


Figure 10: Output Power vs. Supply Voltage (DRIVER)

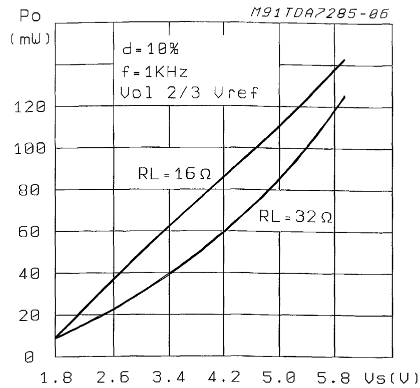


Figure 11: Distortion vs. Output Power (DRIVER)

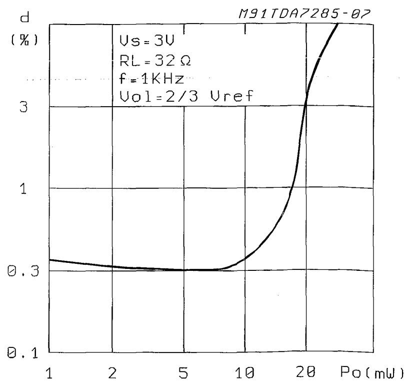


Figure 12: Distortion vs. Frequency (DRIVER)

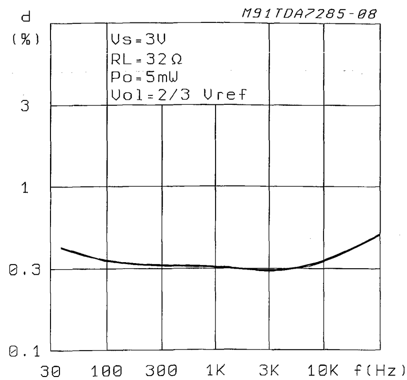


Figure 13: Supply Voltage Rejection vs. Frequency (DRIVER

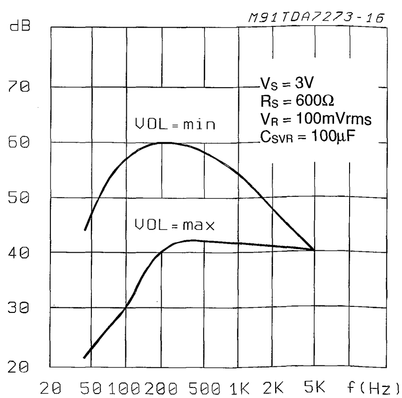


Figure 14: Volume Control (0dB = 10mW; V_S = 3V; R_{VOL} = 50KΩ; R_L = 32Ω; f = 1KHz) (DRIVER)

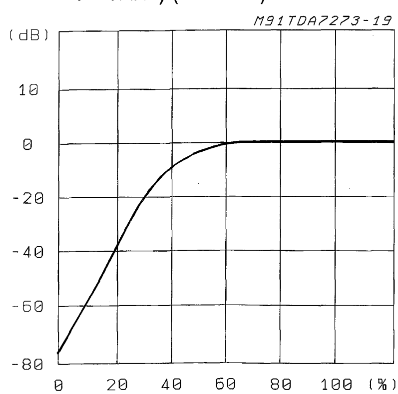


Figure 15: Reference Voltage (Pin 12) vs. Supply Voltage (MOTOR)

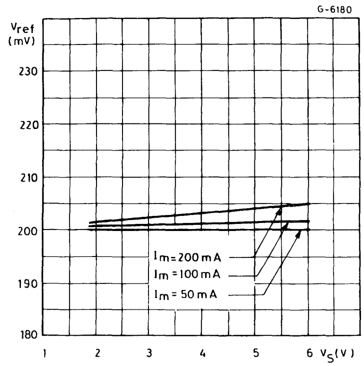


Figure 16: Shunt Ratio vs. Supply Voltage (MOTOR)

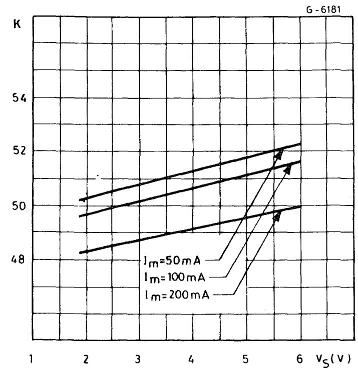


Figure 17: Sunt Ratio vs. Load Current (MOTOR)

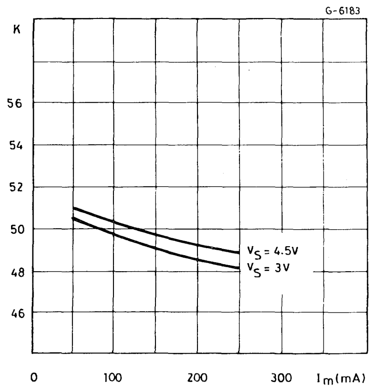


Figure 18: Saturation Voltage vs. Load Current (MOTOR)

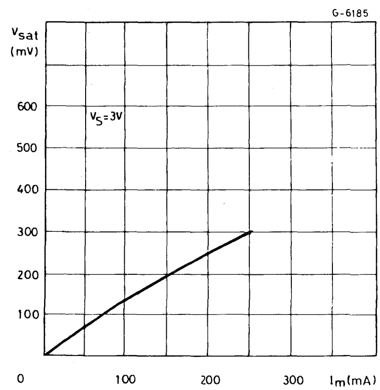


Figure 19: Speed Variations vs. Supply Voltage (MOTOR)

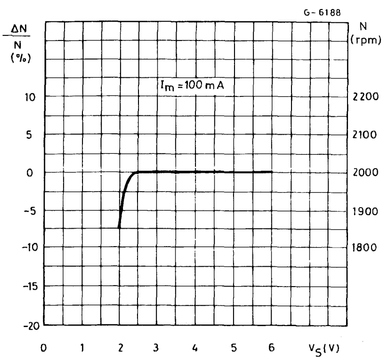
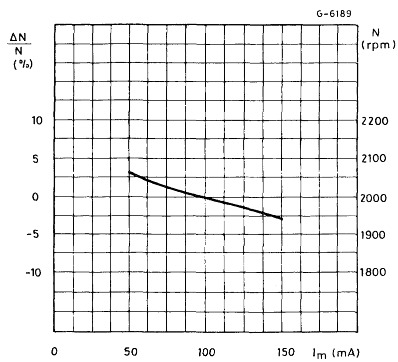
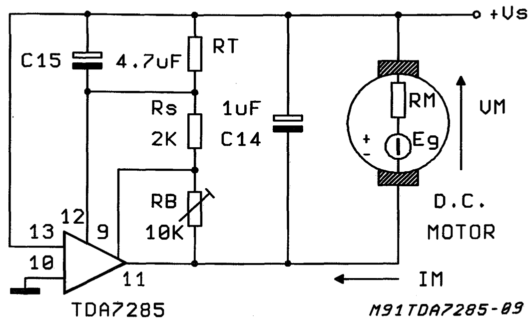


Figure 20: Speed Variations vs. Motor Current (MOTOR)



APPLICATION INFORMATION

Figure 21.



$$E_g = R_T\, I_d + I_M \left(\frac{R_T}{K} - R_M \right) + V_{ref}$$

$$\left[1 + \frac{R_b}{R_S} + \frac{R_T}{R_S} \left(1 + \frac{1}{K} \right) \right]$$

R_S has to be adjusted so that the applied voltage V_M is suitable for a given motor, the speed is then linearly adjustable varing R_B.

The value R_T is calculated so that

$R_{T\,(max.)} > K_{(min.)} * R_{M\,(min.)}$

if $R_{T\,(max.)} > K * R_M$, instability may occur.

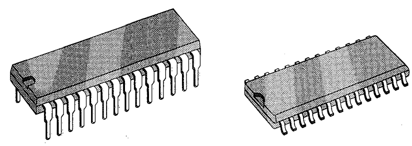
The values of C15 (4.7μF typ.) and C14 (1μF typ.) depend on the type of motor used. C15 adjusts WOW and flutter of the system. C14 suppresses motor spikes.

SGS-THOMSON MICROELECTRONICS

TDA7300

DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

- SINGLE SUPPLY OPERATION
- FOUR STEREO INPUT SOURCE SELECTION
- MONO INPUT
- TREBLE, BASS, VOLUME, AND BALANCE CONTROL
- FOUR INDEPENDENT SPEAKER CONTROL (FRONT/REAR)
- SINGLE SUPPLY OPERATION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- VERY LOW NOISE AND VERY LOW DISTORTION
- POP FREE SWITCHING



DIP28	SO28
ORDERING NUMBERS:	
TDA7300	TDA7300D

DESCRIPTION

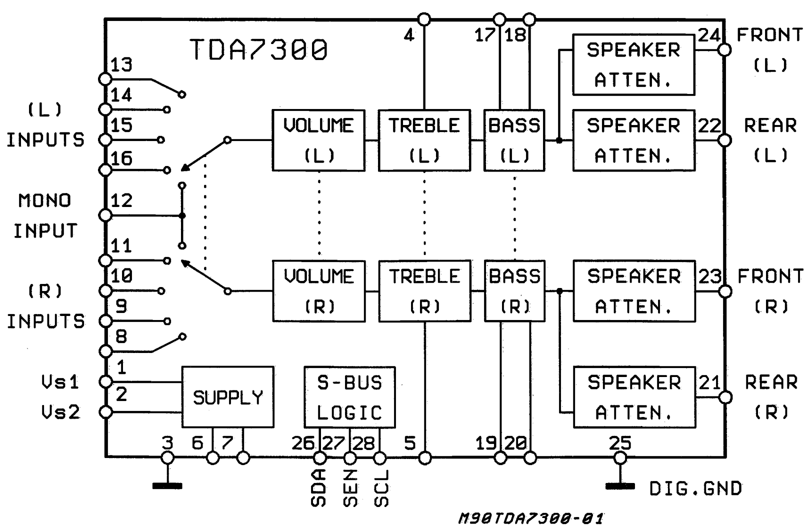
The TDA7300 is a volume, tone (bass and treble), balance (left/right) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi systems.

Control is accomplished by serial bus microprocessor interface.

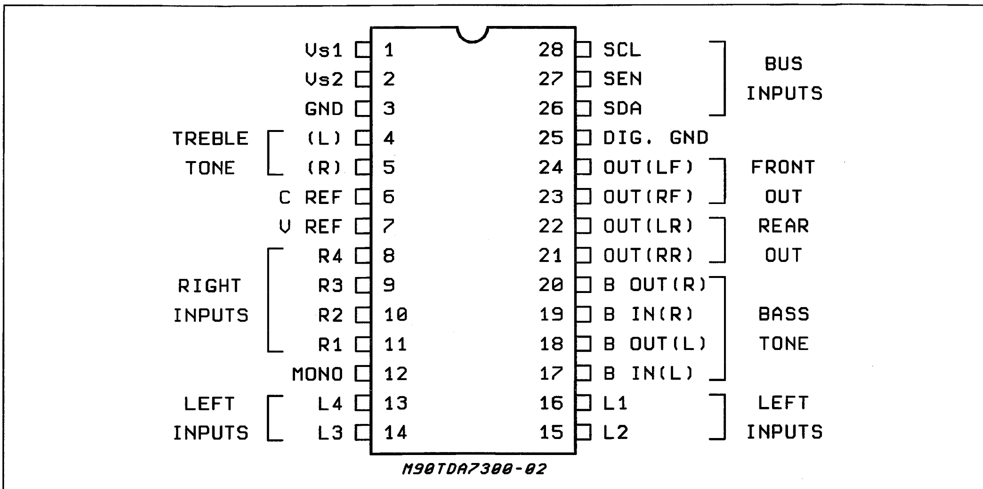
The AC signal setting is obtained by resistor networks and analog switches combined with operational amplifiers.

The results are: low noise, low distortion and high dynamic range.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (V_{S1})	18	V
T_{amb}	Operating Ambient Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		SO28	DIP28	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	85	65	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{S1} = 12V or V_{S2} = 8.5V , R_L = 10kΩ and R_g = 600Ω , f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY (1)						
V_{S1}	Supply Voltage VS1		10	12	16	V
V_{S2}	Supply Voltage VS2		6	8.5	10	V
I_{S2}	Supply Current		15	30	40	mA
V_{ref}	Reference Voltage (pin 7)		3.5	4.3	5	V
SVR	Ripple Rejection at V_{S1}	f = 300Hz to 10KHz	80	97		dB
SVR	Ripple Rejection at V_{S2}	f = 300Hz to 10KHz	50	58		dB
INPUT SELECTORS						
R_i	Input Resistance		30	45		KΩ
$V_{IN\ max}$	Max. Input Signal	GV = 0dB d = 0.3%	1.5	2.2		Vrms
IN_S	Input Separation	f = 1KHz (2)	90	100		dB
		f = 10KHz (2)	70	80		dB
$V_{i\ (DC)}$	Input DC Voltage		3.5	4.3	5	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VOLUME CONTROLS						
	Control Range			78		dB
G_{max}	Max Gain		8	10	12	dB
	Max Attenuation		64	68		dB
	Step Resolution	G_V = -50 to 10dB		2	3	dB
	Attenuator Set Error				2	dB
	Tracking Error				2	dB
SPEAKER ATTENUATORS						
	Control Range		35	38	41	dB
	Step Resolution			2	3	dB
	Attenuator Set Error				2	dB
	Tracking Error				2	dB
BASS AND TREBLE CONTROL (3)						
	Control Range			±15		dB
	Step Resolution			2.5	3.5	dB
AUDIO OUTPUT						
V_O	Max. Output Voltage	d = 0.3%	1.5	2.2		Vrms
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				1	nF
R_O	Output Resistance			70	150	Ω
V_O(DC)	DC Voltage Level		3	3.8	4.5	V
GENERAL						
e_{NO}	Output Noise	BW = 22Hz to 22KHz, G_v = 0dB		6	15	μV
		Curve A G_v = 0dB		4		μV
S/N	Signal to Noise Ratio	All gain = 0dB V_O = 1Vrms BW = 22Hz to 22KHz		105		dB
d	Distortion	f = 1KHz; V_O = 1V; G_v = 0		0.01	0.1	%
	Frequency Response (-1dB)	G_v = 0 High Low	20		 20	KHz Hz
S_C	Channnel Separation left/right	f = 1KHz f = 10KHz	90 70	100 80		dB dB
BUS INPUTS						
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage		2.4			V
V_O	Output Voltage SDA Acknowledge	I = 1.6mA			0.4	V
	Digital Input Current		-5		+5	μA

Notes:
(1) The circuit can be supplied either at V_{S1} or without the use of the internal voltage regulator at V_{S2}. The circuit also operates at a supply voltage V_{S1} lower than 10V. In this case the ripple rejection of V_{S2} is valid, because the voltage regulator saturates to a saturation voltage of about 0.8V.
(2) The selected input is grounded thru the 2.2μF capacitor.
(3) Bass and Treble response see attached diagram. The center frequency and quality of the resonance behaviour can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.

Figure 1: Application Circuit

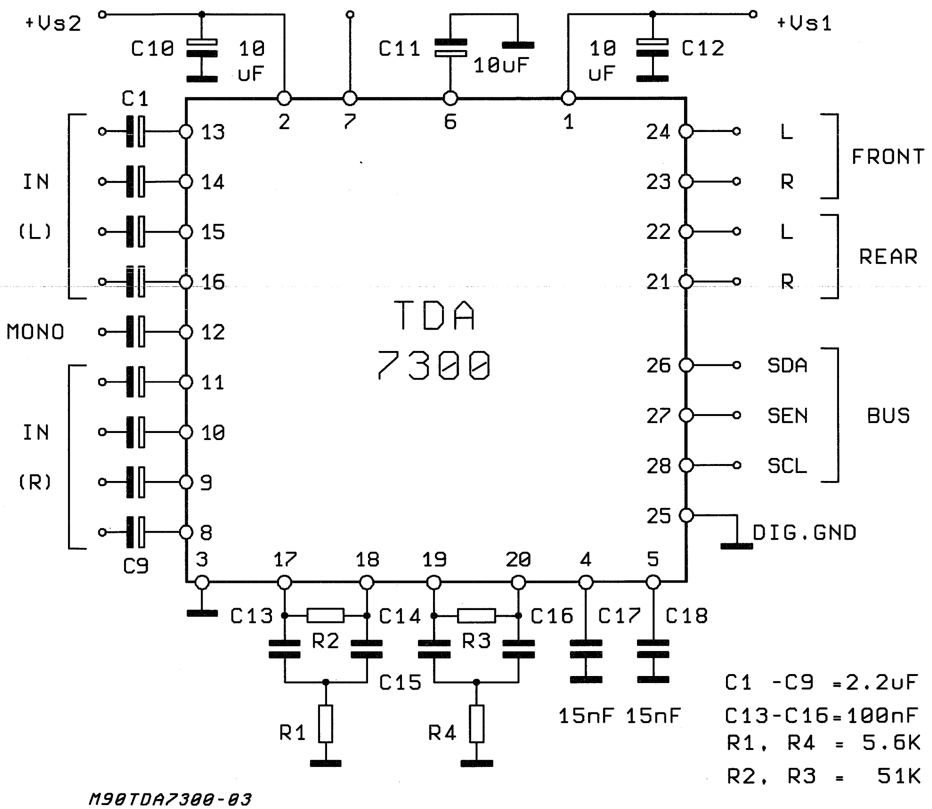
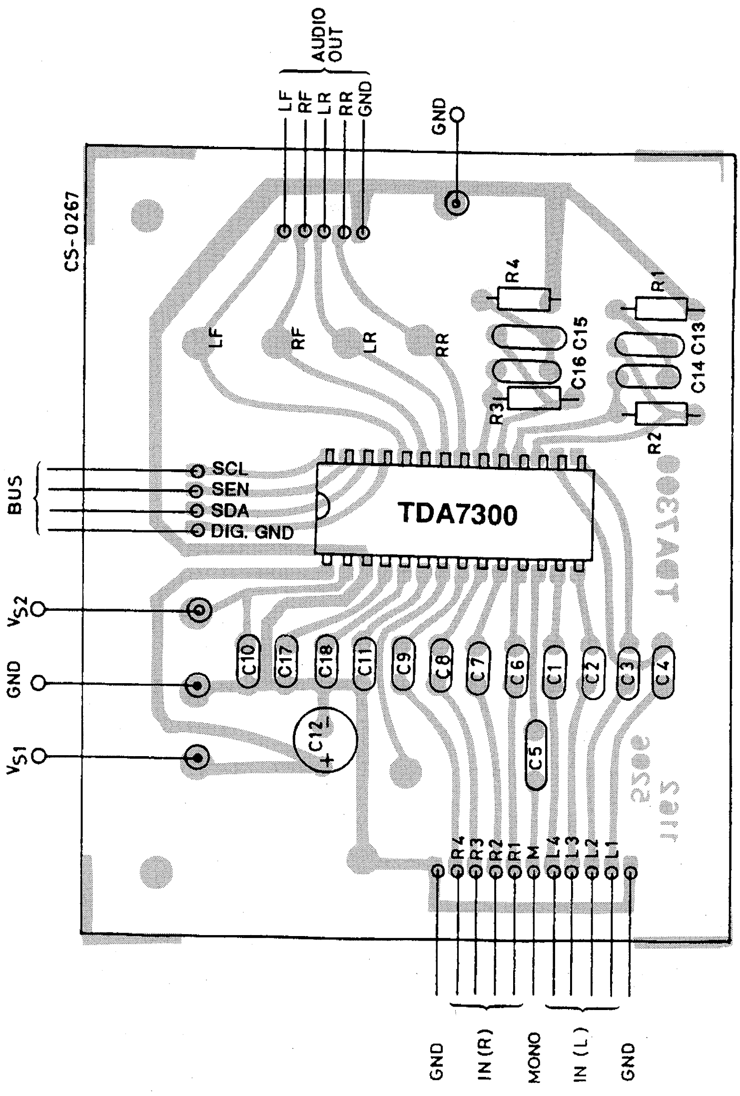


Figure 2: P.C. Board and Components Layout of the Fig.1 (1:1 scale)



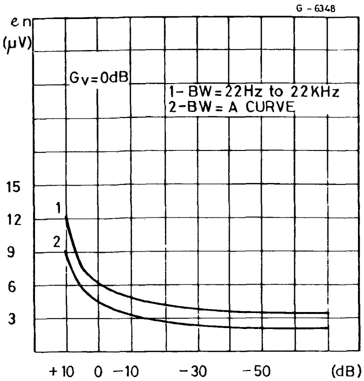


Figure 3: Total Output Noise vs. Volume Setting

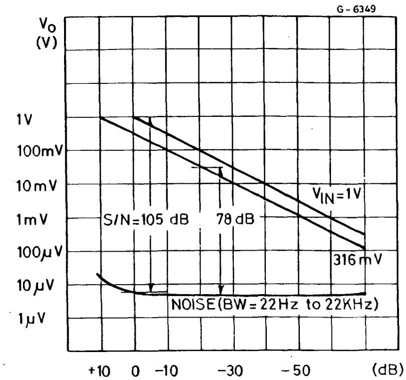


Figure 4: Signal to Noise Ratio vs. Volume Setting

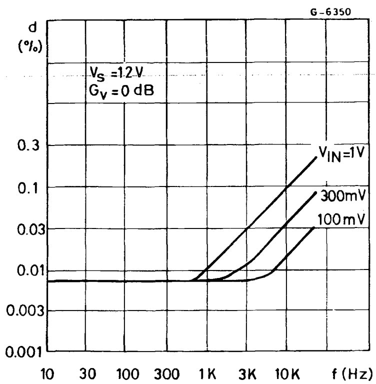


Figure 5: Distortion + Noise vs. Frequency

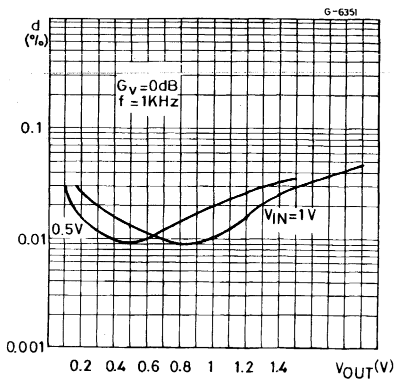


Figure 6: Distortion vs. Output Voltage

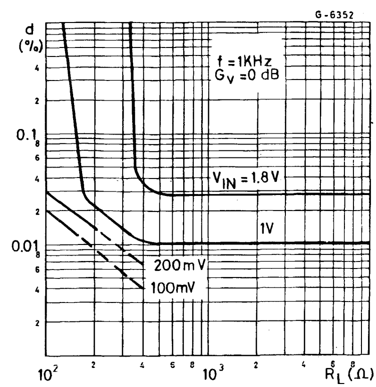


Figure 7: Distortion vs. Load Resistance

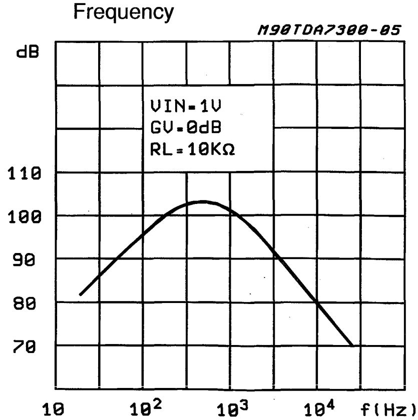


Figure 8: Channel Separation (L1 - R1) vs. Frequency

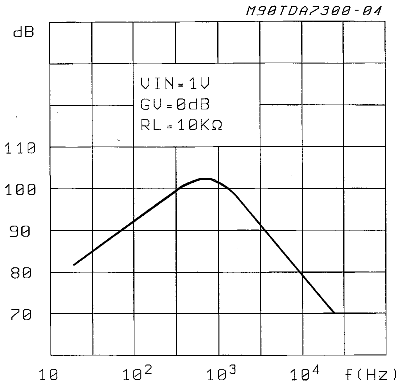


Figure 9: Input Separation (L1 - L2) vs. (V_{S1}) Frequency

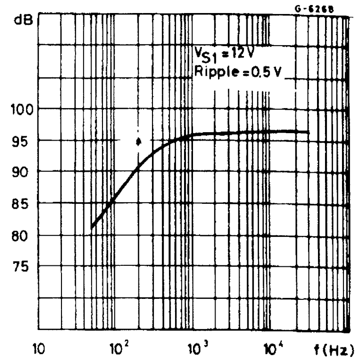


Figure 10: Supply Voltage Rejection (V_{S1}) vs. Frequency

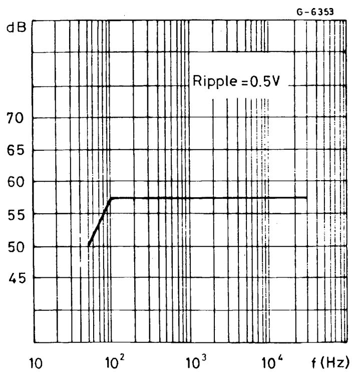


Figure 11: Supply Voltage Rejection (V_{S2}) vs. Frequency

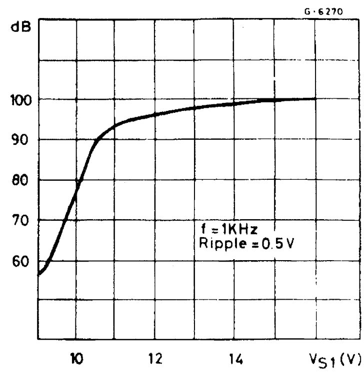


Figure 12: Supply Voltage Rejection vs. V_{S1}

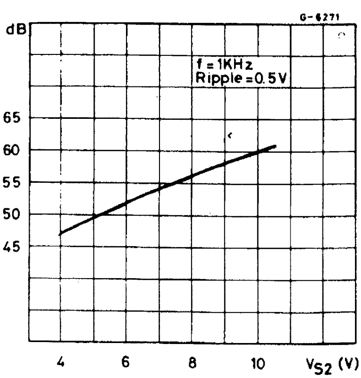


Figure 13: Supply Voltage Rejection vs. V_{S2}

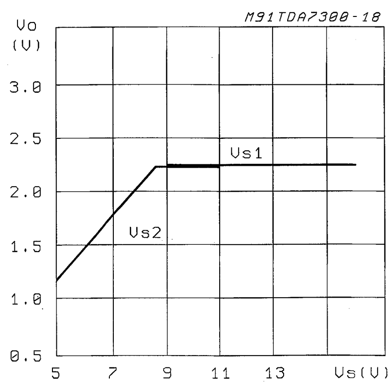


Figure 14: Clipping Level (Vrms) vs. Supply Voltage

APPLICATION INFORMATION

Volume Control Concept

Traditional electronic volume control circuits use a multiplier technique with all the disadvantages of high noise and distortion.

The used concept, as shown in Fig. 15 with digital switched resistor dividers, provides extremely low noise and distortion. The multiplexing of the resistive dividers is realized with a multiple-input operational amplifier.

Bass and Treble Control

The principle operation of the bass control is shown in Fig. 16. The external filter together with the internal buffer allows a flexible filter design according to the different requirements in car radios. The function of the treble is similar to the bass.
A typical curve is shown in Fig.19.

Outputs

A special class-A output amplifier with a modulated sink current provides low distortion and ground compatibility with low current consumption.

Figure 15: Volume Control

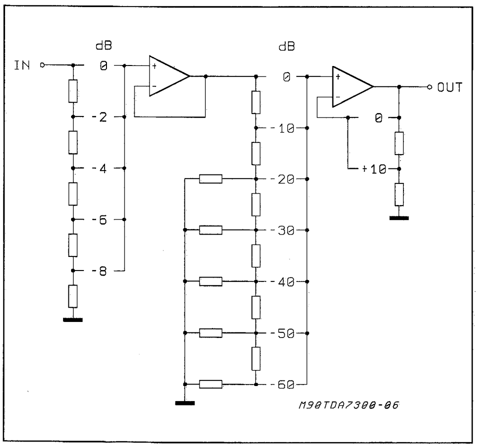


Figure 16: Bass Control

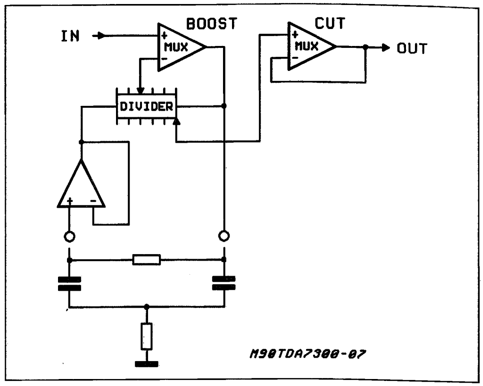


Figure 17: Quiescent Current vs. Supply Voltage

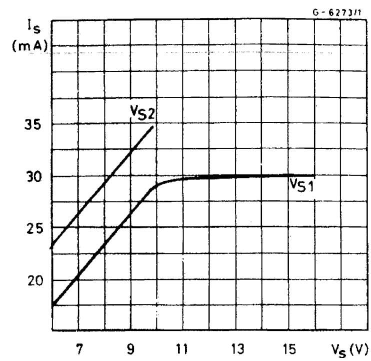
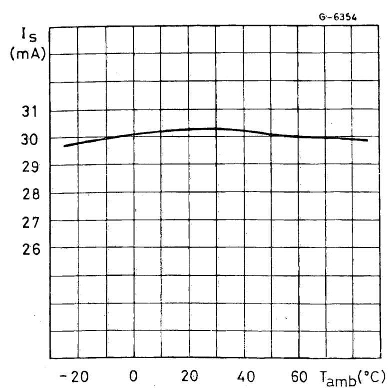


Figure 18: Quiescent Current vs. Temperature



APPLICATION INFORMATION (continued)

Figure 19: Typical Tone Response

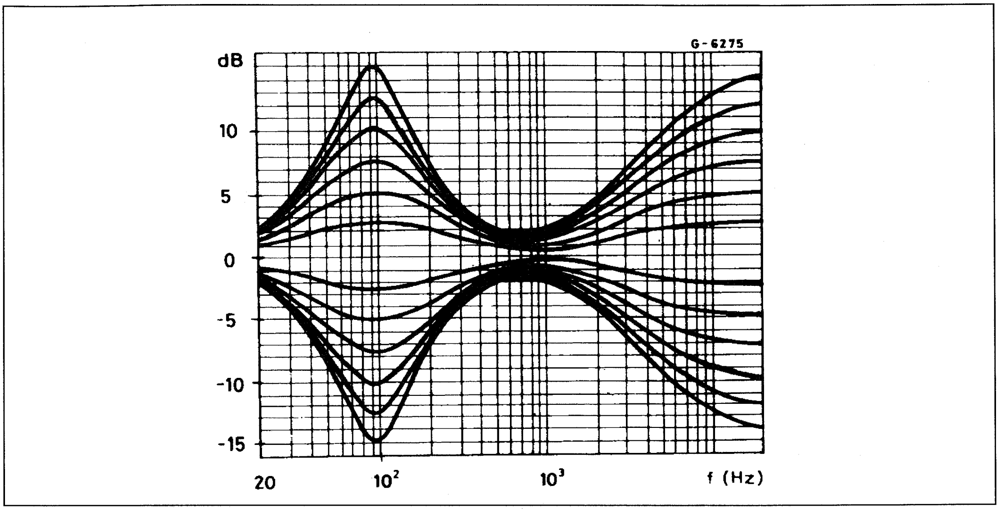
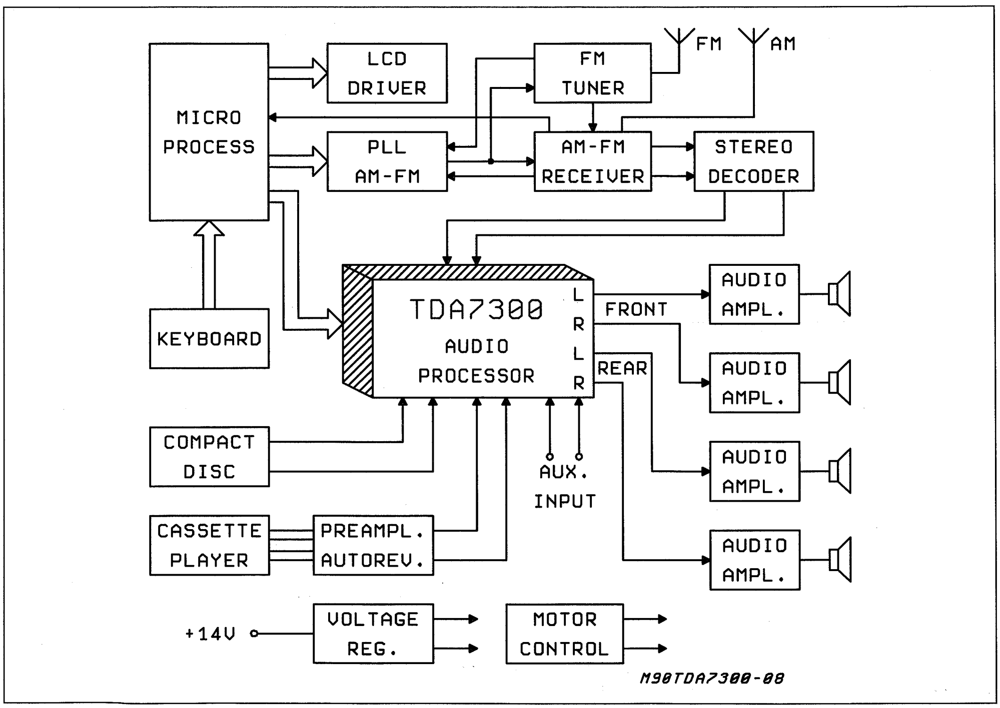


Figure 20: Complete Car-Radio System using Digital Controlled Audio Processor



APPLICATION INFORMATION (continued)

SERIAL BUS INTERFACE

S-BUS Interface and I²CBUS Compatibility

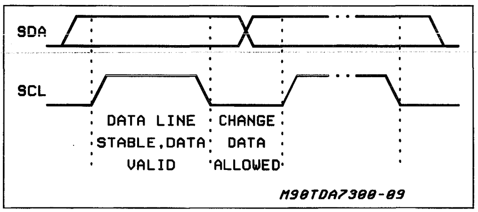
Data transmission from microprocessor to the TDA7300 and viceversa takes place thru the 3-wire S-BUS interface, consisting of the three lines SDA, SCL, SEN. If SDA and SEN inputs are short-circuited together, then the TDA7300 appears as a standard I²CBUS slave.

According to I²CBUS specification the S-BUS lines are connected to a positive supply voltage via pull-up resistors.

Data Validity

As shown in fig. 21, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Figure 21: Data Validity on the I²CBUS



Start and Stop Conditions

I²CBUS:
as shown in fig.22 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

S-bus:
the start/stop conditions (points 1 and 6) are detected exclusively by a transition of the SEN line (1 → 0 / 0 → 1) while the SCL line is at the HIGH level.

The SDA line is only allowed to change during the time the SCL line is low (points 2, 3, 4, 5). After the start information (point 1) the SEN line returns to the HIGH level and remains unchanged for all the time the transmission is performed.

Byte Format

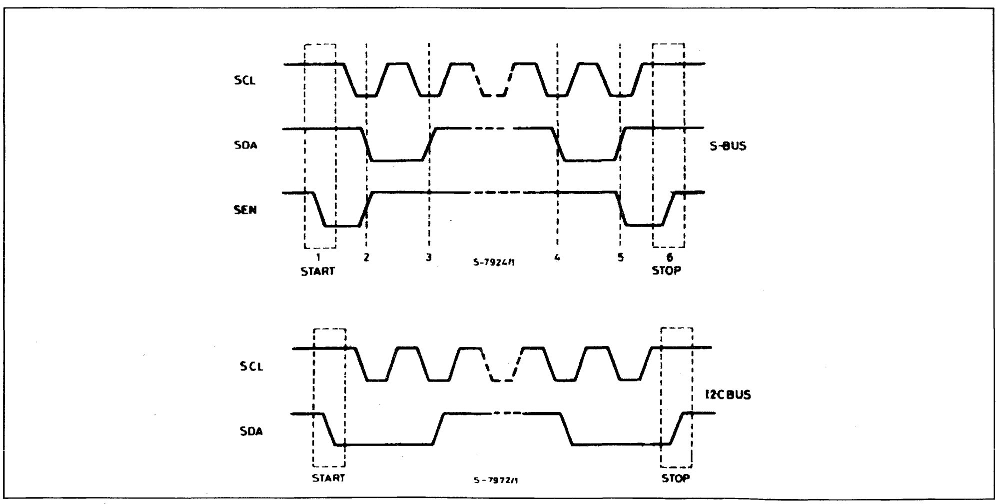
Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 23). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

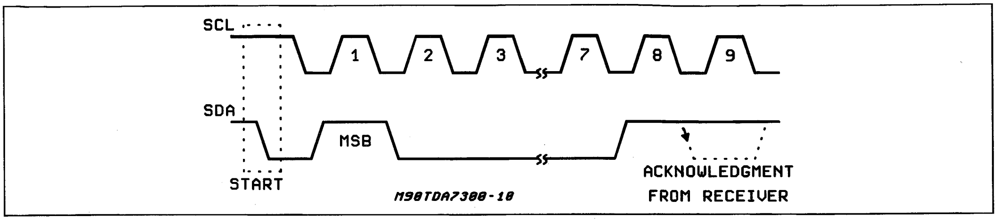
The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Figure 22: Timing Diagram of S-BUS and I²CBUS



APPLICATION INFORMATION (continued)

Figure 23: Acknowledge on the I²CBUS



Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7300 address (the 8th bit of the byte must be 0). The TDA7300 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)

TDA7300 ADDRESS (first byte, MSB … LSB); then DATA bytes (MSB … LSB), each followed by ACK

S	1	0	0	0	1	0	0	0	ACK				DATA				ACK				DATA					ACK	P

Data Transferred (N-bytes + Acknowledge)

ACK = Acknowledge
S = Start
P = Stop

MAX CLOCK SPEED 100kbits/s

SOFTWARE SPECIFICATION

Chip address (TDA7300 address)

1	0	0	0	1	0	0	0
MSB							LSB

DATA BYTES

Status after power-on reset

DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	X	X	S2	S1	S0	Audio Switch
0	1	1	0	C3	C2	C1	C0	Bus Control
0	1	1	1	C3	C2	C1	C0	Treble Control

X = don't care
Ax = 2dB steps
Bx = 10dB steps
Cx = 2.5dB steps

STATUS AFTER POWER-ON-RESET

Volume	– 68 dB
Speaker	– 38 dB
Audio Switch	Mono
Bass	+ 2.5 dB
Treble	+ 2.5 dB

SOFTWARE SPECIFICATION (continued)
DATA BYTES (detailed description)

VOLUME

MSB							LSB	
0	0	B2	B1	B0	A2	A1	A0	Volume 2dB Steps
					0	0	0	0
					0	0	1	-2
					0	1	0	-4
					0	1	1	-6
					1	0	0	-8
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
0	0	B2	B1	B0				Volume 10dB steps
		0	0	0				+10
		0	0	1				0
		0	1	0				-10
		0	1	1				-20
		1	0	0				-30
		1	0	1				-40
		1	1	0				-50
		1	1	1				-60

For example if you want setting the volume at -32dB the 8 bit string is: 0 0 1 0 0 0 0 1

SPEAKER ATTENUATORS

MSB							LSB	
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-2
					0	1	0	-4
					0	1	1	-6
					1	0	0	-8
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30

For example attenuation of 24dB on speaker RF is given by: 1 0 1 1 0 0 1 0

SOFTWARE SPECIFICATION (continued)

AUDIO SWITCH - Select the input Channel to Activate

MSB							LSB	
0	1	0	X	X	S2	S1	S0	Audio Switch
			X	X	0	0	0	Stereo 1
			X	X	0	0	1	Stereo 2
			X	X	0	1	0	Stereo 3
			X	X	0	1	1	Stereo 4
			X	X	1	0	0	Mono
			X	X	1	0	1	Not Allowed
			X	X	1	1	0	Not Allowed
			X	X	1	1	1	Not Allowed

X = don't care
For example to set the stereo 2 channel the 8 bit string may be: 0 1 0 0 0 0 0 1

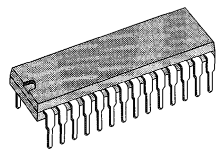
BASS AND TREBLE - Control Range of ± 15 dB (boost and cut) Steps of 2.5 dB

0	**1**	**1**	**0**	**C3**	**C2**	**C1**	**C0**	**Bass**
0	**1**	**1**	**1**	**C3**	**C2**	**C1**	**C0**	**Treble**
				0	0	0	0	– 15
				0	0	0	1	– 15
				0	0	1	0	– 12.5
				0	0	1	1	– 10
				0	1	0	0	– 7.5
				0	1	0	1	– 5
				0	1	1	0	– 2.5
				0	1	1	1	– 0
				1	1	1	1	+ 0
				1	1	1	0	+ 2.5
				1	1	0	1	+ 5
				1	1	0	0	+ 7.5
				1	0	1	1	+ 10
				1	0	1	0	+ 12.5
				1	0	0	1	+ 15
				1	0	0	0	+ 15

C3 = Sign
For example Bass at -12.5dB is obtained by the following 8 bit string: 0 1 1 0 0 0 1 0

DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

- INPUT AND OUTPUT PINS FOR EXTERNAL EQUALIZER
- THREE STEREO INPUT SOURCE SELECTION PLUS MONO INPUT
- TREBLE, BASS, VOLUME AND BALANCE CONTROL
- FOUR INDEPENDENT SPEAKER CONTROL (FRONT/REAR)
- SINGLE SUPPLY OPERATION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- VERY LOW NOISE AND VERY LOW DISTORTION
- POP FREE SWITCHING



DIP28

ORDERING NUMBER: TDA7302

DESCRIPTION

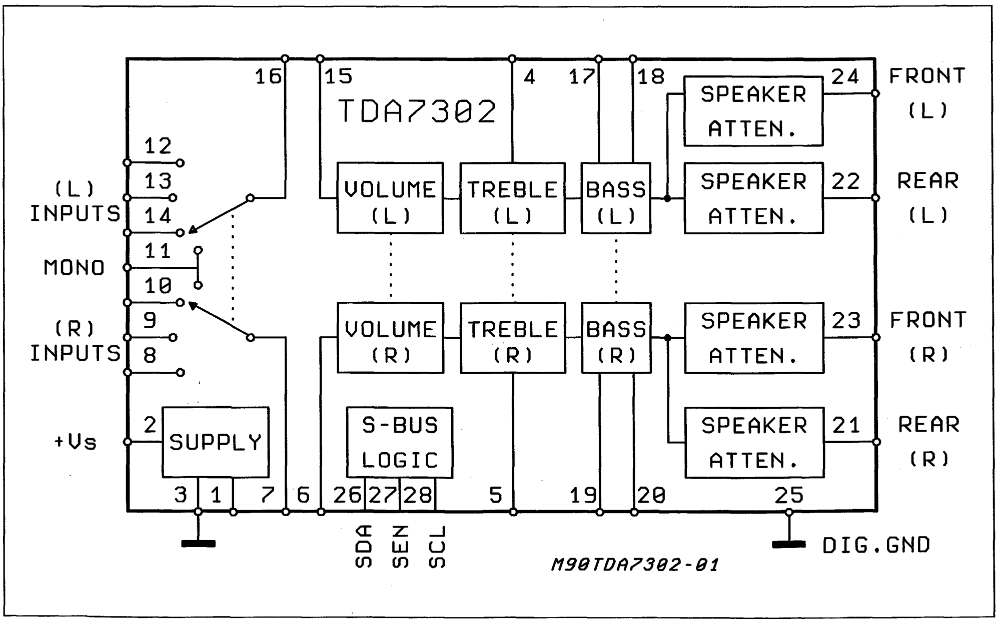
The TDA7302 is a volume, tone (bass and treble), balance (left/right) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi system.

Control is accomplished by serial bus microprocessor interface.

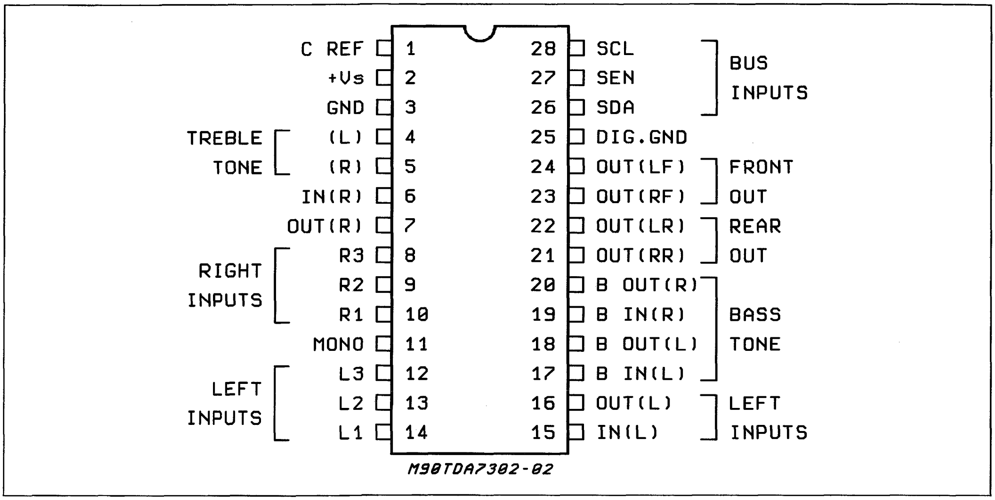
The AC signal setting is obtained by resistor networks and analog switches combined with operational amplifiers.

The results are: low noise, low distortion and high dynamic range.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	14	V
P_{tot}	Total Power Dissipation T_{amb} = 25°C	2	W
T_{amb}	Operating Ambient Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	65	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 10V, R_L = 10kΩ, R_g = 600Ω , f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	10	14	V
I_S	Supply Current		15	30	40	mA
SVR	Ripple Rejection	f = 300Hz to 10KHz	50	58		dB
INPUT SELECTORS						
R_i	Input Resistance		30	45		KΩ
$V_{IN\ max}$	Max. Input Signal	GV = 0dB d = 0.3%	1.5	2.2		Vrms
IN_S	Input Separation	f = 1KHz (2)	90	100		dB
		f = 10KHz (2)	70	80		dB
R_L	Output Load Resistance		5			KΩ
$V_{i\ (DC)}$	Input DC Voltage		3.5	4.3	5	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VOLUME CONTROLS						
R_{IN}	Input Resistance		5	10	20	KΩ
	Control Range			78		mA
G_{max}	Max Gain		8	10	12	dB
	Max Attenuation		64	68		dB
	Step Resolution			2	3	dB
	Attenuator Set Error	G_V = -50 to 10dB			2	dB
	Tracking Error				2	dB
SPEAKER ATTENUATORS						
	Control Range		35	38	41	dB
	Step Resolution			2	3	dB
	Attenuator Set Error				2	dB
	Tracking Error				2	dB
BASS AND TREBLE CONTROL (1)						
	Control Range			±15		dB
	Step Resolution			2.5	3.5	dB
AUDIO OUTPUT						
V_O	Max. Output Voltage	d = 0.3%	1.5	2.2		Vrms
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				1	nF
R_O	Output Resistance			70	150	Ω
$V_O(DC)$	DC Voltage Level		3	3.8	4.5	V
GENERAL						
e_{NO}	Output Noise	BW = 22Hz to 22KHz, G_v = 0dB		6	15	µV
		BW = 22Hz to 22KHz, Out atten. ≥ 20dB		3.5		µV
		G_v = 0dB Curve A		4		µV
S/N	Signal to Noise Ratio	All gain = 0dB V_O = 1Vrms BW = 22Hz to 22KHz		105		dB
d	Distortion	f = 1KHz V_O = 1V G_v = 0		0.01	0.1	%
	Frequency Response (-1dB)	G_v = 0 High	20			KHz
		Low			20	Hz
S_C	Channnel Separation left/right	f = 1KHz	90	100		dB
		f = 10KHz	70	80		dB
BUS INPUTS						
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage		2.4			V
V_O	Output Voltage SDA Acknowledge	I = 1.6mA			0.4	V
	Digital Input Current		-5		+5	µA

Notes:
(1) Bass and Treble response see attached diagram. The center frequency and quality of the resonance behaviour can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.
(2) The selected input is grounded thru the 2.2µF capacitor.

Figure 1: Application Circuit

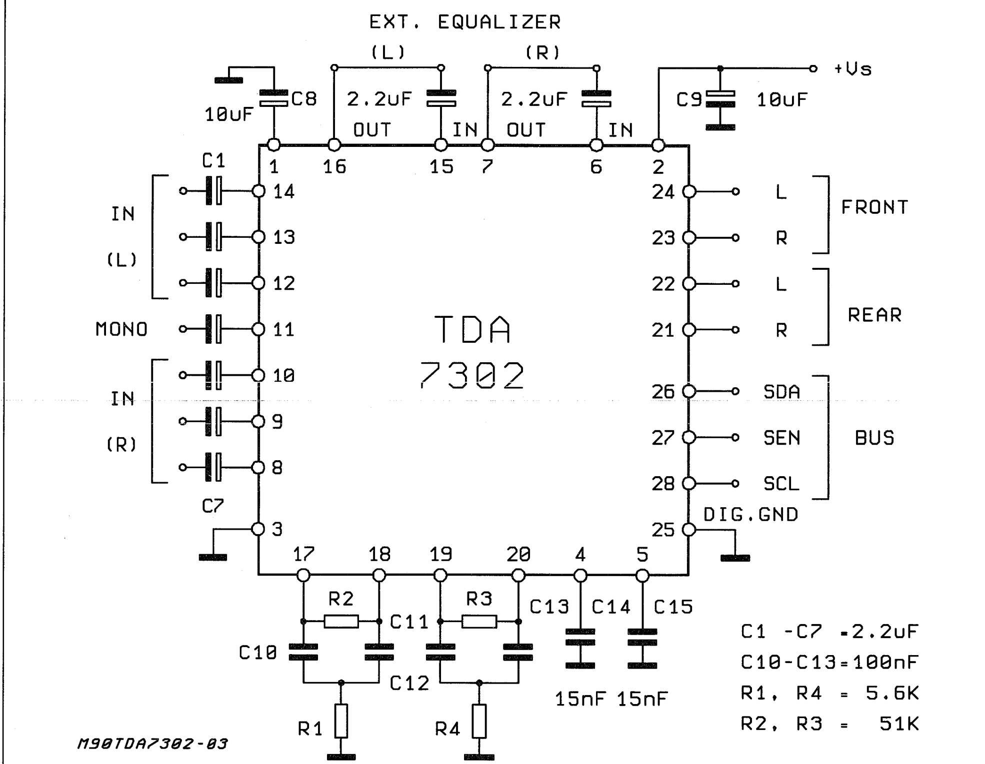


Figure 2: P.C. Board and Components Layout of the Fig.1 (1:1 scale)

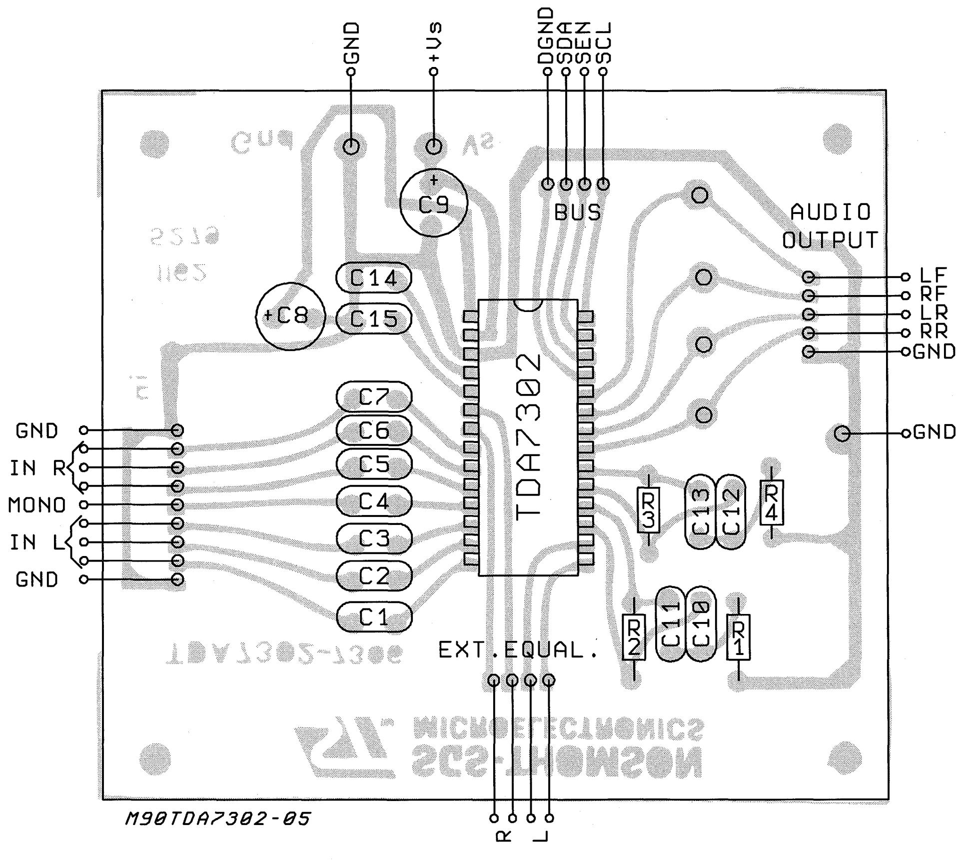


Figure 3: Total Output Noise vs. Volume Setting

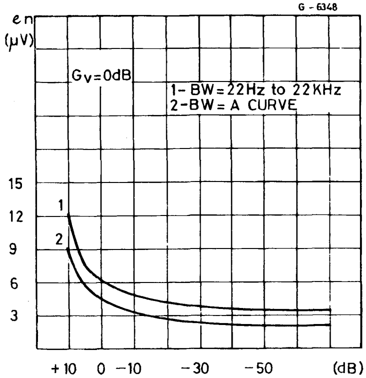


Figure 4: Signal to Noise Ratio vs. Volume Setting

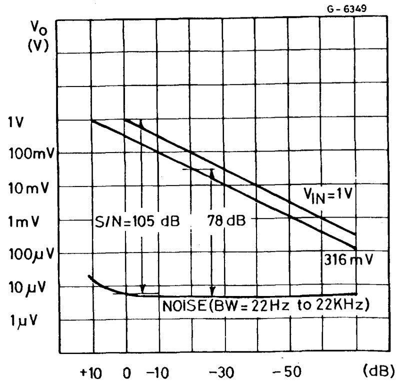


Figure 5: Distortion + Noise vs. Frequency

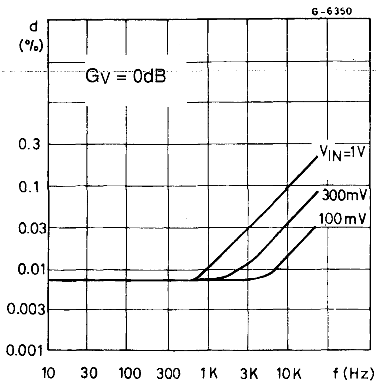


Figure 6: Distortion vs. Output Voltage

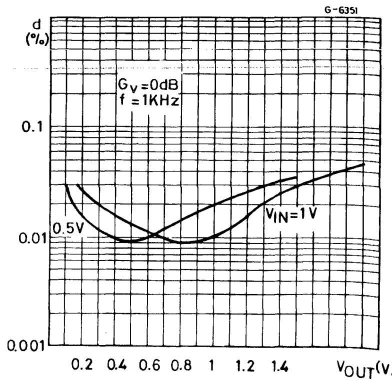


Figure 7: Distortion vs. Load Resistance

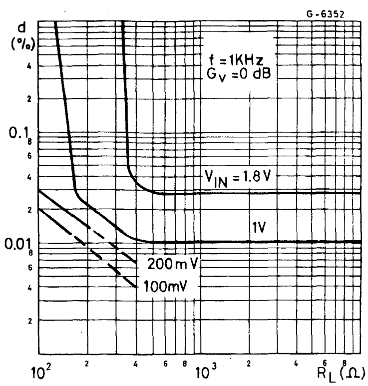
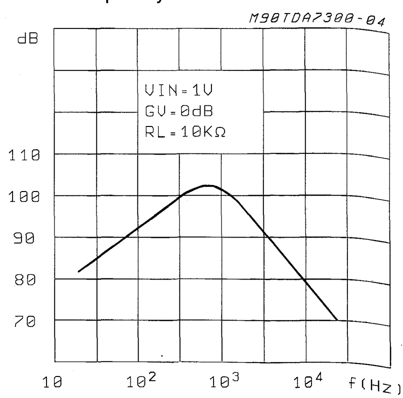


Figure 8: Channel Separation (L1 - R1) vs. Frequency



SGS-THOMSON MICROELECTRONICS

Figure 9: Input Separation (L1 - L2) vs. Frequency

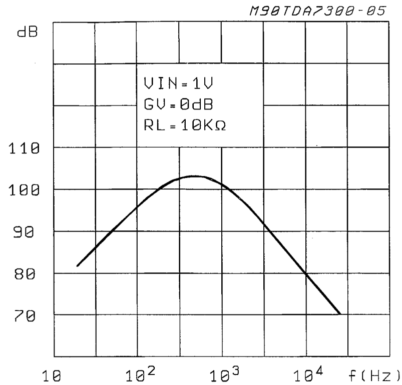


Figure 10: Supply Voltage Rejection vs. Frequency

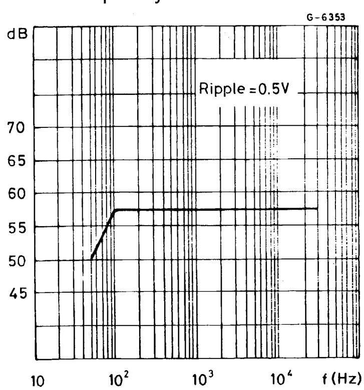
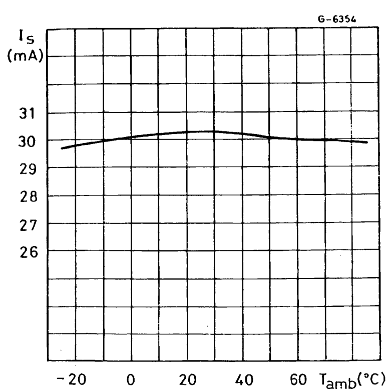


Figure 11: Quiescent Current vs. Temperature

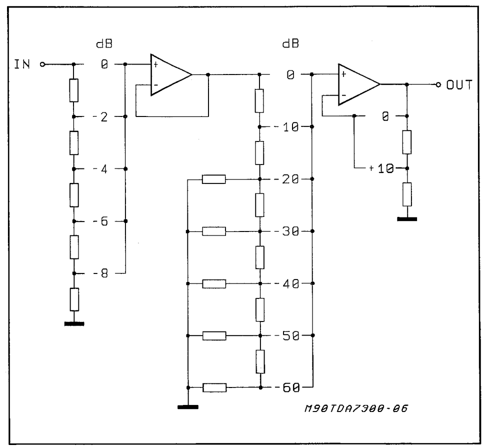


APPLICATION INFORMATION

Volume Control Concept

Traditional electronic volume control circuits use a multiplier technique with all the disadvantages of high noise and distortion.
The used concept, as shown in Fig. 12 with digital switched resistor dividers, provides extremely low noise and distortion. The multiplexing of the resistive dividers is realized with a multiple-input operational amplifier.

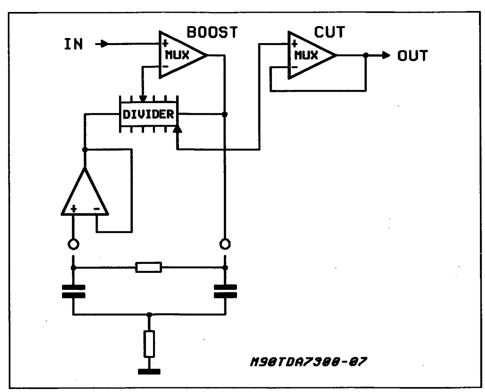
Figure 12: Volume Control



Bass and Treble Control

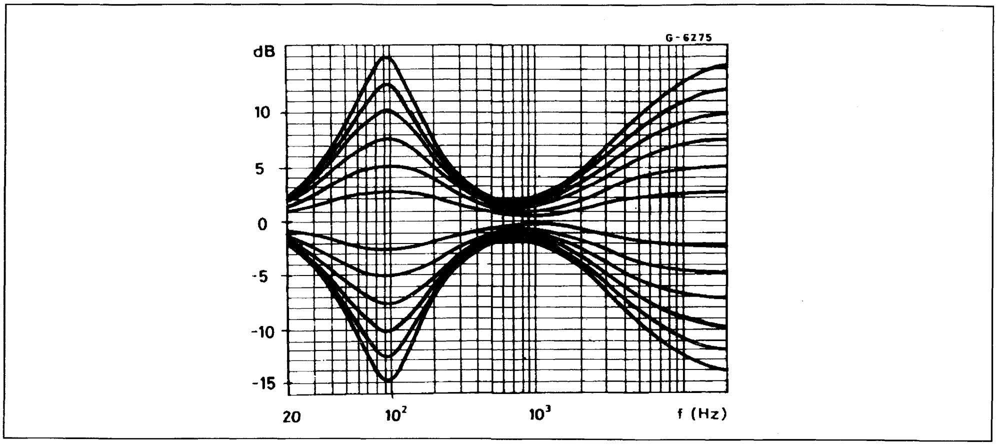
The principle operation of the bass control is shown in Fig. 12. The external filter together with the internal buffer allows a flexible filter design according to the different requirements in car radios. The function of the treble is similar to the bass.
A typical curve is shown in Fig.14.

Figure 13: Bass Control



APPLICATION INFORMATION (continued)

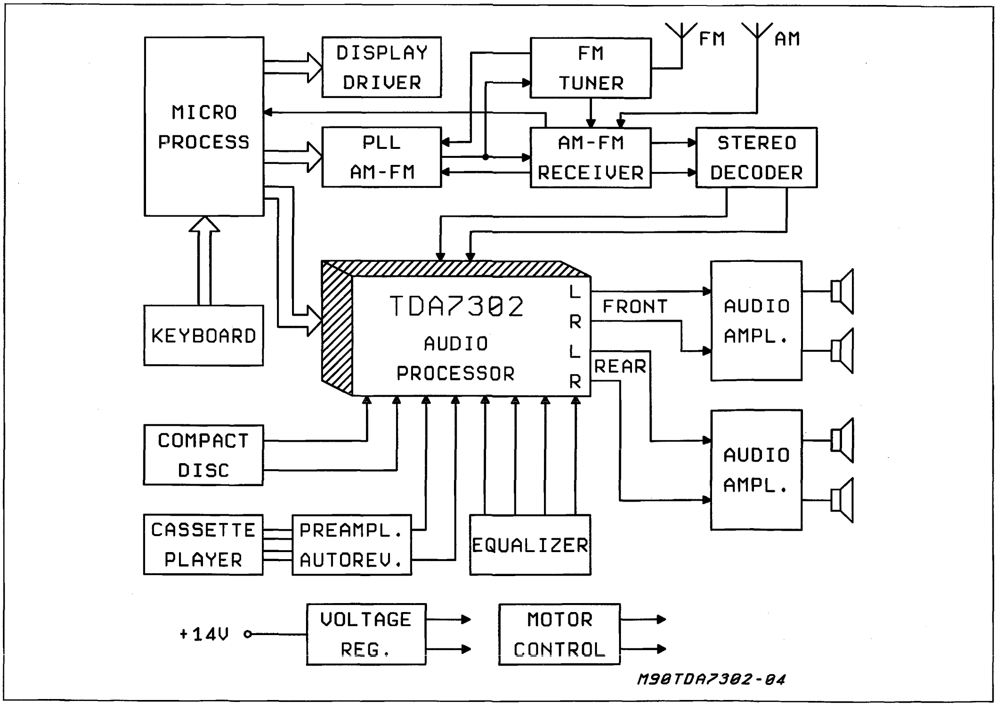
Figure 14: Typical Tone Response



Outputs

A special class-A output amplifier with a modulated sink current provides low distortion and ground compatibility with low current consumption.

Figure 15: Complete Car-Radio System using Digital Controlled Audio Processor



APPLICATION INFORMATION (continued)

SERIAL BUS INTERFACE

S-BUS Interface and I²CBUS Compatibility

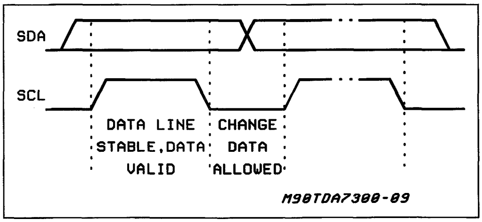
Data transmission from microprocessor to the TDA7302 and viceversa takes place thru the 3-wire S-BUS interface, consisting of the three lines SDA, SCL, SEN. If SDA and SEN inputs are short-circuited together, then the TDA7302 appears as a standard I²CBUS slave.

According to I²CBUS specification the S-BUS lines are connected to a positive supply voltage via pull-up resistors

Data Validity

As shown in fig. 16, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Figure 16: Data Validity on the I²CBUS



Start and Stop Conditions

I²CBUS:
as shown in fig.17 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

S-bus:
the start/stop conditions (points 1 and 6) are detected exclusively by a transition of the SEN line (1 → 0 / 0 →1) while the SCL line is at the HIGH level.

The SDA line is only allowed to change during the time the SCL line is low (points 2, 3, 4, 5). After the start information (point 1) the SEN line returns to the HIGH level and remains unchanged for all the time the transmission is performed.

Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 18). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Figure 17: Timing Diagram of S-BUS and I²CBUS

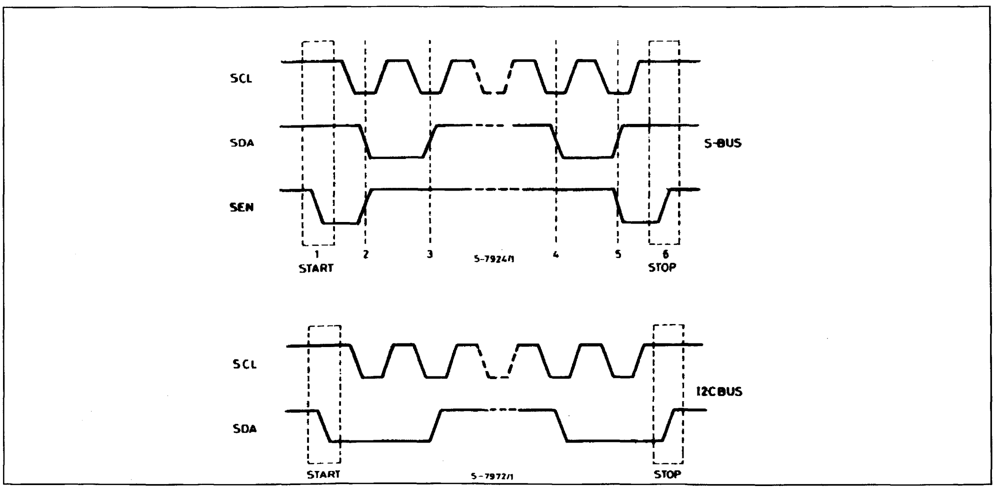
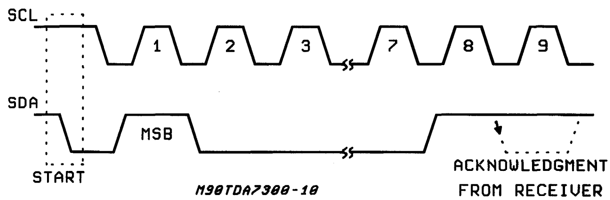


Figure 18: Acknowledge on the I^2CBUS



Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7302 address (the 8th bit of the byte must be 0). The TDA7302 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)

TDA7302 ADDRESS

MSB first byte LSB MSB LSB MSB LSB

S	1	0	0	0	1	0	0	0	ACK				DATA				ACK				DATA				ACK	P

Data Transferred (N-bytes + Acknowledge)

ACK = Acknowledge
S = Start
P = Stop

MAX CLOCK SPEED 100kbits/s

SOFTWARE SPECIFICATION

Chip address (TDA7302 address)

1	0	0	0	1	0	0	0
MSB							LSB

DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	X	X	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

X = don't care
Ax = 2dB steps
Bx = 10dB steps
Cx = 2.5dB steps

Status after power-on reset

STATUS AFTER POWER-ON-RESET

Volume	– 68 dB
Speaker	– 38 dB
Audio Switch	Mono
Bass	+ 2.5 dB
Treble	+ 2.5 dB

SOFTWARE SPECIFICATION (continued)
DATA BYTES (detailed description)

VOLUME

MSB							LSB	
0	0	B2	B1	B0	A2	A1	A0	Volume 2dB Steps
					0	0	0	0
					0	0	1	-2
					0	1	0	-4
					0	1	1	-6
					1	0	0	-8
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
0	0	B2	B1	B0				Volume 10dB STEPS
		0	0	0				+10
		0	0	1				0
		0	1	0				-10
		0	1	1				-20
		1	0	0				-30
		1	0	1				-40
		1	1	0				-50
		1	1	1				-60

For example if you want setting the volume at -32dB the 8 bit string is: 0 0 1 0 0 0 0 1

SPEAKER ATTENUATORS

MSB							LSB	
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-2
					0	1	0	-4
					0	1	1	-6
					1	0	0	-8
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30

For example attenuation of 24dB on speaker RF is given by: 1 0 1 1 0 0 1 0

SOFTWARE SPECIFICATION (continued)

AUDIO SWITCH - Select the input Channel to Activate

MSB							LSB	
0	1	0	X	X	S2	S1	S0	Audio Switch
			X	X	0	0	0	Stereo 1
			X	X	0	0	1	Stereo 2
			X	X	0	1	0	Stereo 3
			X	X	0	1	1	Mute Input
			X	X	1	0	0	Mono
			X	X	1	0	1	Not Allowed
			X	X	1	1	0	Not Allowed
			X	X	1	1	1	Not Allowed

X = don't care

For example to set the stereo 2 channel the 8 bit string must be: 0 1 0 0 0 0 0 1

BASS AND TREBLE - Control Range of ± 15 dB (boost and cut) Steps of 2.5 dB

0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	– 15
				0	0	0	1	– 15
				0	0	1	0	– 12.5
				0	0	1	1	– 10
				0	1	0	0	– 7.5
				0	1	0	1	– 5
				0	1	1	0	– 2.5
				0	1	1	1	– 0
				1	1	1	1	+ 0
				1	1	1	0	+ 2.5
				1	1	0	1	+ 5
				1	1	0	0	+ 7.5
				1	0	1	1	+ 10
				1	0	1	0	+ 12.5
				1	0	0	1	+ 15
				1	0	0	0	+ 15

C3 = Sign

For example Bass at -12.5dB is obtained by the following 8 bit string: 0 1 1 0 0 0 1 0

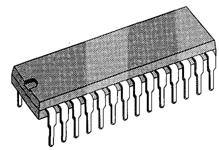
SGS-THOMSON MICROELECTRONICS

TDA7306

DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

ADVANCE DATA

- CONTROL IS ACCOMPLISHED BY MICRO-WIRE/SPI - COMPATIBLE SERIAL BUS INTERFACE
- INPUT AND OUTPUT PINS FOR EXTERNAL EQUALIZER
- THREE STEREO INPUT SOURCE SELECTION PLUS MONO INPUT
- TREBLE, BASS, VOLUME AND BALANCE CONTROL
- FOUR INDEPENDENT SPEAKER CONTROL (FRONT/REAR)
- SINGLE SUPPLY OPERATION
- VERY LOW NOISE AND VERY LOW DISTORTION
- POP FREE SWITCHING



DIP28

ORDERING NUMBER: TDA7306

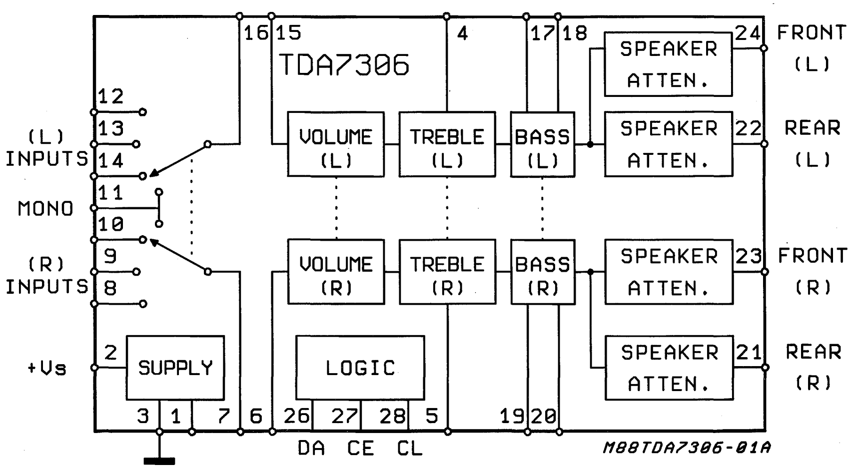
DESCRIPTION

The TDA7306 is a volume, tone (bass and treble), balance (left/right) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi systems.

The AC signal setting is obtained by resistor networks and analog switches combined with operational amplifiers.

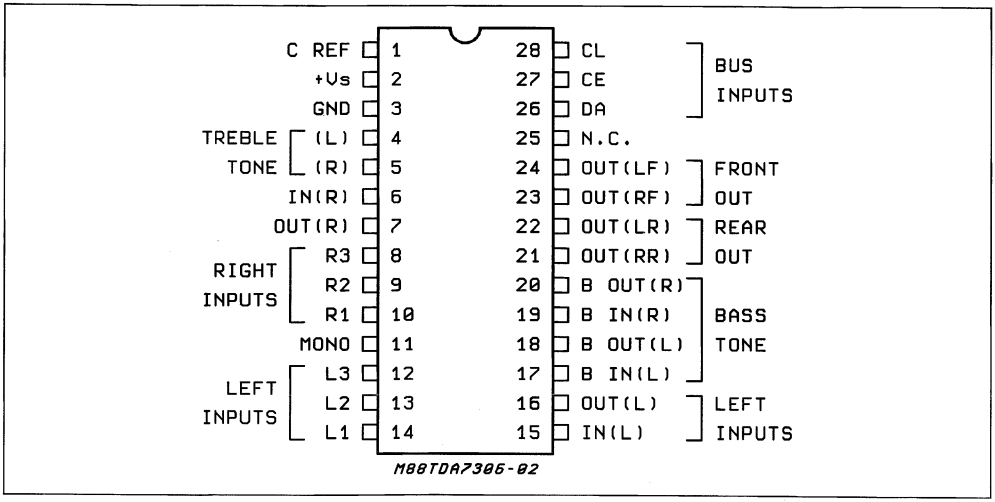
The results are: low noise, low distortion and high dynamic range.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice. notice.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	14	V
P_{tot}	Total Power Dissipation (T_{amb} = 25°C)	2	W
T_{amb}	Operating Ambient Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	65	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 10V , R_L = 10KΩ; R_g = 600Ω , f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	10	14	V
I_S	Supply Current		15	30	40	mA
SVR	Ripple Rejection	f = 300Hz to 10KHz	50	60		dB
INPUT SELECTORS						
R_i	Input Resistance		30	45		KΩ
V_I(DC)	Input DC Voltage		3.5	4.3	5	V
$V_{IN\ MAX}$	Max. Input Signal	GV = 0dB d = 0.3%	1.5	2.0		Vrms
IN_S	Input Separation	f = 1KHz (2)	90	100		dB
		f = 10KHz (2)	70	80		dB
R_L	Output Load Resistance		5			KΩ

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VOLUME CONTROLS						
R_{IN}	Input Resistance		10	18	26	KΩ
	Control Range			78		dB
G_{max}	Max Gain		8	10	12	dB
	Max Attenuation		48	52.4		dB
	Step Resolution			1.6	2.5	dB
	Attenuator Set Error	G_V = -50 to 10dB			2	dB
	Tracking Error				2	dB
SPEAKER ATTENUATORS						
	Control Range		38	41	44	dB
	Step Resolution	see Note (3)				
	Attenuator Set Error				3	dB
	Tracking Error				2	dB
BASS AND TREBLE CONTROL (1)						
	Control Range			±15		dB
	Step Resolution			2.5	3.5	dB
AUDIO OUTPUT						
V_O	Max. Output Voltage	d = 0.3%	1.5	2.2		Vrms
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				1	nF
R_O	Output Resistance			70	150	Ω
V_O(DC)	DC Voltage Level		3	3.8	4.5	V
GENERAL						
e_{NO}	Output Noise	BW = 22Hz to 22KHz, G_V = 0dB		6	15	μV
		BW = 22Hz to 22KHz, Out atten. ≥ 20dB		3.5		μV
		G_v = 0dB Curve A		4		μV
S/N	Signal to Noise Ratio	All gain = 0dB V_O = 1Vrms BW = 22Hz to 22KHz		105		dB
d	Distortion	f = 1KHz; V_O = 1V; G_v = 0		0.01	0.1	%
	Frequency Response (-1dB)	G_v = 0 High Low	20		 20	KHz Hz
S_C	Channnel Separation left/right	f = 1KHz f = 10KHz	90 70	100 80		dB dB
BUS INPUTS						
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage		2.4			V
	Digital Input Current		-5		+5	μA

Notes:
(1) Bass and Treble response see attached diagram. The center frequency and quality of the resonance behaviour can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.
(2) The selected input is grounded thru the 2.2μF capacitor.
(3) See speaker attenuators table on "Software specification".

Figure 1: Application Circuit

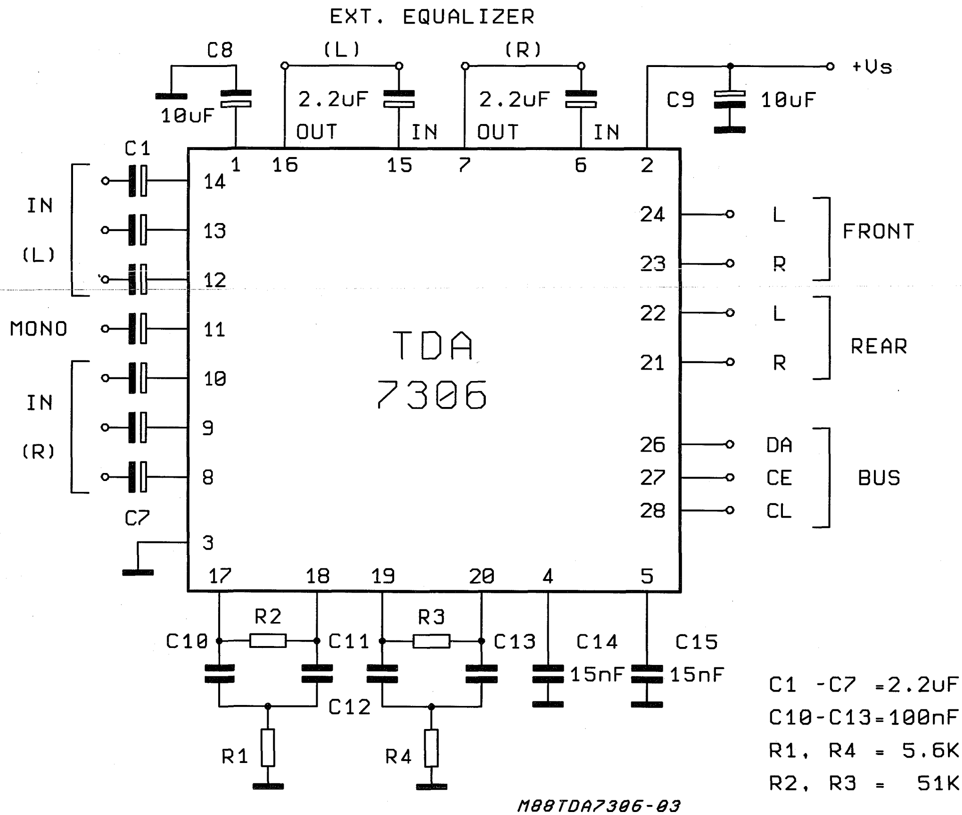


Figure 2: P.C. Board and Components Layout of the Fig.1 (1:1 scale)

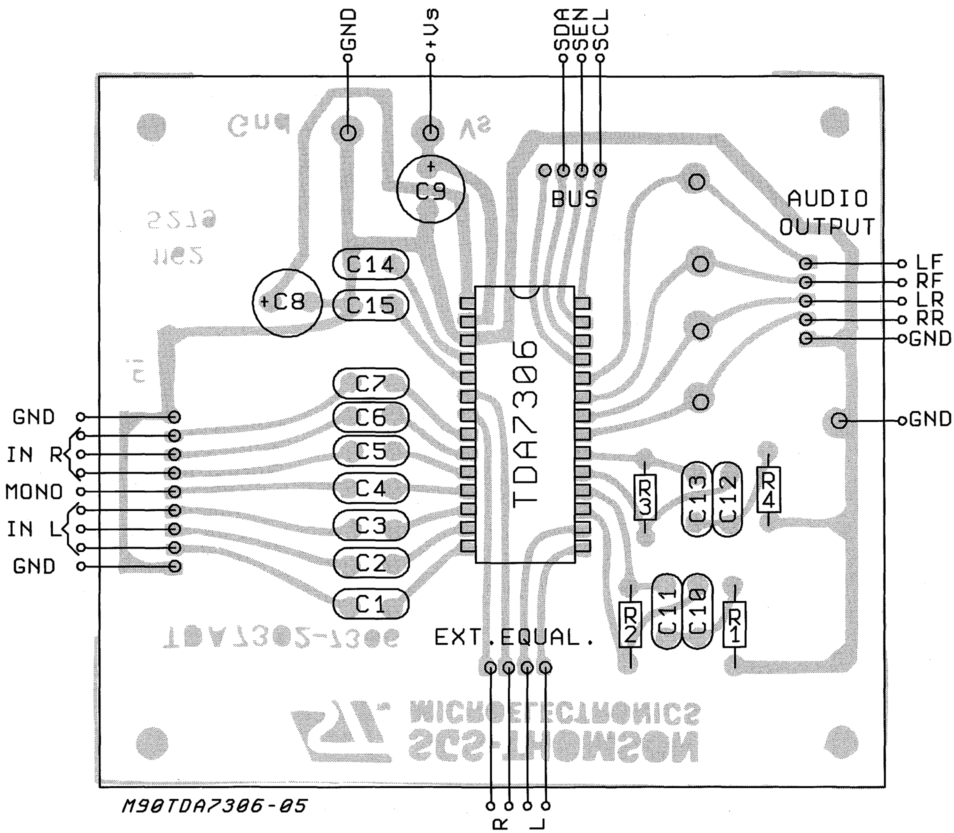


Figure 3: Total Output Noise vs. Volume Setting

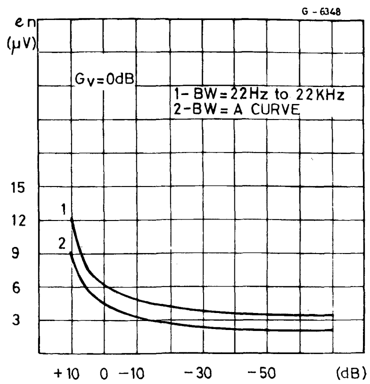


Figure 4: Signal to Noise Ratio vs. Volume Setting

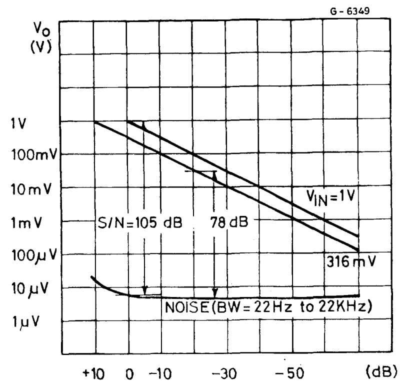


Figure 5: Distortion + Noise vs. Frequency

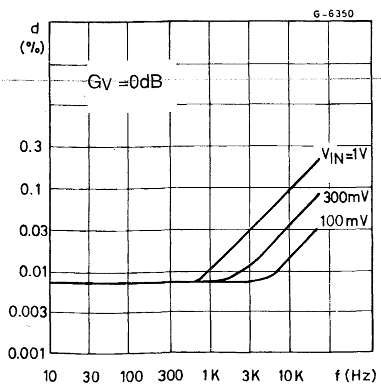


Figure 6: Distortion vs. Output Voltage

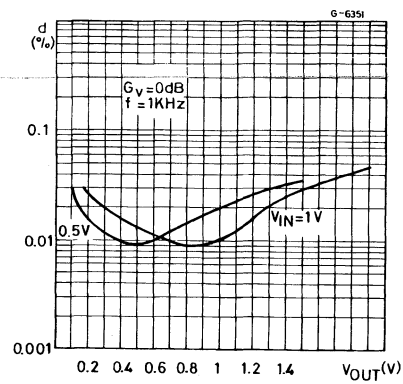


Figure 7: Distortion vs. Load Resistance

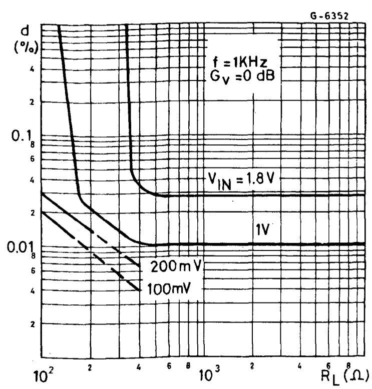


Figure 8: Channel Separation (L1 - R1) vs. Frequency

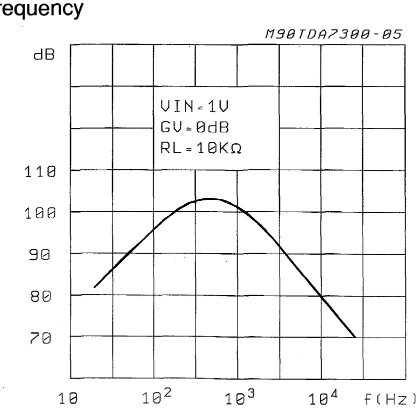


Figure 9: Input Separation (L1 - L2) vs. Frequency

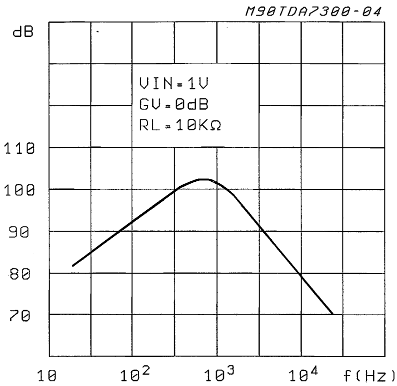


Figure 10: Supply Voltage Rejection vs. Frequency

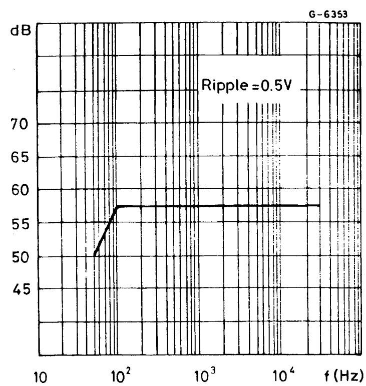
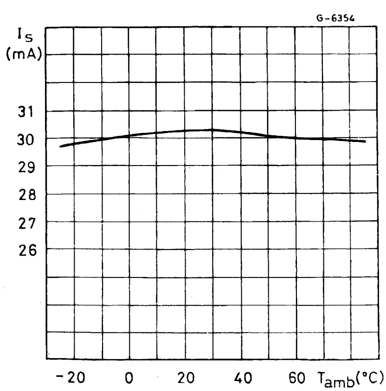


Figure 11: Quiescent Current vs. Temperature

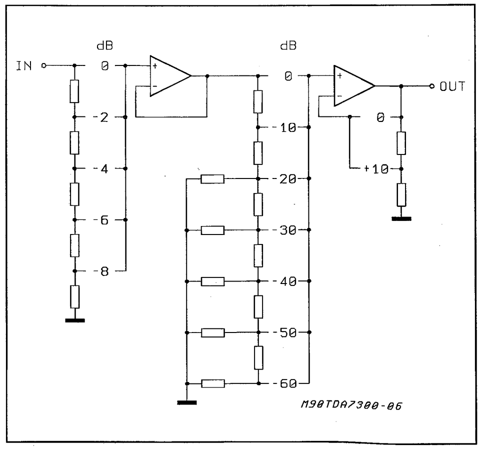


APPLICATION INFORMATION

Volume Control Concept

Traditional electronic volume control circuits use a multiplier technique with all the disadvantages of high noise and distortion.
The used concept, as shown in Fig. 12 with digital switched resistor dividers, provides extremely low noise and distortion. The multiplexing of the resistive dividers is realized with a multiple-input operational amplifier.

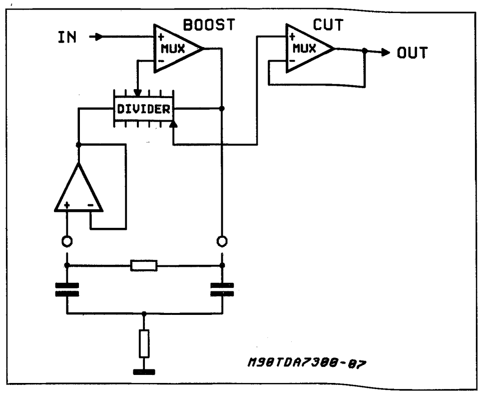
Figure 12: Volume Control



Bass and Treble Control

The principle operation of the bass control is shown in Fig. 13. The external filter together with the internal buffer allows a flexible filter design according to the different requirements in car radios.
The function of the treble is similar to the bass.
A typical curve is shown in Fig.14.

Figure 13: Bass Control



APPLICATION INFORMATION (continued)

Outputs
A special class-A output amplifier with a modulated sink current provides low distortion and ground compatibility with low current consumption.

Figure 14: Typical Tone Response

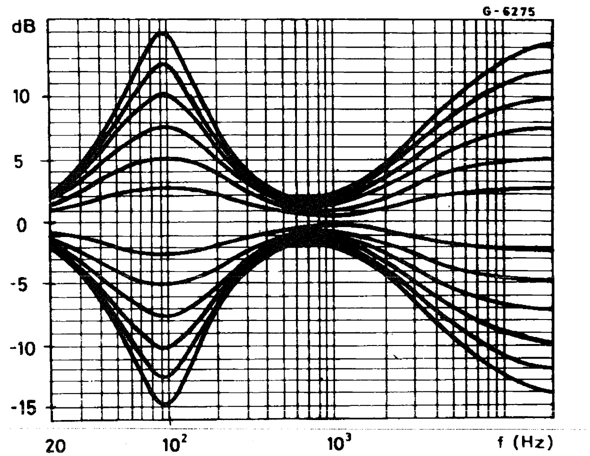
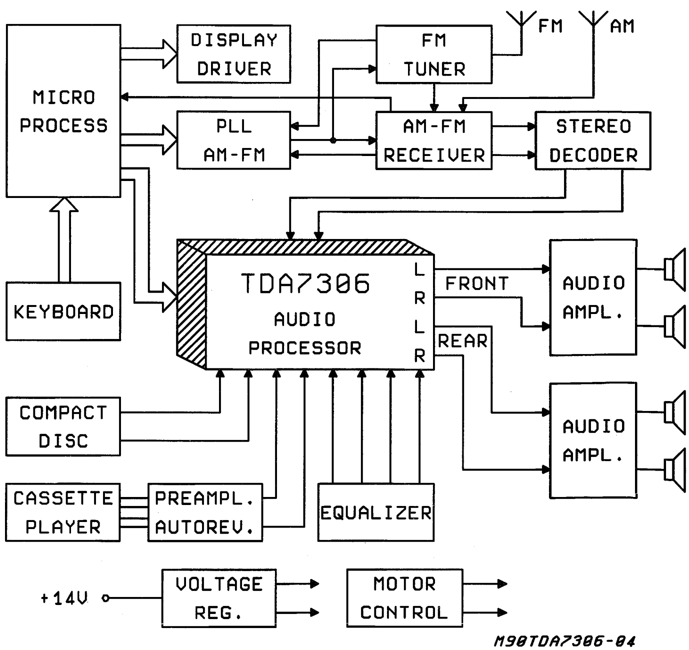


Figure 15: Complete Car-Radio System using Digital Controlled Audio Processor



APPLICATION INFORMATION (continued)

SERIAL BUS INTERFACE

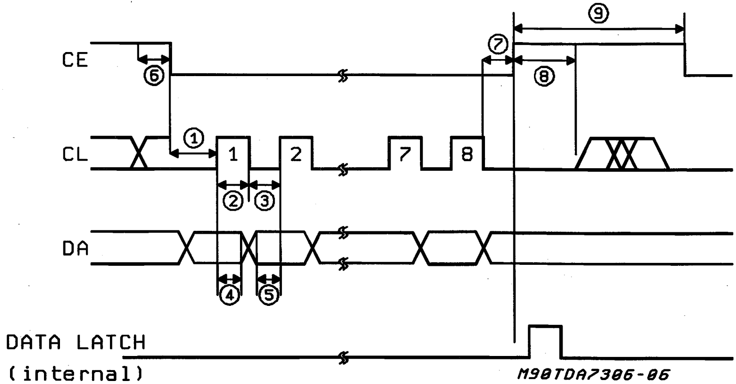
The serial bus interface is compatible to MICRO-WIRE and SPI bus systems.
During the LOW state of the chip enable signal (CE) the data on pin DA are clocked into the shift register at the LOW to HIGH transition of the clock signal CL.

At the LOW to HIGH transition of the CE signal the content of the internal shift register is stored into the addressed latches.

The transmission is separated into bytes with 8 bit according to the data specification of the audio-processor. After every byte a positive slope of the CE signal has to be generated in order to store the data byte.

A special clock counter enables the latch of the data byte only, if exactly 8 clocks were present during the LOW state of the CE signal. This results in a high immunity against spikes on the clock line and avoids a storage of wrong data-bytes.

Figure 16: BUS Timing



Nr.	Parameter	Min.	Max.	Units
	Clock Frequency		250	KHz
1	CE Lead time	4		µs
2	Clock High Time	2		µs
3	Clock Low Time	2		µs
4	Data Hold Time	1.8		µs
5	Data Setup Time	1.8		µs
6	Clock Setup Time	0		µs
7	CE lagtime	0		µs
8	Clock Hold Time	6		µs
9	CE High TIme	6		µs

SOFTWARE SPECIFICATION
DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
0	1	0	X	X	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

X = don't care Ax = 2dB steps Bx = 10dB steps
Cx = 2.5dB steps

STATUS AFTER POWER-ON-RESET

Volume	– 68 dB
Speaker	– 38 dB
Audio Switch	Mono
Bass	+ 2.5 dB
Treble	+ 2.5 dB

VOLUME

MSB							LSB	
0	0	B2	B1	B0	A2	A1	A0	Volume 2dB Steps
					0	0	0	0
					0	0	1	-1.6
					0	1	0	-3.2
					0	1	1	-4.8
					1	0	0	-6.4
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
0	0	B2	B1	B0				Volume 10dB Steps
		0	0	0				+10
		0	0	1				+2
		0	1	0				-8
		0	1	1				-16
		1	0	0				-24
		1	0	1				-32
		1	1	0				-40
		1	1	1				-48

For example if you want setting the volume at -25.6dB the 8 bit string is: 0 0 1 0 0 0 0 1

SPEAKER ATTENUATORS

MSB							LSB	
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-1
					0	1	0	-2
					0	1	1	-4
					1	0	0	-5
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
			0	0				0
			0	1				-6
			1	0				-18
			1	1				-36

For example attenuation of 20dB on speaker RF is given by: 1 0 1 1 0 0 1 0

SOFTWARE SPECIFICATION (continued)

AUDIO SWITCH - Select the input Channel to Activate

MSB							LSB	
0	1	0	X	X	S2	S1	S0	Audio Switch
			X	X	0	0	0	Stereo 1
			X	X	0	0	1	Stereo 2
			X	X	0	1	0	Stereo 3
			X	X	0	1	1	Mute Input
			X	X	1	0	0	Mono
			X	X	1	0	1	Not Allowed
			X	X	1	1	0	Not Allowed
			X	X	1	1	1	Not Allowed

X = don't care

For example to set the stereo 2 channel the 8 bit string must be: 0 1 0 0 0 0 0 1

BASS AND TREBLE - Control Range of ± 15 dB (boost and cut) Steps of 2.5 dB

0	1	1	0	C3	C2	C1	C0	Bass
0	**1**	**1**	**1**	**C3**	**C2**	**C1**	**C0**	**Treble**
				0	0	0	0	– 15
				0	0	0	1	– 15
				0	0	1	0	– 12.5
				0	0	1	1	– 10
				0	1	0	0	– 7.5
				0	1	0	1	– 5
				0	1	1	0	– 2.5
				0	1	1	1	– 0
				1	1	1	1	+ 0
				1	1	1	0	+ 2.5
				1	1	0	1	+ 5
				1	1	0	0	+ 7.5
				1	0	1	1	+ 10
				1	0	1	0	+ 12.5
				1	0	0	1	+ 15
				1	0	0	0	+ 15

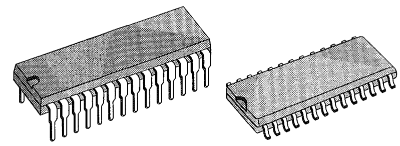
C3 = Sign

For example Bass at -12.5dB is obtained by the following 8 bit string: 0 1 1 0 0 0 1 0

DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

ADVANCE DATA

- INPUT MULTIPLEXER:
  - 4 STEREO INPUTS
  - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTION TO DIFFERENT SOURCES
- INPUT AND OUTPUT FOR EXTERNAL EQUALIZER OR NOISE REDUCTION SYSTEM
- VOLUME CONTROL IN 1.25dB STEPS
- TREBLE AND BASS CONTROL
- FOUR SPEAKER ATTENUATORS:
  - 4 INDEPENDENT SPEAKERS CONTROL IN 1.25dB STEPS FOR BALANCE AND FADER FACILITIES
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL I²C BUS



DIP28 **SO28**

ORDERING NUMBERS:
TDA7318 TDA7318D

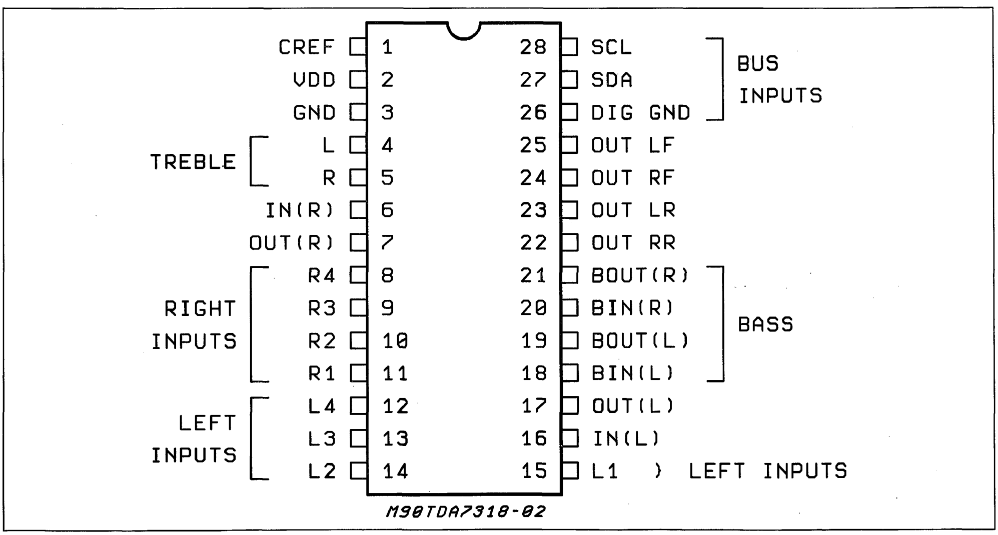
DESCRIPTION

The TDA7318 is a volume, tone (bass and treble) balance (Left/Right) and fader (front/rear) processor for quality audio applications in car radio and Hi-Fi systems.

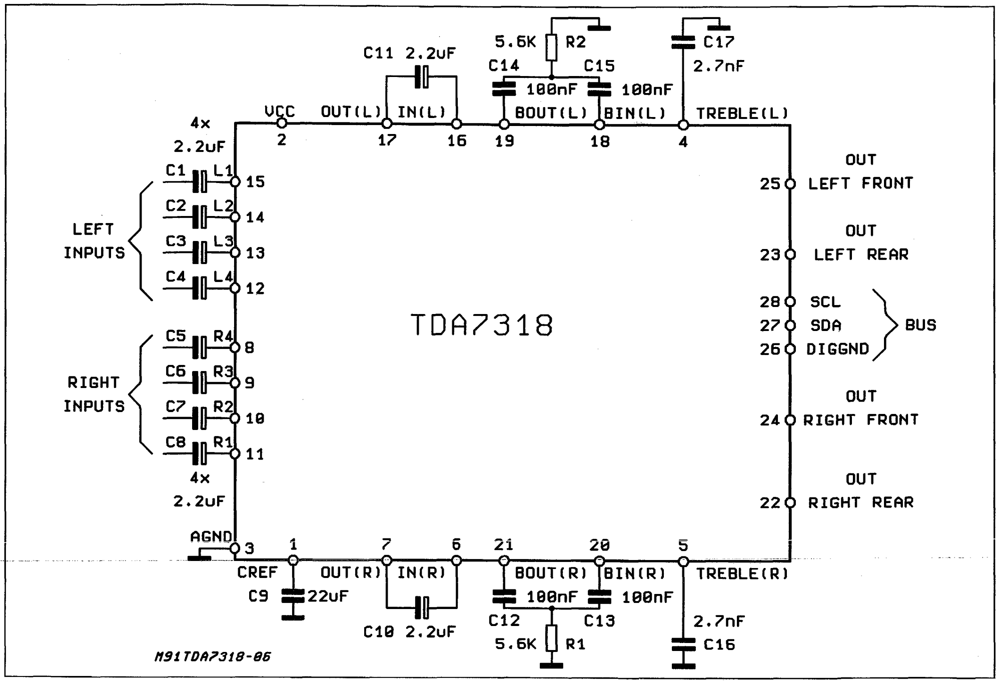
Selectable input gain is provided. Control is accomplished by serial I²C bus microprocessor interface. The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Tecnology, Low Distortion, Low Noise and Low DC stepping are obtained.

PIN CONNECTION (Top view)



TEST CIRCUIT



THERMAL DATA

Symbol	Description		SO28	DIP28	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	max	85	65	°C/W

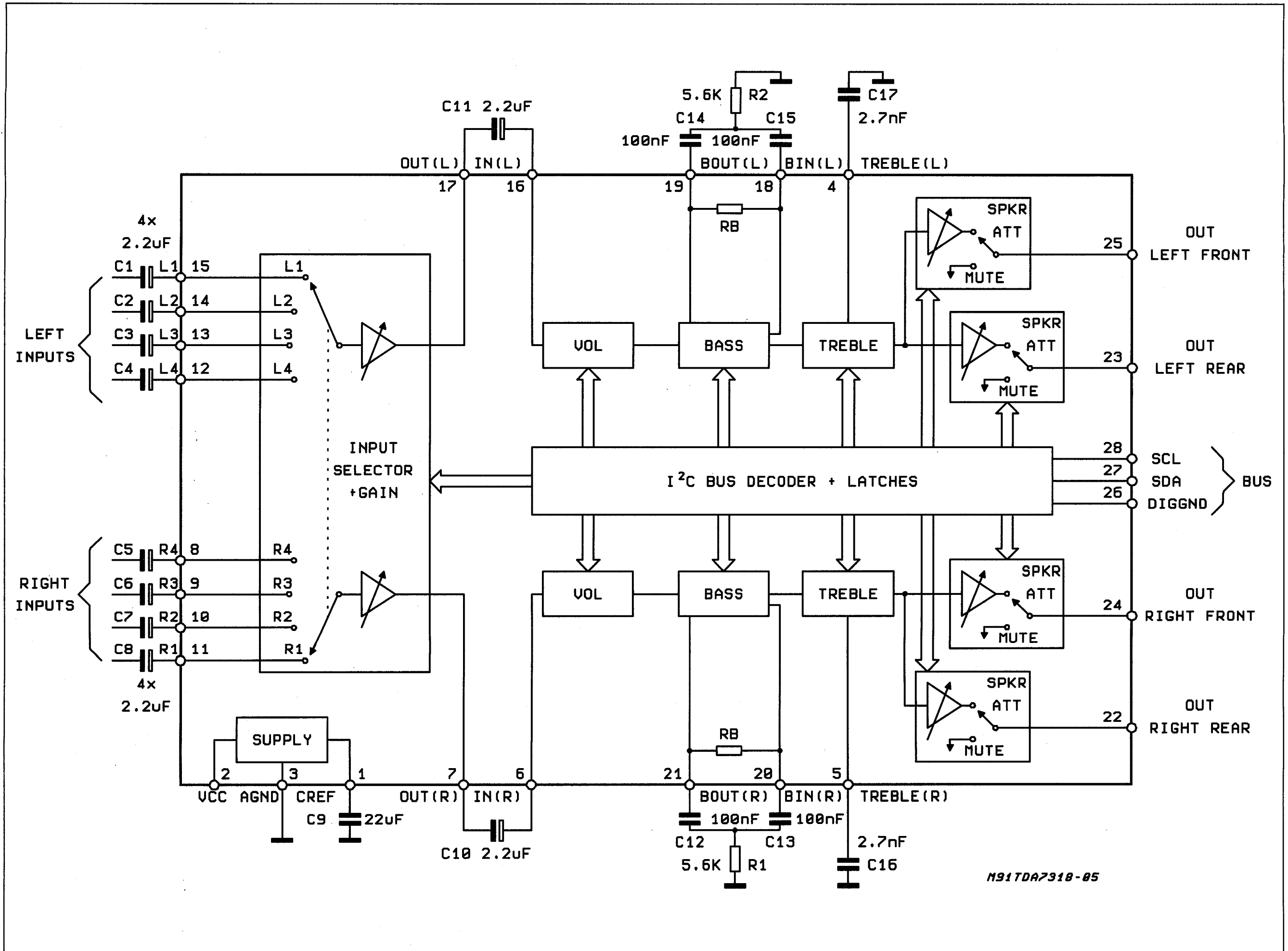
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.2	V
T_{amb}	Operating Ambient Temperature	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	6	9	10	V
V_{CL}	Max. input signal handling	2			Vrms
THD	Total Harmonic Distortion V = 1Vrms f = 1KHz		0.01	0.1	%
S/N	Signal to Noise Ratio		106		dB
S_C	Channel Separation f = 1KHz		103		dB
	Volume Control 1.25dB step	-78.75		0	dB
	Bass and Treble Control 2db step	-14		+14	dB
	Fader and Balance Control 1.25dB step	-38.75		0	dB
	Input Gain 6.25dB step	0		18.75	dB
	Mute Attenuation		100		dB

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (refer to the test circuit T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ, R_G = 600Ω, all controls flat (G = 0), f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	9	10	V
I_S	Supply Current		4	8	11	mA
SVR	Ripple Rejection		60	85		dB
INPUT SELECTORS						
R_{II}	Input Resistance	Input 1, 2, 3, 4	35	50	70	KΩ
V_{CL}	Clipping Level		2	2.5		Vrms
S_{IN}	Input Separation (2)		80	100		dB
R_L	Output Load resistance	pin 7, 17	2			KΩ
G_{INmin}	Min. Input Gain		-1	0	1	dB
G_{INmax}	Max. Input Gain		17	18.75	20	dB
G_{STEP}	Step Resolution		5	6.25	7.5	dB
e_{IN}	Input Noise	G = 18.75dB		2		μV
V_{DC}	DC Steps	adjacent gain steps		4	20	mV
		G = 18.75 to Mute		4		mV
VOLUME CONTROL						
R_{IV}	Input Resistance		20	33	50	kΩ
C_{RANGE}	Control Range		70	75	80	dB
A_{VMIN}	Min. Attenuation		-1	0	1	dB
A_{VMAX}	Max. Attenuation		70	75	80	dB
A_{STEP}	Step Resolution		0.5	1.25	1.75	dB
E_A	Attenuation Set Error	Av = 0 to -20dB Av = -20 to -60dB	-1.25 -3	0	1.25 2	dB dB
E_T	Tracking Error				2	dB
V_{DC}	DC Steps	adjacent attenuation steps From 0dB to Av max		0 0.5	3 7.5	mV mV
SPEAKER ATTENUATORS						
C_{range}	Control Range		35	37.5	40	dB
S_{STEP}	Step Resolution		0.5	1.25	1.75	dB
E_A	Attenuation set error				1.5	dB
A_{MUTE}	Output Mute Attenuation		80	100		dB
V_{DC}	DC Steps	adjacent att. steps from 0 to mute		0 1	3 10	mV mV
BASS CONTROL (1)						
Gb	Control Range	Max. Boost/cut	±12	±14	±16	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		34	44	58	KΩ
TREBLE CONTROL (1)						
Gt	Control Range	Max. Boost/cut	±13	±14	±15	dB
T_{STEP}	Step Resolution		1	2	3	dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
AUDIO OUTPUTS						
V_{OCL}	Clipping Level	d = 0.3%	2	2.5		Vrms
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				10	nF
R_{OUT}	Output resistance		30	75	120	Ω
V_{OUT}	DC Voltage Level		4.2	4.5	4.8	V
GENERAL						
e_{NO}	Output Noise	BW = 20-20KHz, flat output muted all gains = 0dB		2.5 5	 15	µV µV
		A curve all gains = 0dB		3		µV
S/N	Signal to Noise Ratio	all gains = 0dB; V_O = 1Vrms		106		dB
d	Distortion	A_V = 0, V_{IN} = 1Vrms A_V = -20dB V_{IN} = 1Vrms V_{IN} = 0.3Vrms		0.01 0.09 0.04	0.1 0.3	% % %
Sc	Channel Separation left/right		80	103		dB
	Total Tracking error	A_V = 0 to -20dB -20 to -60 dB		0 0	1 2	dB dB
BUS INPUTS						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current		-5		+5	µA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V

Notes:

(1) Bass and Treble response see attached diagram (fig.19). The center frequency and quality of the resonance behaviour can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network

(2) The selected input is grounded thru the 2.2µF capacitor.

Figure 1: Noise vs. Volume/Gain Settings

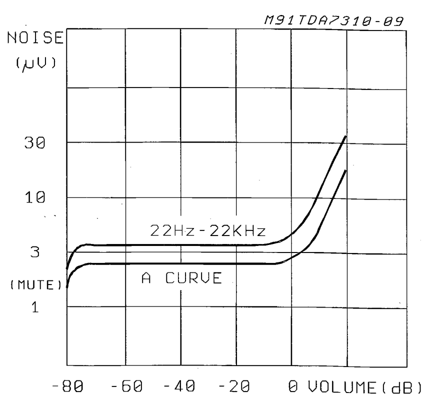


Figure 2: Signal to Noise Ratio vs. Volume Setting

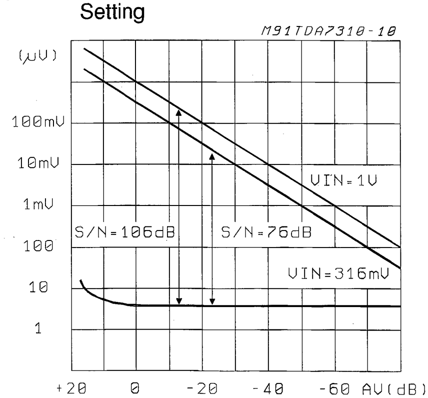


Figure 3: Distortion & Noise vs. Frequency

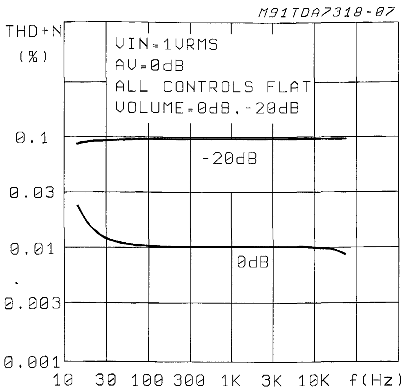


Figure 4: Distortion & Noise vs. Frequency

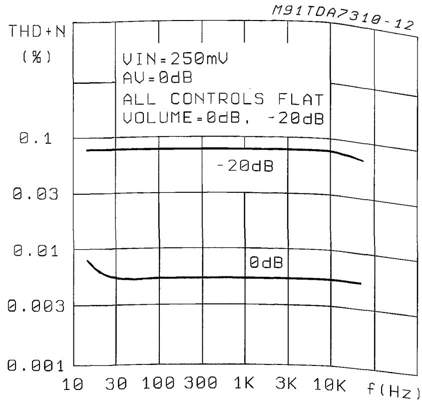


Figure 5: Distortion vs. Load Resistance

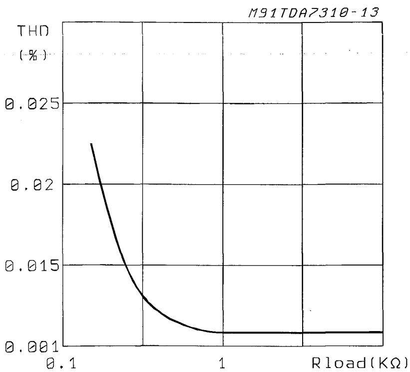


Figure 6: Channel Separation (L → R) vs. Frequency

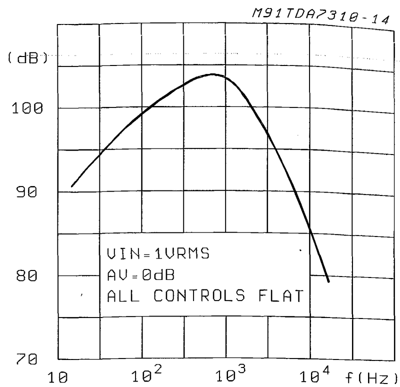


Figure 7: Input Separation (L1 → L2, L3, L4) vs. Frequency

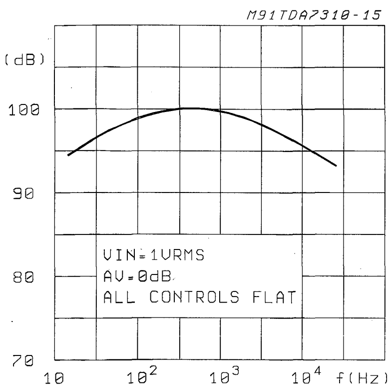


Figure 8: Supply Voltage Rejection vs. Frequency

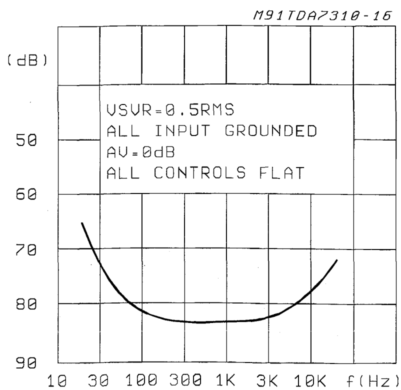


Figure 9: Output Clipping Level vs. Supply Voltage

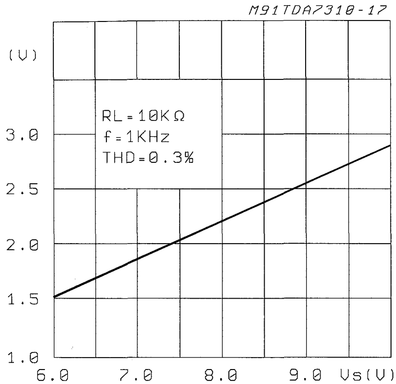


Figure 10: Quiescent Current vs. Supply Voltage

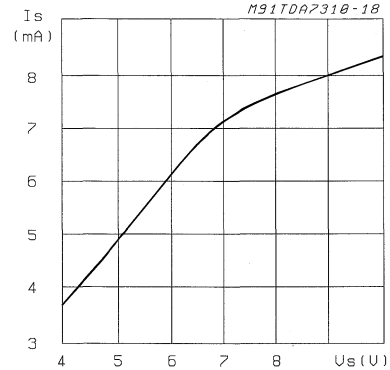


Figure 11: Supply Current vs. Temperature

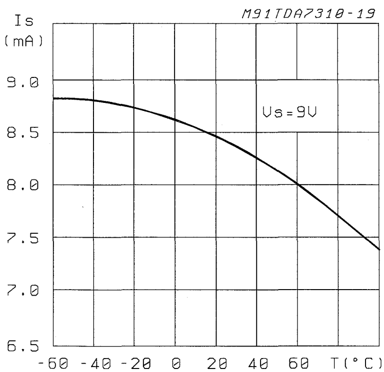


Figure 12: Bass Resistance vs. Temperature

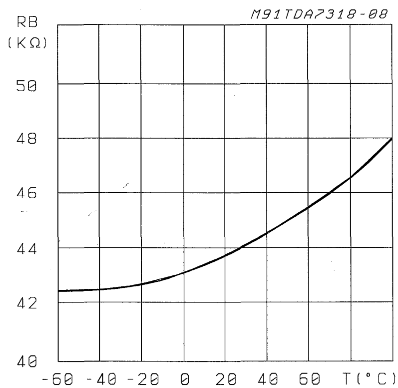
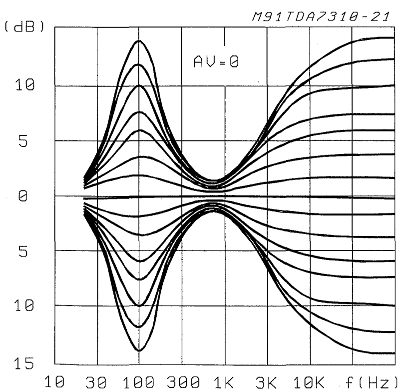


Figure 13: Typical Tone Response (with the ext. components indicated in the test circuit)



I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7318 and viceversa takes place thru the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

Data Validity

As shown in fig. 14, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.15 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 16). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Figure 14: Data Validity on the I²CBUS

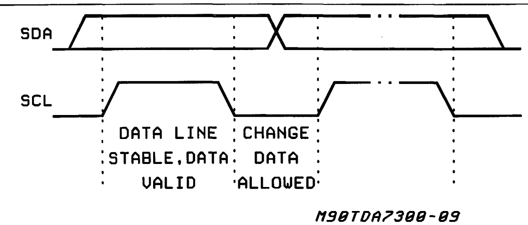


Figure 15: Timing Diagram of I²CBUS

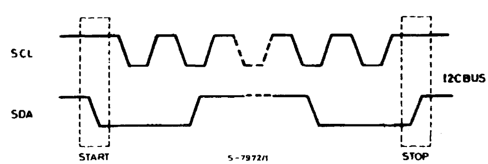
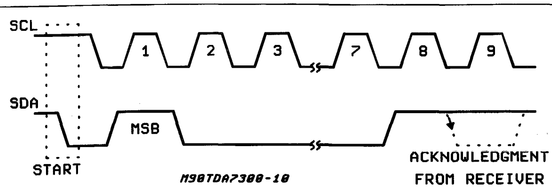


Figure 16: Acknowledge on the I²CBUS



SOFTWARE SPECIFICATION

Interface Protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7318 address (the 8th bit of the byte must be 0). The TDA7318 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)

TDA7318 ADDRESS

MSB first byte LSB | MSB LSB | MSB LSB

S	1	0	0	0	1	0	0	0	ACK				DATA				ACK				DATA				ACK	P

Data Transferred (N-bytes + Acknowledge)

ACK = Acknowledge
S = Start
P = Stop

MAX CLOCK SPEED 100kbits/s

SOFTWARE SPECIFICATION

Chip address

1 MSB	0	0	0	1	0	0	0 LSB

DATA BYTES

MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	G1	G0	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

Ax = 1.25dB steps; Bx = 10dB steps; Cx = 2dB steps; Gx = 6.25dB steps

SOFTWARE SPECIFICATION (continued)

DATA BYTES (detailed description)

Volume

MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

For example a volume of -45dB is given by:

0 0 1 0 0 1 0 0

Speaker Attenuators

MSB							LSB	FUNCTION
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

For example attenuation of 25dB on speaker RF is given by:

1 0 1 1 0 1 0 0

Audio Switch

MSB							LSB	FUNCTION
0	1	0	G1	G0	S2	S1	S0	Audio Switch
					0	0	0	Stereo 1
					0	0	1	Stereo 2
					0	1	0	Stereo 3
					0	1	1	Stereo 4
					1	0	0	Not allowed
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
			0	0				+18.75dB
			0	1				+12.5dB
			1	0				+6.25dB
			1	1				0dB

For example to select the stereo 2 input with a gain of +12.5dB the 8bit string is:
0 1 0 0 1 0 0 1

Bass and Treble

0 0	1 1	1 1	0 1	C3 C3	C2 C2	C1 C1	C0 C0	Bass Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

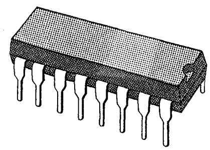
C3 = Sign
For example Bass at -10dB is obtained by the following 8 bit string:
0 1 1 0 0 0 1 0

TDA7326

AM-FM RADIO FREQUENCY SYNTHESIZER

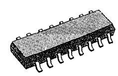
ADVANCE DATA

- FM INPUT AND PRECOUNTER FOR UP TO 160MHz
- AM INPUT FOR UP TO 32MHz
- 6-BIT SWALLOW COUNTER, 8-BIT PROGRAMMABLE COUNTER FOR FM AND SW
- 14-BIT PROGRAMMABLE COUNTER FOR LW AND MW
- ASYNCHRONOUS 8-BIT SERIAL INTERFACE
- ON-CHIP REFERENCE OSCILLATOR AND COUNTER
- PROGRAMMABLE SCANNING STEPS FOR AM AND FM
- DIGITAL PHASE DETECTOR
- ON-CHIP LOOP FILTER
- TWO SEPARATE FREE PROGRAMMABLE FILTER APPLICATIONS AVAILABLE
- TUNING VOLTAGE OUTPUT 0.5 TO 9V
- PROGRAMMABLE CURRENT SOURCES TO SET THE LOOP GAIN
- ON-CHIP POWER ON RESET
- STANDBY MODE
- SWITCH OUTPUT



DIP16
(Plastic Package)

ORDER CODE : TDA7326



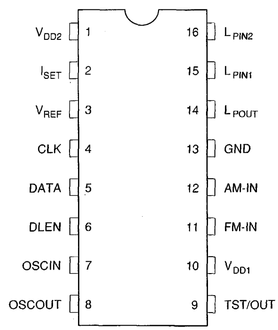
SO-16L
(Plastic Package)

ORDER CODE : TDA7326D

DESCRIPTION

The TDA7326 is a PLL frequency synthesizer in CMOS technology that performs all the function of a PLL radio tuning system for FM and AM (LW, MW, SW).

PIN CONNECTIONS



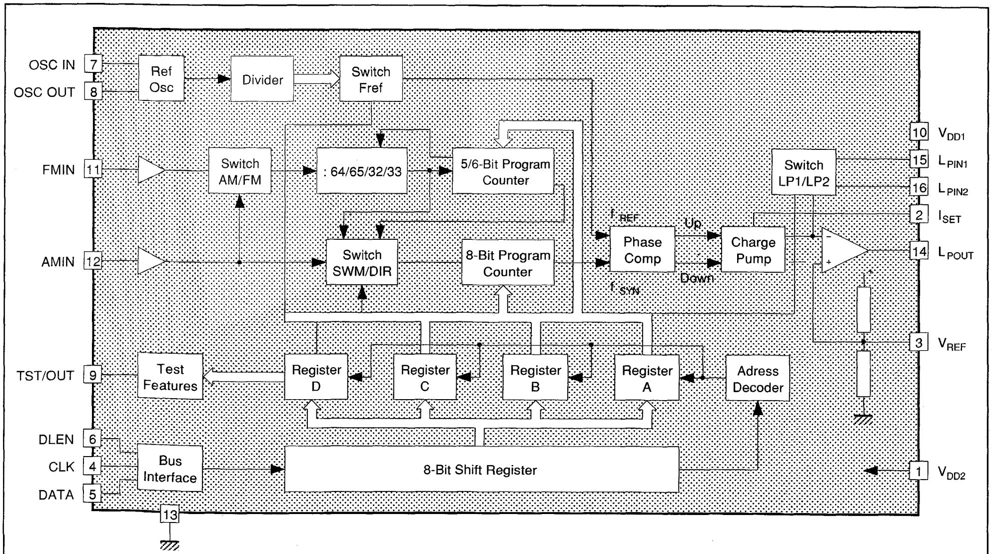
91DSTDA7326-01

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN FUNCTIONS

Number	Name	Function
1	V_{DD2}	Positive Power Supply for Loop Filter (9V)
2	I_{SET}	Current Adjust for the Charge Pump
3	V_{REF}	Reference Voltage for Comparator
4	CLK	Bus Interface
5	DATA	Bus Interface
6	DLEN	Bus Interface
7	OSCIN	Oscillator Input
8	OSCOUT	Oscillator Output
9	TST/OUT	Port Output and Test Input Output
10	V_{DD1}	Positive Power Supply for Logic (5V)
11	FM-IN	FM Oscillator Input
12	AM-IN	AM Oscillator Input
13	GND	Negative Power Supply
14	LPOUT	Loop Filter Output
15	LPIN1	Loop Filter Input 1
16	LPIN2	Loop Filter Input 2

BLOCK DIAGRAM



91DSTDA7326-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD1} - V_{SS}	Supply Voltage	- 0.3 to + 7	V
V_{DD2} - V_{SS}	Supply Voltage	- 0.3 to + 12	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3	V
I_{IN}	Input Current	- 10 to + 10	mA
I_{OUT}	Output Current	- 10 to + 10	mA
P_D	Power Dissipation	150	mW
T_{stg}	Storage Temperature	- 55 to + 125	°C
T_A	Ambient Temperature	-40 to + 85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD1} - V_{SS} = 5V, V_{DD2} - V_{SS} = 9V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD1}	Supply Voltage		4.5	5	5.5	V
V_{DD2}	Supply Volatge				10	V
I_{DD1}	Supply Current	• f_{OSC} = 4MHz no output load FM = 100MHz		15	20	mA
		• f_{OSC} = 4MHz no output load		6	10	mA
		• Standby mode			1	µA
I_{DD2}	Supply Current	R_{ISET} = 22kΩ		2	3	mA
RF INPUTS						
$f_{i\ AM}$	Input Frequency AM	Sinus	0.5		32	MHz
$f_{i\ FM}$	Input Frequency FM	Sinus	30		160	MHz
$V_{i\ AM}$	Input Voltage AM	0.6 to 16MHz (Sinus)	20		600	mV_{RMS}
$V_{i\ FM}$	Input Voltage FM	70 to 120MHz (Sinus)	30		600	mV_{RMS}
Z_{IN}	Input Impedance AM	f_{IN} = 12MHz		1400		Ω
Z_{IN}	Input Impedance FM	f_{IN} = 120MHz		200		Ω
OSCILLATOR						
f_{OSC}	Oscillation Frequency			4		MHz
t_{bu}	Built up Time	Euro-quartz ITT			100	ms
C_{IN}	Internal Capacity			9		pF
C_{OUT}	Internal Capacity			9		pF
Z_{IN}	Input Impedance	f_{OSC} = 4MHz		4		kΩ
POWER ON RESET						
t_{RISE}	Supply Rise Time	10% to 90%	0.01			ms
V_{ton}	Trigger Level On		1.4	0.9		V
V_{toff}	Trigger Level Off				3.5	V

ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25^oC$, $V_{DD1} - V_{SS} = 5V$, $V_{DD2} - V_{SS} = 9V$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PLL CHARACTERISTICS						
f_{STEP}	Step Width AM	f_{OSC} = 4MHz		1/2.5		kHz
f_{STEP}	Step Width FM	f_{OSC} = 4MHz		12.5/25		kHz
f_{REF}	Reference Frequency AM	f_{OSC} = 4MHz		1/2.5		kHz
f_{REF}	Reference Frequency FM	f_{OSC} = 4MHz		12.5/25		kHz
BUS INTERFACE INPUT						
$- I_{IL}$	Input Leakage Current	$V_{IN} = V_{SS}$	- 10		+ 10	µA
I_{IH}	Input Leakage Current	$V_{IN} = V_{DD}$	- 10		+ 10	µA
V_{IH}	High Input Voltage	Leading edge	3.4			V
V_{IL}	Low Input Voltage	Trailing edge			1.6	V
TRANSFER TIME (see Figure 4) Waiting Time						
t_1	CLK to DLEN		0.2			µs
t_3	DATA to CLK		0.1			µs
t_5	DATA to CLK		0.4			µs
Data Repetition Time						
t_r			0.1			ms
Setup Time						
t_2	DLEN to CLK		1			µs
Hold Time						
t_4	CLK to DATA		0			µs
t_6	CLK to DLEN		0.4			µs
$t_{PH} = t_{PL}$	Pulse Width CLK		1			µs
LOOP FILTER INPUT						
$- I_{IN}$	Input Leakage Current	$V_{IN} = V_{SS}$, P_{DOUT} = tristate	- 0.1		+ 0.1	µA
I_{IN}	Input Leakage Current	$V_{IN} = V_{DD}$, P_{DOUT} = tristate	- 0.1		+ 0.1	µA
LOOP FILTER OUTPUT						
V_O	Output Voltage	I = 0.2mA, V_{DD2} = 10V	0.5		9	V

GENERAL DESCRIPTION

This circuit contains a frequency synthesizer and a loop filter for an FM and AM radio tuning system. Only a V_{CO} is required to build a complete PLL system.
A small signal of the AM and FM V_{CO} can be accepted by the circuit.
For FM and SW application, the counter works in a two stages configuration.
The first stage is a swallow counter with a four modulus (:32/33/64/65) precounter.
The second stage is an 8-bit programmable counter.
For LW and MW application, a 14-bit programmable counter is available.
The circuit receives the scalling factors for the programmable counters and the values of the reference frequencies via a three line serial bus interface.
The reference frequency is generated by a 4MHz XTAL oscillator followed by the reference divider.
The reference- and step-frequency is 1 or 2.5kHz for AM.
For FM mode a step frequency of 12.5 and 25kHz can be selected.
The circuit checks the format of the received data words.
Valid data in the interface shift register are stored automatically in buffer registers at the end of transmission.

GENERAL DESCRIPTION (continued)

The output signals of the phase detector switch the programmable current sources.
Their currents are integrated in the loop filter to a DC voltage.
The values of the current sources are programmable by two bits also received via the serial bus.
The loop filter amplifier is supplied by a separate positive power supply, to minimize the noise induced by the digital part of the system.
The loop gain can be set for different conditions.
After a power on reset, all registers are reset to zero and the standby mode is activated.
In standby mode, oscillator, reference counter, AM input and FM input are stopped. The power consumption is reduced to a minimum.

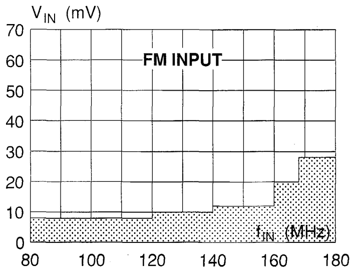
DETAILED DESCRIPTION OF THE PLL FREQUENCY SYNTHESIZER

1. Input Amplifiers

Signals applied on AM and FM input are amplified to get logic level in order to drive the frequency dividers.

Typical input impedance : for FM input is 200Ω and AM input is 1.5kΩ.
Input sensitivity (see Figures 1a and 1b).

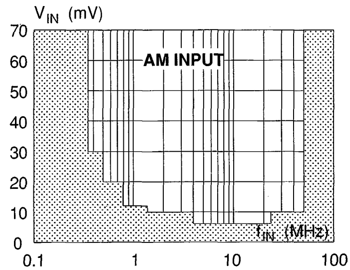
Figure 1a



Input Sensitivity FM

91DSTDA7326-03A

Figure 1b



Input Sensitivity AM

91DSTDA7326-03B

2. Register Organisation

2.1. REGISTER LOCATION

The data registers (bit2...bit7) for the control register and the data registers PC0...PC7, SW0...SW5 for the counters are organized in four words, identified by two address bits (bit0 and bit1), bit0 is the first bit to be send by the controller, bit7 is the last one. The order and the number of the bytes to be transmitted is free selectable. The modification of the PC0...PC7 registers is valid for the internal counters only after transmission of bite4 (SW0...SW5).

byte	MSB - bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	LSB - bit 7
	adr 0	adr 1	data 0	data 1	data 2	data 3	data 4	data 5
byte 1	0	0	test 0	test 1	test 2	SOUT	CURR2	f_{REF}
byte 2	0	1	PC7	PC6	LPF1/2	CURR1	SWM/DIR	AM/FM
byte 3	1	0	PC5	PC4	PC3	PC2	PC1	PC0
byte 4	1	1	SW5	SW4	SW3	SW2	SW1	SW0

2.2 CONTROL AND STATUS REGISTERS

Register Name	Function	Location (byte - bit)
SWM/DIR	Swallow-, direct-mode switch	2 - 6
AM/FM	AM-, FM-band switch	2 -7
f_{REF}	Selection of reference frequency	1 - 7
CURR1	Current select of charge pump	2 - 5
CURR2	Current select of charge pump	1 - 6
LPF1/LPF2	Loop filter input select	2 - 4
SOUT	Switch output condition	1 - 5

3. Divider from V_{CO} Frequency to Reference Frequency

This divide provides a low frequency f_{SYN} which is phase compared with the reference frequency f_{REF}.

3.1 OPERATING MODE

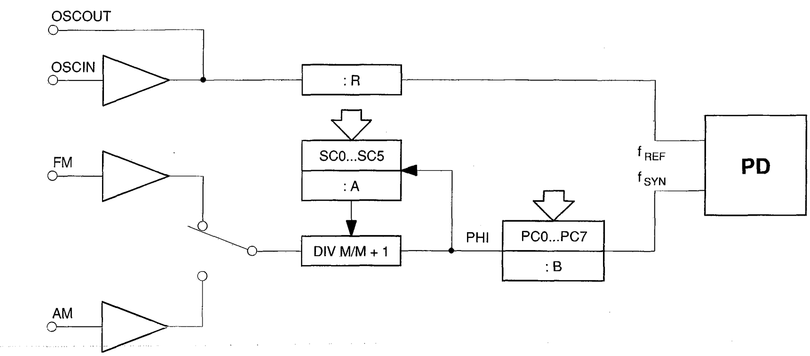
Four operating modes are available : FM mode, AM swallow mode, AM direct mode, standby mode.

They are user programmable with the SWR/DIR and AM/FM registers.

Standby mode : all functions are stopped. This allows low current consumption without lost of information in all registers.

3.2 FM AND AM (SW) OPERATION (SWALLOW MODE)

Figure 2



REGISTER STATUS / FUNCTION

CURR1	CURR2	I_{CHARGE} (ratio)
0	0	1
1	0	100
1	1	60
0	1	40

REGISTER STATUS / FUNCTION

f_{REF}	SWM /DIR	AM/FM	MODE	f_{REF} freq
X	0	0	STOP	0
0	1	1	SW	1k
1	1	1	SW	2.5k
0	1	0	FM	12.5k
1	1	0	FM	25k

REGISTER STATUS / FUNCTION

TEST0	TEST1	TEST2	TST/OUT PIN	OSCIN PIN
0	0	0	SOUT	OSC
1	0	0	f_{REF} OUT	OSC
0	1	0	PHI IN	f_{REF} IN
1	1	0	f_{SYN} OUT	f_{REF} IN
0	0	1	f_{SYN} IN	OSC

91DSTDA7326-04

The FM or AM signal is applied to a four modulus : 32/33/64/65 high speed prescaler, which is controlled by a 6 bit divider 'A'. This divider is controlled by the 6 bit SC register. In parallel the output of the prescaler is connected to a 8 bit divider 'B'. This divider is controlled by the 8 bit PC register. For FM mode with 25kHz reference frequency operation, the divider A is a 5 bit divider. The high speed prescaler is working in : 32/33 dividing mode. Bit 6 of the SC register has to kept to "0".

Dividing range calculation :

For FM mode with 12.5kHz reference frequency and SW swallow mode operation :

$f_{VCO} = [\ 65 \cdot A_1 + (B_1 + 1 - A_1) \cdot 64\ ] . f_{REF}$ or

$f_{VCO} = (64 \cdot B_1 + A_1 + 64) \cdot f_{REF}$

Important : For correct operation $B \geq 64$ and $B \geq A$.

At FM mode with 25kHz reference frequency :

$f_{VCO} = [\ 33 \cdot A_2 + (B_2 + 1 - A_2) \cdot 32\ ] \cdot f_{REF}$

$f_{VCO} = (32 \cdot B_2 + A_2 + 32) \cdot f_{REF}$

Important : For correct operation $B \geq 32$ and $B \geq A$.

A and B are variable values of the dividers.

To keep the actual tuning frequency after a modification of the reference frequency, the values of the dividers have to be modified in the following way.

Switching from 25kHz to 12.5kHz reference frequency : $B_1 = B_2$, $A_1 = A_2 \cdot 2$

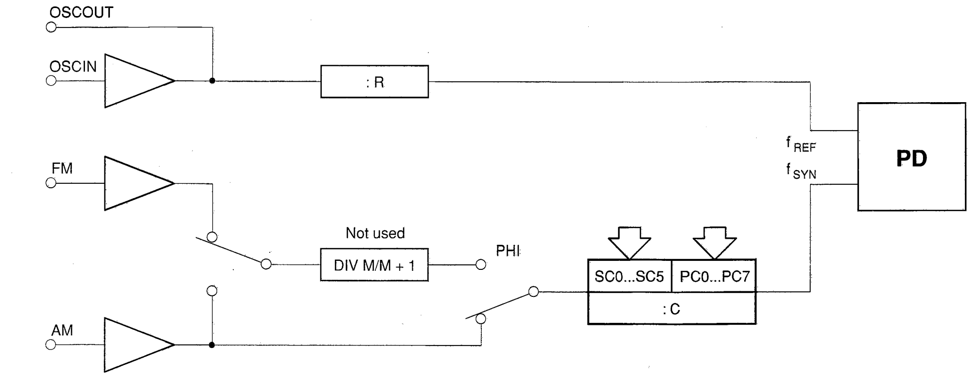
Switching from 12.5kHz to 25kHz reference frequency :

$B_2 = B_1$, $A_2 = \frac{A_1}{2}$ and $A_2 = \frac{(A_1 + 1)}{2}$

for odd values A_1.

3.3 AM DIRECT MODE OPERATION FOR SW, MW AND LW

Figure 3



REGISTER STATUS / FUNCTION

CURR1	CURR2	I_{CHARGE} (ratio)
0	0	1
1	0	100
1	1	60
0	1	40

REGISTER STATUS / FUNCTION

f_{REF}	SWM /DIR	AM/FM	MODE	f_{REF} freq
X	0	0	STOP	0
0	1	0	AM	1k
1	1	0	AM	2.5k

REGISTER STATUS / FUNCTION

TEST0	TEST1	TEST2	TST/OUT PIN	OSCIN PIN
0	0	0	SOUT	OSC
1	0	0	f_{REF} OUT	OSC
0	1	0	PHI IN	f_{REF} IN
1	1	0	f_{SYN} OUT	f_{REF} IN
0	0	1	f_{SYN} IN	OSC

91DSTDA7326-05

The AM signal is directly applied to the 14 bit static divider 'C'. This divider is controlled by both SC and PC registers.
Dividing range : $f_{VCO} = (C + 1) \cdot f_{REF}$

4. Reference Frequency Generator

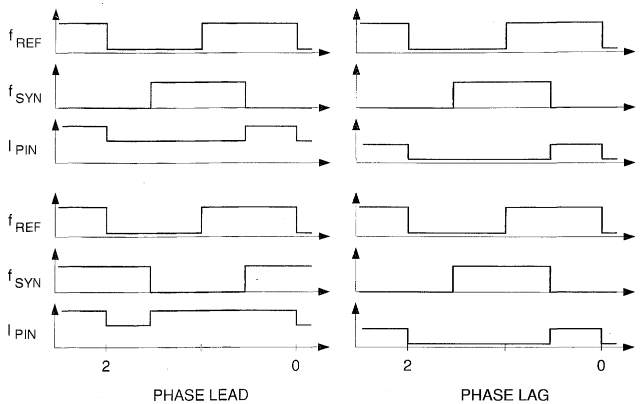
The crystal oscillator clock is divided by the reference frequency divider to provide the reference frequency to the phase comparator. Reference frequency divider range is selectable by the programming bit 'f_{REF}'. Available reference frequency are shown in following table.

AM/FM	f_{REF}	f_{REF} (kHz)
0	0	12.5
0	1	25
1	0	1
1	1	2.5

5. Three State Phase Comparator

The phase comparator generates a phase error signal according to phase difference between f_{SYN} and f_{REF}. This phase error signal drives the charge pump current generator.

Figure 4



6. Charge Pump Current Generator

This system generators signed pulses of current. Duration and polarity of those pulses are determined by the phase error signal. The current absolute values are programmable by 'CURR1' and 'CURR2' register and controlled by an external resistor R_{ISET} connected to Pin 2 and GND. Available current values are shown on following table.

R_{ISET} (kΩ)		10	22	47
Curr1	Curr2	I_{CHARGE} (µA)		
0	0		1	
0	1		40	
1	0		100	
1	1		60	

7. Low Noise MOS Op-Amp

A low noise Op-Amp is available on chip. The positive input of this Op-Amp is connected to an internal voltage divider and to Pin 3 'V_{REF}'. The negative input is connected to the charge pump output.

In cooperation with this internal amplifier and external components, a active filter can be provided. To increase the flexibility in application the negative input can be switched to two input pins (Pins 15 and 16). This switch is controlled by 'LPF' register with 'LPF' low Pin 15 is active and 'LPF' high Pin 16 is active. This feature allows two separate active filters with different performance.

8. Switch Output

At Pin 9 'TST/SOUT' a digital n-channel open drain output is available in application. This output is controlled by the 'SOUT' -register.

9. C-Bus Interface

This interface allows communication between the PLL device and µp systems. A bus control system check the format of transmission, only eight bit word transmission is allowed. Four registers with 6 bit are user programmable. The selection of this four registers is controlled by two address bits.

Figure 5 : Bus Timing

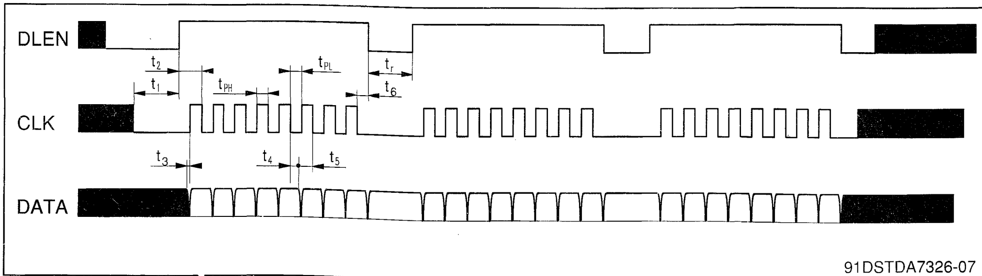


Figure 6 : Bit Organisation of Bus Transfer

Loading registers for all bytes of the programmable counters and all control registers

0	1	PC7	PC6	LPF1 /LPF2	CURR1	SWM /DIR	AM /FM	1	0	PC5	PC4	PC3	PC2	PC1	PC1
1	1	SW5 (0) *	SW4	SW3	SW2	SW1	SW0	0	0	0	0	0	SOUT	CURR2	f_{REF}

Loading registers for all bytes of the programmable counters and all control registers

0	1	PC7	PC6	LPF2 /LPF1	CURR1	SWM /DIR	AM /FM	1	0	PC5	PC4	PC3	PC2	PC1	PC1
1	1	SW5 (0) *	SW4	SW3	SW2	SW1	SW0								

Loading registers for 11 or 12 bits of the programmable counters

1	0	PC5	PC4	PC3	PC2	PC1	PC0	1	1	SW5 (0) *	SW4	SW3	SW2	SW1	SW0

Loading registers for 5 or 6 bits of the programmable counters

1	1	SW5 (0) *	SW4	SW3	SW2	SW1	SW0

Setting control register for loop filter select, charge pump current, mode select

0	1	X	X	LPF2 /LPF1	CURR1	SWM /DIR	AM /FM

Setting control register for switch output Pin 9, charge pump current bit2, reference frequency select

0	0	0	0	0	SOUT	CURR2	f_{REF}

Test mode initialization

0	0	TST0	TST1	TST2	SOUT	CURR2	f_{REF}

* This bit has to be '0' for f_{REF} = '1' (f_{REF} = 25kHz in FM mode)

91DSTDA7326-08

Figure 7 : Bit Organisation of Bus Transfer (continued)

FM mode, loopfilter 1, f_{REF} = 12.5kHz, charge pump current 100µA
SOUT = 1, divider ratio = 7816, input frequency FM IN = 98.50MHz

0	1	0	1	1	1	1	0	1	0	1	1	1	0	1	0
1	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0

Switch from 98.50MHz to 99.00MHz input frequency FM mode

1	1	0	0	1	1	0	0

Switch from 100µA to 1µA charge pump current

0	1	0	1	0	0	1	0

Switch Pin 9 'SOUT' from '1' to 'C'

0	0	0	0	0	0	0	0

AM mode (MW), loopfilter 2, f_{REF} = 1kHz, charge pump current 100µA
SOUT = 1, divider ratio = 543, input frequency AM IN = 544kHz

0	1	0	0	0	1	0	1	1	0	0	0	1	0	0	0
1	1	0	1	1	1	1	1	0	0	0	0	0	1	0	0

Switch from 544kHz to 800kHz input frequency

1	0	0	0	1	1	0	0	1	1	0	1	1	1	1	1

SWitch from 800kHz to 791kHz AM input frequency

1	1	0	1	0	1	1	0

91DSTDA7326-09

Figure 8 : Application with two Loop Filters

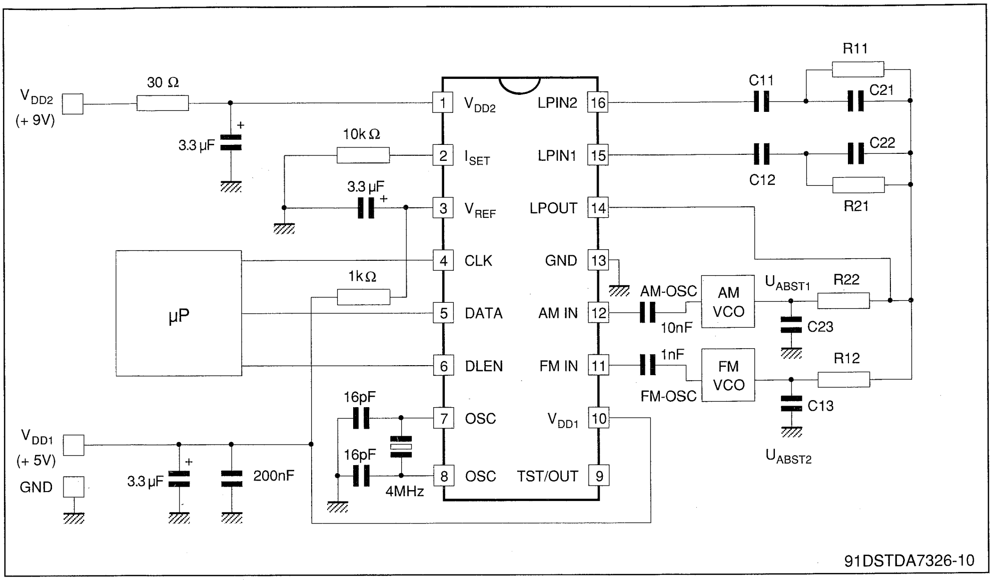
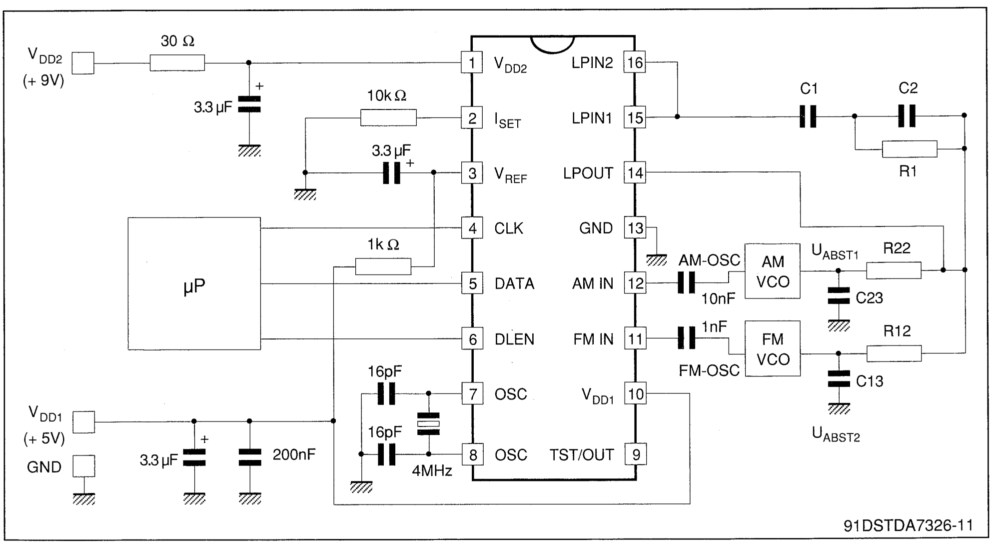


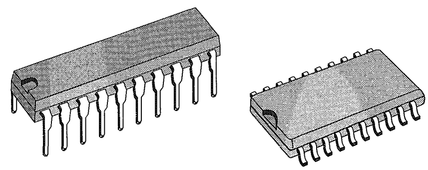
Figure 9 : Application with one Loop Filter



SINGLE CHIP RDS DEMODULATOR + FILTER

ADVANCE DATA

- HIGH PERFORMANCE, STABLE 57KHz FILTER
- FILTER ADJUSTMENT FREE AND WITHOUT EXTERNAL COMPONENTS
- PURELY DIGITAL RDS DEMODULATION WITHOUT EXTERNAL COMPONENTS
- ARI OUTPUT (SK INDICATION)
- RDS SIGNAL QUALITY OUTPUT
- 4.332MHz CRYSTAL OSCILLATOR (8.664MHz OPTIONAL)
- LOW NOISE MIXED BIPOLAR/CMOS TECHNOLOGY



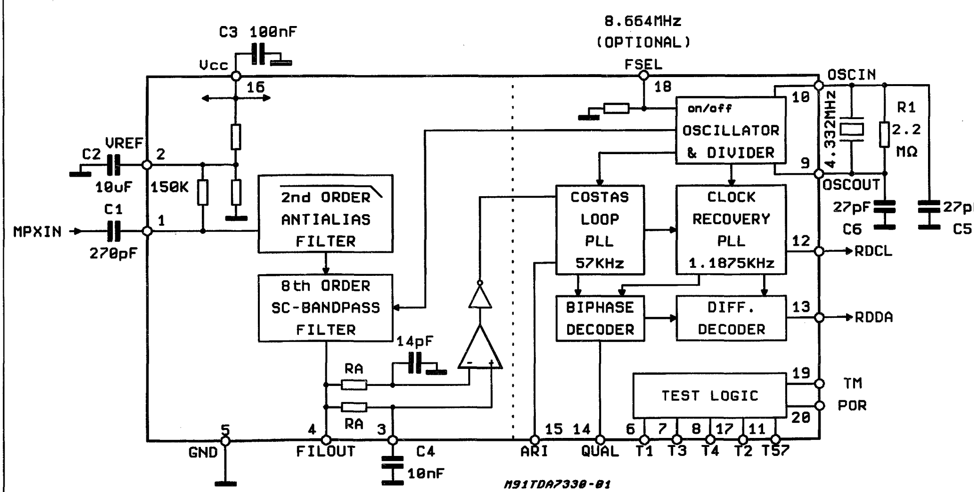
DIP20	SO20
ORDERING NUMBERS:	
TDA7330	TDA7330D

DESCRIPTION

The TDA7330 is a RDS (Radio Data System) demodulator. The IC includes a 57KHz switched capacitor input band pass filter, a bit rate clock recovery circuit, DSB demodulator circuit, BI-PHASE PSK decoder, differential decoding circuit, ARI identification and signal quality outputs.

The data and clock output signal (RDDA, RDCL) can be further processed by a suitable µP.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice. notice.

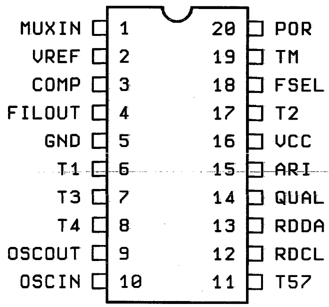
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	7	V
T_{op}	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		DIP20	SO20	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Typ.	100	200	°C/W

PIN CONNECTION (Top view)



M91TDA7330-02

PIN FUNCTION

Nr.	Name	Description
1	MUXIN	RDS input signal.
2	V_{ref}	Reference voltage
3	COMP	Not inverting comparator input (smoothing filter)
4	FIL OUT	Filter Output
5	GND	Ground
6	T1	Testing output pin (not to be used)
7	T3	Testing output pin (not to be used)
8	T4	Testing output pin (not to be used)
9	OSC OUT	Oscillator output
10	OSC IN	Oscillator Input
11	T57	Testing output pin (not to be used)
12	RDCL	RDS clock output
13	RDDA	RDS data output
14	QUAL	Output for signal quality indication (High = good)
15	ARI	Output for ARI indication (High when RDS + ARI signal is present) (High when only ARI is present) (Low when only RDS is present) (indefined when no signal is present)
16	V_{CC}	Supply Voltage
17	T2	Testing output pin (not to be used)
18	FSEL	Frequency selector pin
19	TM	Test mode pin (open = normal RUN) (closed to V_{CC} = Test mode)
20	POR	Reset Input for testing (active high)

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Tamb = 25°C; fosc = 4.332MHz; V_{IN} = 20mVrms unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}	Supply Voltage		4.5	5	5.5	V
I_S	Supply Current			9		mA
FILTER						
F_C	Center Frequency		56.5	57	57.5	KHz
BW	3dB Bandwidth		2.5	3	3.5	KHz
G	Gain	f = 57KHz	18	20	22	dB
A	Attenuation	$\Delta f = \pm 4KHz$ f = 38KHz; V_i = 500mVrms f = 67KHz; V_i = 250mVrms	18 50 35	22 80 50		dB dB dB
ΔPh	Phase non linearity	A (see note1) B (see note1) C (see note1)		0.5 1 2	5 7.5 10	DEG DEG DEG
R_i	Input Impedance		100	160	200	KΩ
S/N	Signal to Noise Ratio	V_i = 3mVrms	30	40		dB
V_i	Input Signal	f = 19KHz; T3 $\leq$ –40dB (see note2) f = 57KHz (RDS + ARI)			1 50	Vrms mVrms
R_L	Load Impedance	Pin 4	100			KΩ
LIMITER						
RA	Resistance pin 3-4		15	21	28	KΩ
OSCILLATOR						
F_{OSC}	Oscillator Frequency	F_{SEL} = Open (*) F_{SEL} = Closed to V_{CC} (**)		4.332 8.664		MHz MHz
VCLL	Clock Input level LOW				1	V
VCLH	Clock Input Level HIGH		4			V
	Output Amplitude			5		V_{PP}

CHRISTAL TYPE = EURO QUARTZ

(*) FSEL pin has an internal 40KΩ pull down resistor A 4.332MHz QUARTZ must be used (**) A 8.664MHz QUARTZ must be used.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DEMODULATOR						
S_{RDS}	RDS Detection Sensitivity		1			mVrms
S_{ARI}	ARI Detection Sensitivity		3			mVrms
T_{lock}	RDS Lockup Time			100		ms
V_{OH}	Output HIGH Voltage	I_L = 0.5mA	4			V
V_{OL}	Output LOW Voltage	I_L = 0.5mA			1	V
f_{RDS}	Data Rate for RDS			1187.5		Hz

Note(1):
The phase non linearity is defined as: $\Delta Ph = | -2\ \phi f2 + \phi f1 + \phi f3 |$
where ϕfx is the input-output phase difference at the frequency fx (x = 1,2,3)

Measure	f1 (KHz)	f2 (KHz)	f3 (KHz)	ΔPh max
A	56.5	57	57.5	<5°
B	56	57	58	<7.5°
C	55.5	57	58.5	<10°

Note(2): The 3th harmonic (57KHz) must be less than -40dB in respect to the input signal plus gain.

SGS-THOMSON MICROELECTRONICS

TDA7332

RDS FILTER

ADVANCE DATA

- HIGH PERFORMANCE, STABLE 57KHz FILTER
- HIGH SELECTIVITY
- FLAT GROUP DELAY
- HIGH PERFORMANCE LIMITER
- VERY FEW EXTERNAL COMPONENTS
- 4.332MHz CLOCK OSCILLATOR (8.664MHz OPTIONAL)

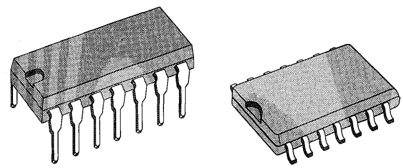
DESCRIPTION

The TDA7332 is an RDS filter, realized in switched capacitor technique.

The 4 biquad stage architecture is working with 4.332MHz clock.

Optionally a 8.664MHz xtal can be used.

The filter has a center frequency of 57KHz and a bandwidth of 3KHz. Input 2nd order antialiasing filter and output smoothing filter are provided.



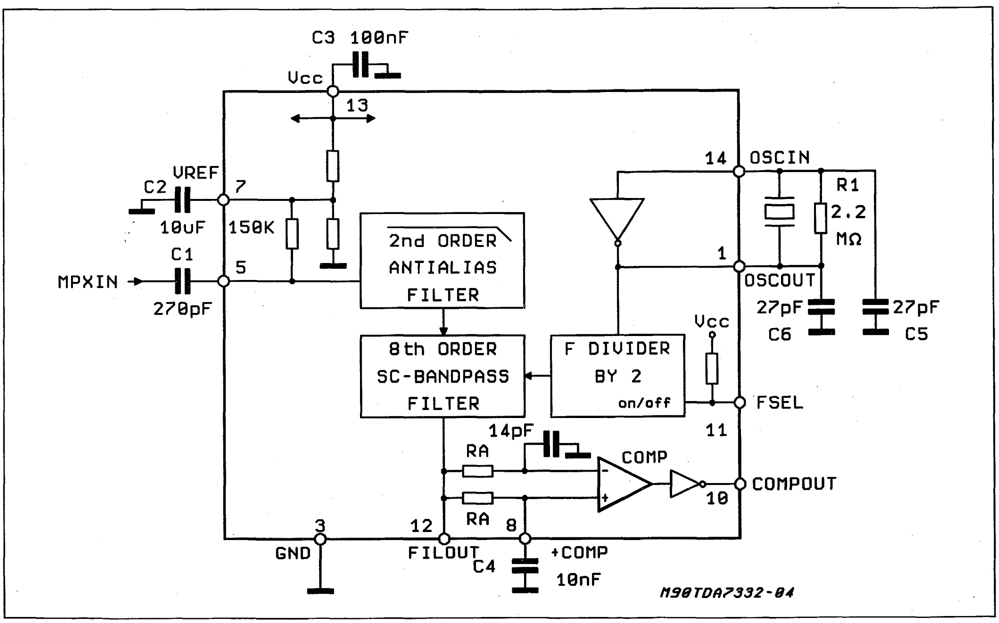
DIP14 **SO14**

ORDERING NUMBERS:

TDA7332 TDA7332D

TDA7332DIE1 (Chip on wafer)

TEST CIRCUIT



May 1991

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice. notice.

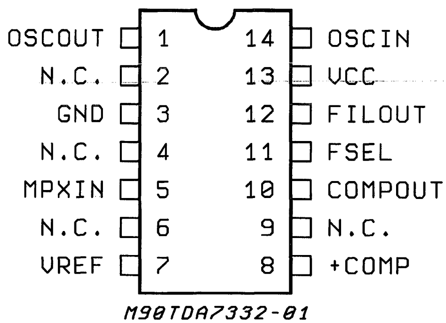
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	7	V
T_{op}	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature	-40 to 150	°C

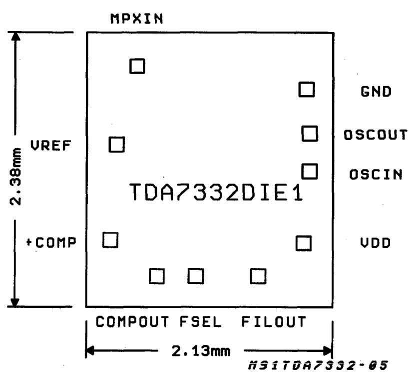
THERMAL DATA

Symbol	Description		DIP14	SO14	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Typ.	100	200	°C/W

PIN CONNECTION (Top view)



BONDING PAD LOCATIONS (Top view)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Tamb = 25°C; fosc = 4.332MHz; V_{IN} = 20mVrms unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY SECTION						
V_{CC}	Supply Voltage		4.5	5	5.5	V
I_S	Supply Current		6	9	14	mA
FILTER						
F_C	Center Frequency		56.5	57	57.5	KHz
BW	3dB Bandwidth		2.5	3	3.5	KHz
G	Gain	f = 57KHz	18	20	22	dB
A	Attenuation	Δf = ±4KHz f = 38KHz; V_i = 500mVrms f = 67KHz; V_i = 250mVrms	18 50 35	22 80 50		dB dB dB
ΔPh	Phase non linearity	A (see note1) B (see note1) C (see note1)		0.5 1 2	5 7.5 10	DEG DEG DEG
R_i	Input Impedance		100	160	200	KΩ
S/N	Signal to Noise Ratio	V_i = 3mVrms	30	40		dB
V_i	Input Signal	f = 19KHz; T3 ≤ –40dB (see note2) f = 57KHz (RDS + ARI)			1 50	Vrms mVrms
R_L	Load Impedance	Pin 12	100			KΩ
LIMITER						
RA	Resistance pin 8-12		15	21	28	KΩ
V_{OL}	Comp. Output LOW	I_O = +0.5mA			1	V
V_{OH}	Comp. Output HIGH	IO = –0.5mA	4			V
	Duty Cycle	V_i = 1mVrms		50		%
OSCILLATOR						
F_{OSC}	Oscillator Frequency	F_{SEL} = Open F_{SEL} = Closed to Ground		4.332 8.664		MHz MHz
	Output Amplitude			5		V_{PP}
V_{CLL}	Clock Input Level LOW				1	V
V_{OLH}	Clock Input Level HIGH		4			V

CRYSTAL TYPE = EURO QUARTZ

Note (1):
The phase non linearity is defined as: $\Delta Ph = | -2\ \phi f2 + \phi f1 + \phi f3 |$
where ϕfx is the input-output phase difference at the frequency fx (x = 1,2,3)

Measure	f1 (KHz)	f2 (KHz)	f3 (KHz)	ΔPh max
A	56.5	57	57.5	<5°
B	56	57	58	<7.5°
C	55.5	57	58.5	<10°

Note (2): The 3th harmonic (57KHz) at the output (pin12) must be less than -40dB in respect to the input signal plus gain.

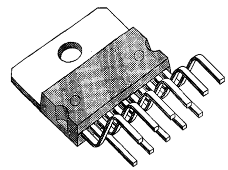
22W BRIDGE-STEREO AMPLIFIER FOR CAR RADIO

PRELIMINARY DATA

- VERY FEW EXTERNAL COMPONENTS
- NO BOUCHEROT CELLS
- NO BOOSTRAP CAPACITORS
- HIGH OUTPUT POWER
- NO SWITCH ON/OFF NOISE
- VERY LOW STAND-BY CURRENT
- FIXED GAIN (30dB STEREO)
- PROGRAMMABLE TURN-ON DELAY

Protections:

- OUTPUT AC-DC SHORT CIRCUIT TO GROUND AND TO SUPPLY VOLTAGE
- VERY INDUCTIVE LOADS
- LOUDSPEAKER PROTECTION
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GROUND



Multiwatt - 11

ORDERING NUMBER: TDA7350

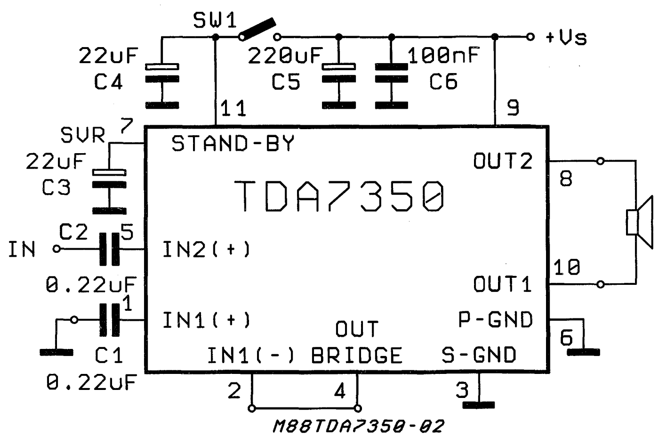
DESCRIPTION

The TDA7350 is a new technology class AB Audio Power Amplifier in the Multiwatt® package designed for car radio applications.

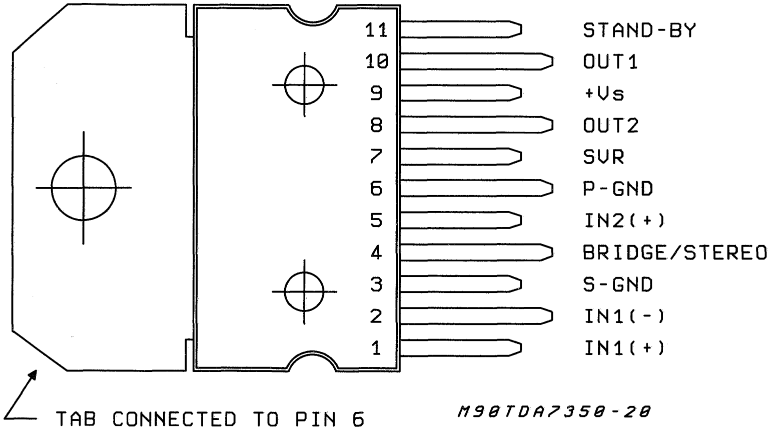
Thanks to the fully complementary PNP/NPN output configuration the high power performance of the TDA7350 is obtained without bootstrap capacitors.

A delayed turn-on mute circuit eliminates audible on/off noise, and a novel short circuit protection system prevents spurious intervention with highly inductive loads.

APPLICATION CIRCUIT BRIDGE



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Operating Supply Voltage	18	V
V_S	DC Supply Voltage	28	V
V_S	Peak Supply Voltage (for t = 50ms)	40	V
I_o	Output Peak Current (non rep. for t = 100µs)	5	A
I_o	Output Peak Current (rep. freq. > 10Hz)	4	A
P_{tot}	Power Dissipation at T_{case} = 85°C	36	W
$T_{stg,TJ}$	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, T_{amb} = 25°C, V_S = 14.4V, f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range			8		18	V
I_d	Total Quiescent Drain Current	stereo configuration				120	mA
A_{SB}	Stand-by attenuation			60	80		dB
I_{SB}	Stand-by Current					100	µA
T_{sd}	Thermal Shut-down Junction Temperature				150		°C

STEREO

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
P_o	Output Power (each channel)	d = 10% R_L = 2Ω R_L = 3.2Ω R_L = 4Ω		 7	 11 8 6.5		 W W W
		d = 10%; V_S = 13.2V R_L = 2Ω R_L = 3.2Ω R_L = 4Ω			 9 6.5 5.5		 W W W
d	Distortion	P_o = 0.1 to 4W; R_L = 3.2Ω				0.5	%
SVR	Supply Voltage Rejection	R_S = 10kΩ f = 100Hz	C3 = 22µF C3 = 100µF	45	50 57		dB
CT	Crosstalk	f = 1KHz f = 10KHz		45	55 50		dB dB
R_I	Input Resistance			30	50		KΩ
G_V	Voltage Gain			27	29	31	dB
G_V	Voltage Gain Match					1	dB
E_{IN}	Input Noise Voltage	R_S = 50Ω (*) R_S = 10KΩ (*) R_S = 50Ω (**) R_S = 10KΩ (**)			1.5 2 2 2.7	 7	µV µV µV µV

BRIDGE

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
P_o	Output Power	d = 10%; R_L = 4Ω d = 10%; R_L = 3.2Ω		 16	20 22		W W
		d = 10%; V_S = 13.2V R_L = 4Ω R_L = 3.2Ω			 17.5 19		 W W
d	Distortion	P_o = 0.1 to 10W; R_L = 4Ω				1	%
V_{OS}	Output Offset Voltage					250	mV
SVR	Supply Voltage Rejection	R_S = 10KΩ f = 100Hz	C3 = 22µF C3 = 100µF	45	50 57		dB
R_I	Input Resistance				50		KΩ
G_V	Voltage Gain			33	35	37	dB
E_{IN}	Input Noise Voltage	R_S = 50Ω (*) R_S = 10KΩ (*) R_S = 50Ω (**) R_S = 10KΩ (**)			2 2.5 2.7 3.2		µV µV µV µV

(*) Curve A
(**) 22Hz to 22KHz

Figure 1: STEREO Test and Appication Circuit

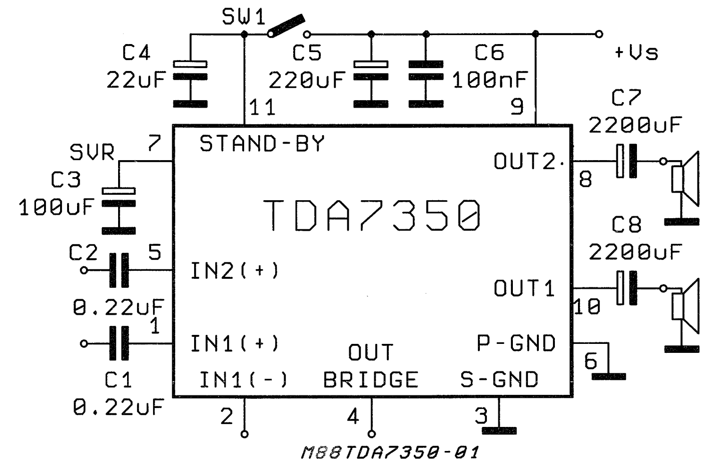


Figure 2: P.C. Board and Layout (STEREO) of the circuit of fig. 1 (1:1 scale)

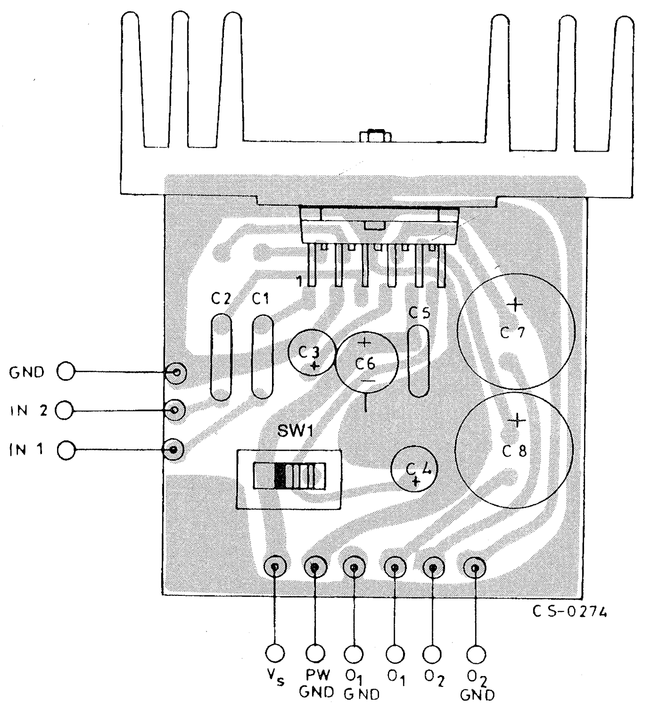


Figure 3: BRIDGE Test and Appication Circuit

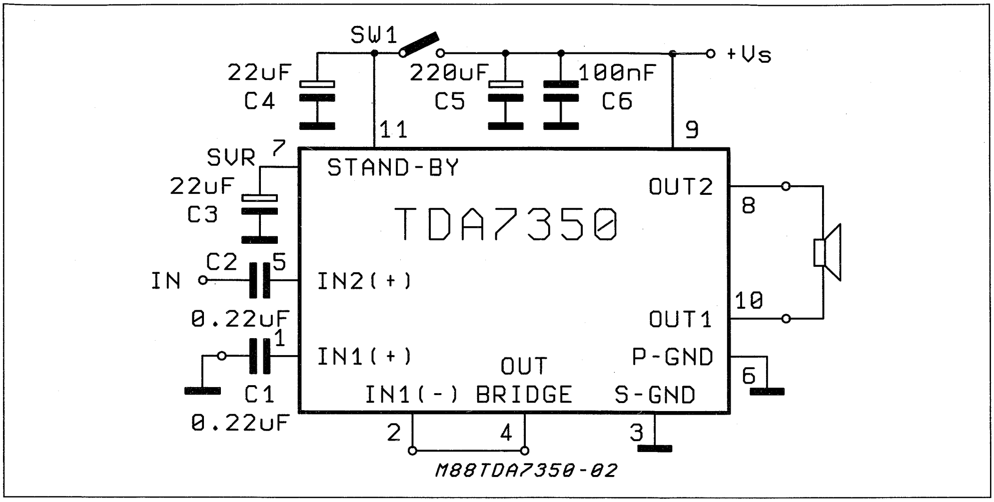
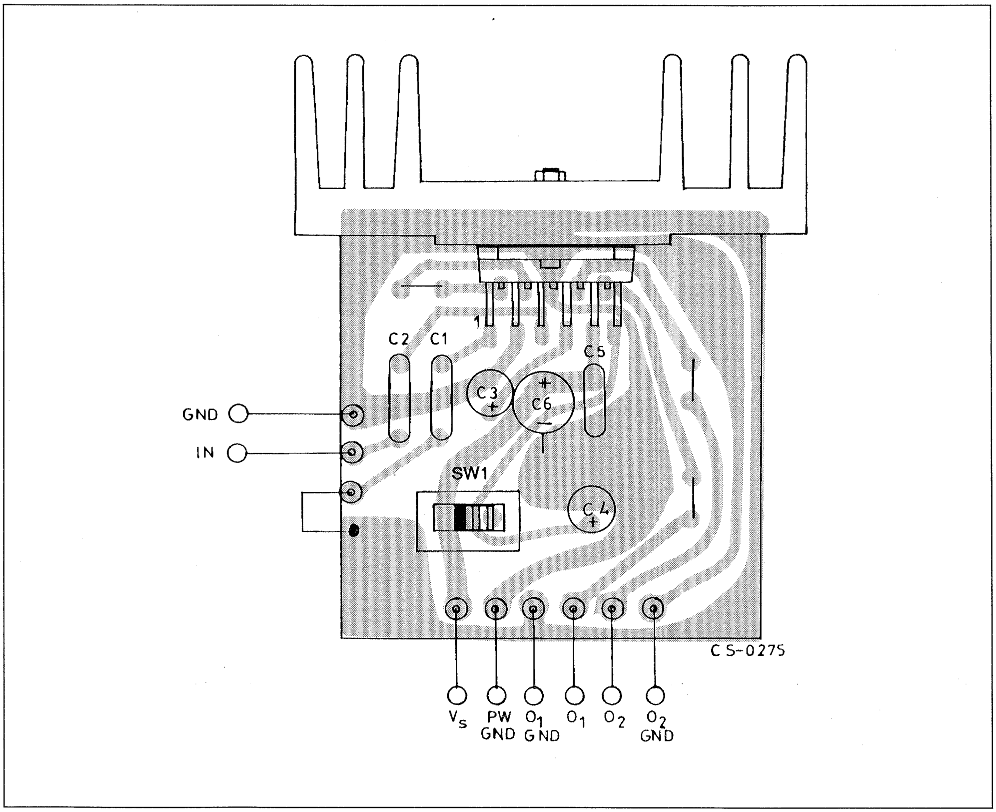


Figure 4: P.C. Board and Layout (BRIDGE) of the circuit of fig. 3 (1:1 scale)



RECOMMENDED VALUES OF THE EXTERNAL COMPONENTS (ref to the Stereo Test and Application Circuit)

Component	Recommended Value	Purpose	Larger than the Recomm. Value	Smaller than the Recomm. Value
C1	0.22µF	Input Decoupling (CH1)	—	—
C2	0.22µF	Input Decoupling (CH2)	—	—
C3	100µF	Supply Voltage Rejection Filtering Capacitor	Longer Turn-On Delay Time	Worse Supply Voltage Rejection. Shorter Turn-On Delay Time Danger of Noise (POP)
C4	22µF	Stand-By ON/OFF Delay	Delayed Turn-Off by Stand-By Switch	Danger of Noise (POP)
C5	220µF (min)	Supply By-Pass		Danger of Oscillations
C6	100nF (min)	Supply By-Pass		Danger of Oscillations
C7	2200µF	Output Decoupling CH2	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay
C8	2200µF	Output Decoupling CH1	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay

Figure 5: Output Power vs. Supply Voltage (Stereo)

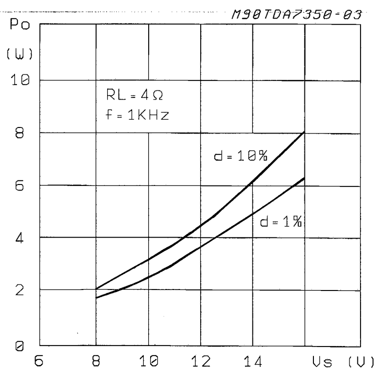


Figure 6: Output Power vs. Supply Voltage (Stereo)

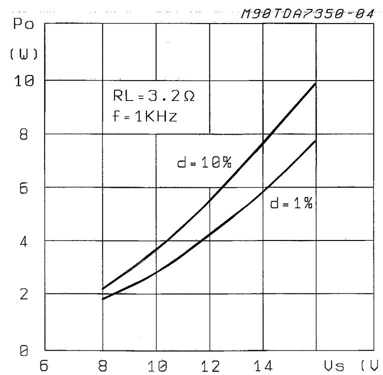


Figure 7: Output Power vs. Supply Voltage (Stereo)

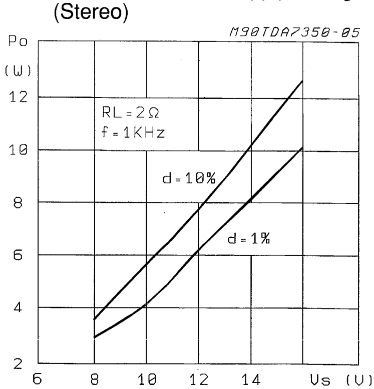


Figure 8: Output Power vs. Supply Voltage (Bridge)

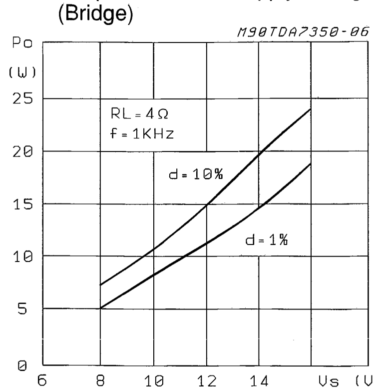


Figure 9: Output Power vs. Supply Voltage (Bridge)

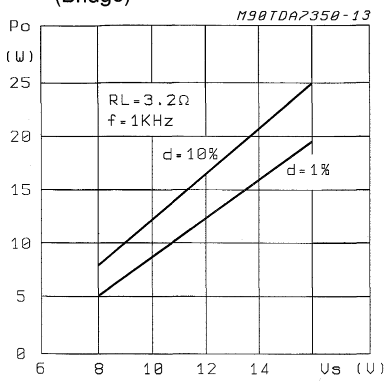


Figure 10: Drain Current vs Supply Voltage (Stereo)

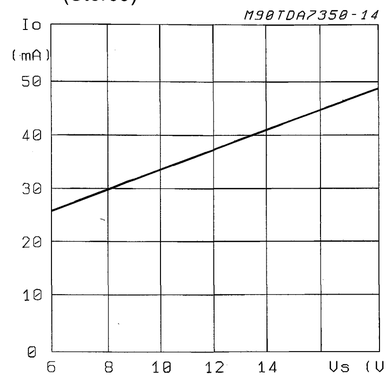


Figure 11: Distortion vs Output Power (Stereo)

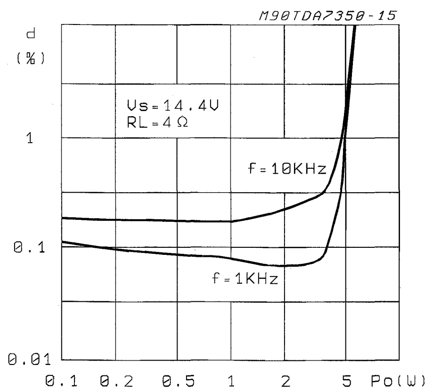


Figure 12: Distortion vs Output Power (Stereo)

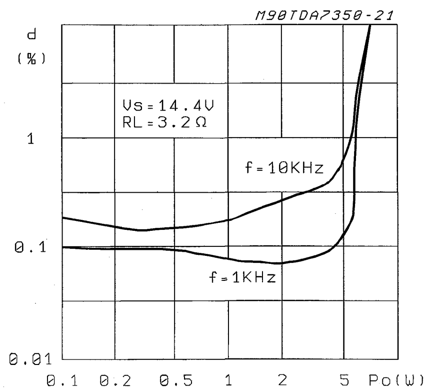


Figure 13: Distortion vs Output Power (Stereo)

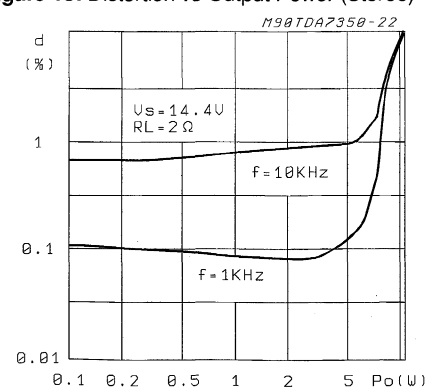


Figure 14: Distortion vs Output Power (Bridge)

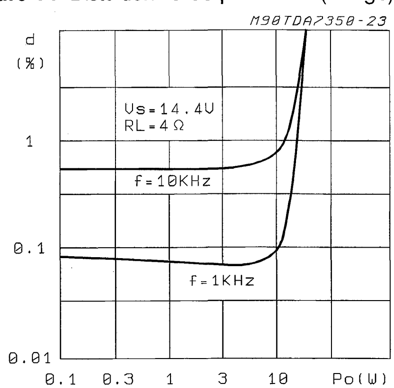


Figure 15: SVR vs. Frequency & C_{SVR} (Stereo)

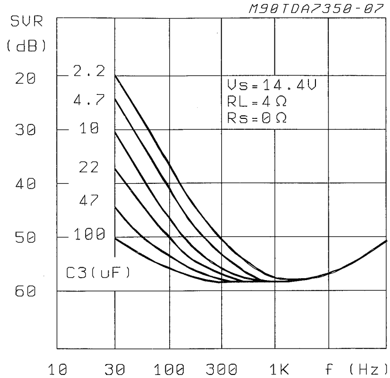


Figure 16: SVR vs. Frequency & C_{SVR}; (Stereo)

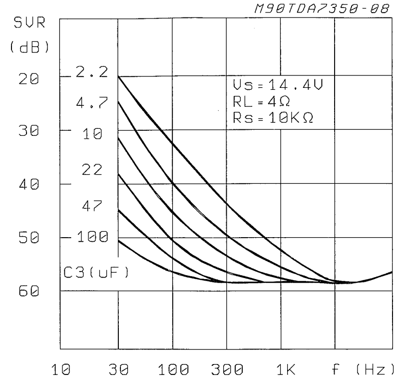


Figure 17: SVR vs. Frequency & C_{SVR}; (Bridge)

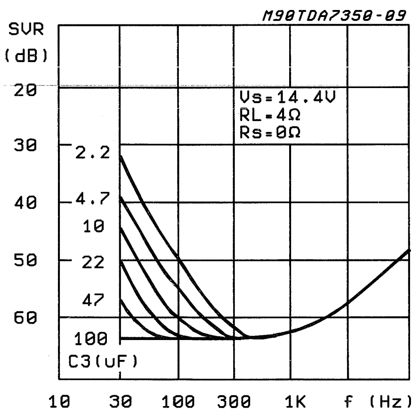


Figure 18: SVR vs. Frequency & C_{SVR}; (Bridge)

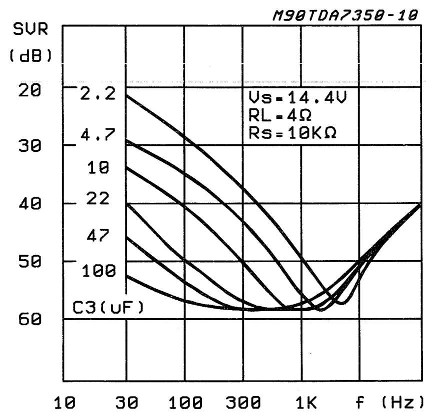


Figure 19: Crosstalk vs. Frequency (Stereo)

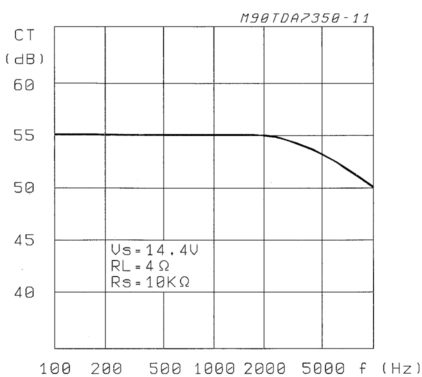


Figure 20: Power Dissipation & Efficiency vs. Output Power (Stereo)

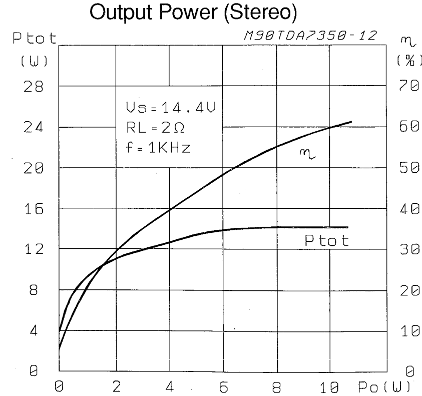


Figure 21: Power Dissipation & Efficiency vs. Output Power (Stereo)

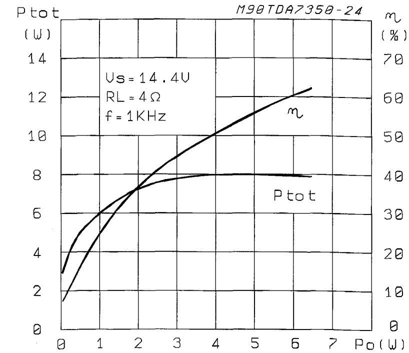


Figure 22: Power Dissipation & Efficiency vs. Output Power (Bridge)

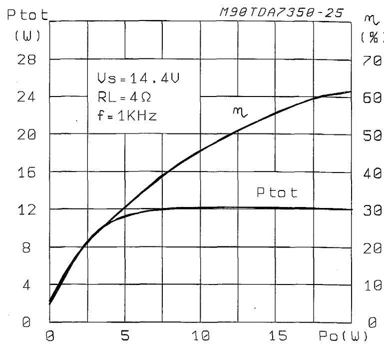
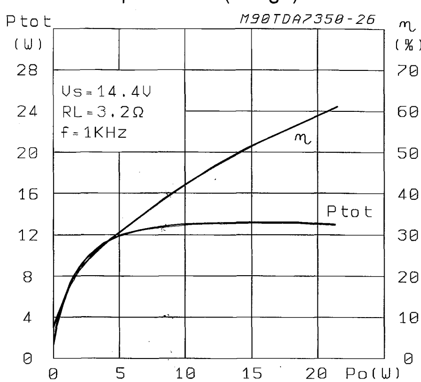


Figure 23: Power Dissipation & Efficiency vs. Output Power (Bridge)



AMPLIFIER ORGANIZATION

The TDA7350 has been developed taking care of the key concepts of the modern power audio amplifier for car radio such as: space and costs saving due to the minimized external count, excellent electrical performances, flexibility in use, superior reliability thanks to a built-in array of protections. As a result the following performances has been achieved:

- NO NEED OF BOOTSTRAP CAPACITORS EVEN AT THE HIGHEST OUTPUT POWER LEVELS
- ABSOLUTE STABILITY WITHOUT EXTERNAL COMPENSATION THANKS TO THE INNOVATIVE OUT STAGE CONFIGURATION, ALSO ALLOWING INTERNALLY FIXED CLOSED LOOP LOWER THAN COMPETITORS
- LOW GAIN (30dB STEREO FIXED WITHOUT ANY EXTERNAL COMPONENTS) IN ORDER TO MINIMIZE THE OUTPUT NOISE AND OPTIMIZE SVR
- SILENT MUTE/ST-BY FUNCTION FEATURING ABSENCE OF POP ON/OFF NOISE
- HIGH SVR
- STEREO/BRIDGE OPERATION WITHOUT ADDITION OF EXTERNAL COMPONENT
- AC/DC SHORT CIRCUIT PROTECTION (TO GND, TO V_S, ACROSS THE LOAD)
- LOUDSPEAKER PROTECTION
- DUMP PROTECTION

BLOCK DESCRIPTION

Polarization

The device is organized with the gain resistors directly connected to the signal ground pin i.e. without gain capacitors (fig. 24).

The non inverting inputs of the amplifiers are connected to the SVR pin by means of resistor dividers, equal to the feedback networks. This allows the outputs to track the SVR pin which is sufficiently slow to avoid audible turn-on and turn-off transients.

SVR

The voltage ripple on the outputs is equal to the one on SVR pin: with appropriate selection of C_{SVR}, more than 55dB of ripple rejection can be obtained.

Delayed Turn-on (muting)

The C_{SVR} sets a signal turn-on delay too. A circuit is included which mutes the device until the voltage on SVR pin reaches ~2.5V typ. (fig. 25). The mute function is obtained by duplicating the input differential pair (fig. 26): it can be switched to the signal source or to an internal mute input. This feature is necessary to prevent transients at the inputs reaching the loudspeaker(s) immediately after power-on).

Fig. 25 represents the detailed turn-on transient with reference to the stereo configuration.
At the power-on the output decoupling capacitors are charged through an internal path but the device itself remains switched off (Phase 1 of the represented diagram).
When the outputs reach the voltage level of about 1V (this means that there is no presence of short circuits) the device switches on, the SVR capacitor starts charging itself and the output tracks exactly the SVR pin.
During this phase the device is muted until the SVR reaches the "Play" threshold (~2.5V typ.), after that the music signal starts being played.

Stereo/Bridge Switching
There is also no need for external components for changing from stereo to bridge configuration (figg. 24-27). A simple short circuit between two pins allows phase reversal at one output, yet maintaining the quiescent output voltage.

Stand-by
The device is also equipped with a stand-by function, so that a low current, and hence low cost switch, can be used for turn on/off.

Stability
The device is provided with an internal compensation wich allows to reach low values of closed loop gain.
In this way better performances on S/N ratio and SVR can be obtained.

Figure 24: Block Diagram; Stereo Configuration

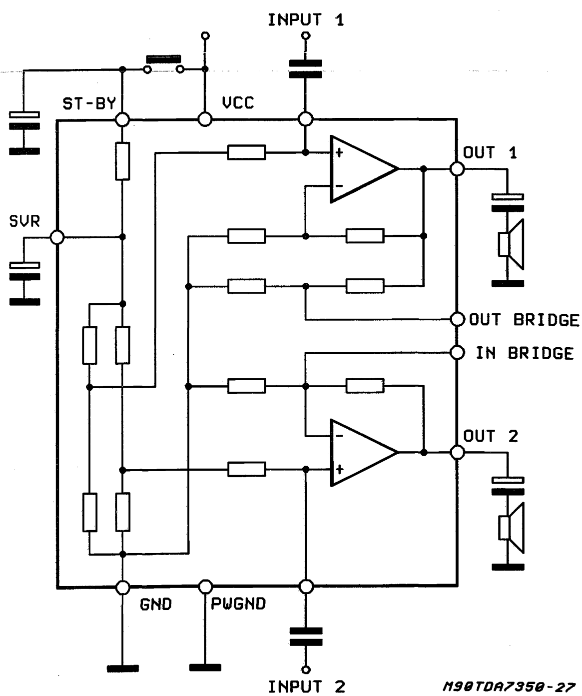


Figure 25: Turn-on Delay Circuit

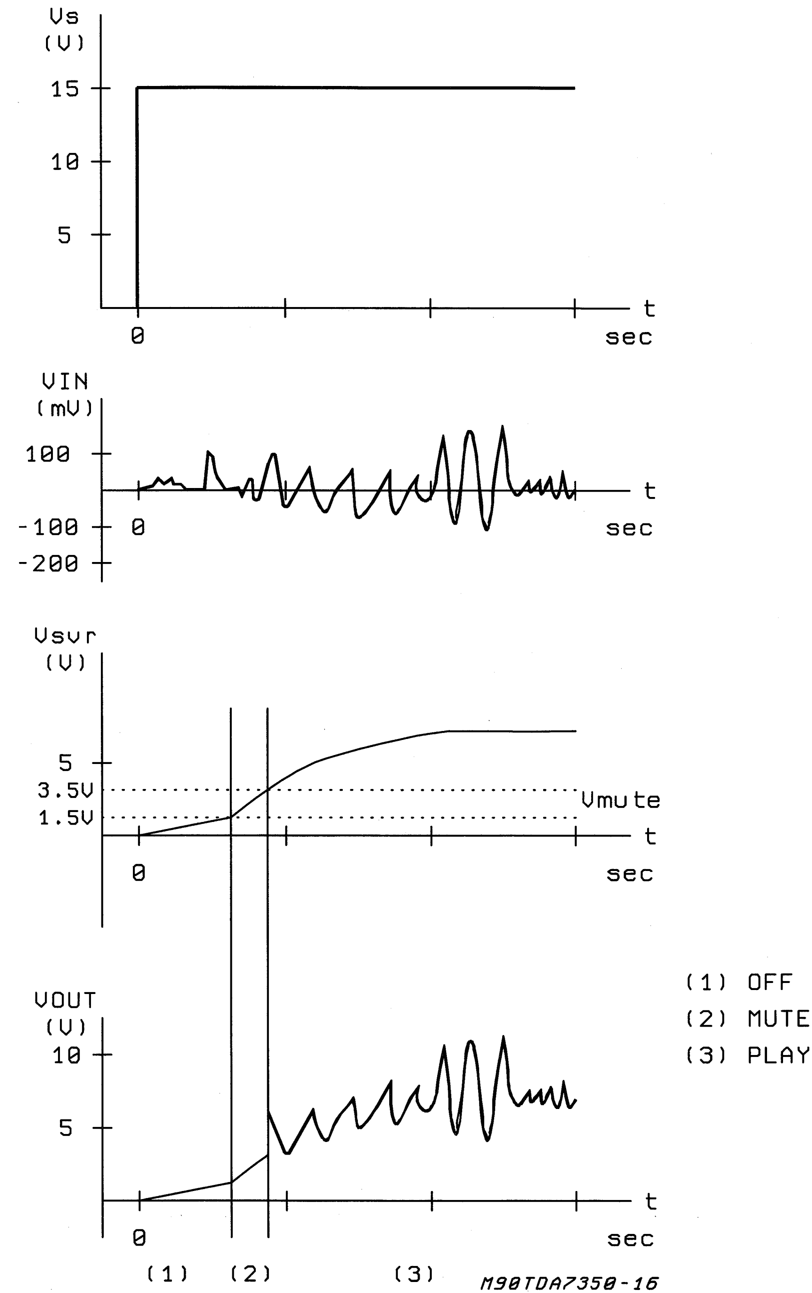


Figure 26: Mute Function Diagram

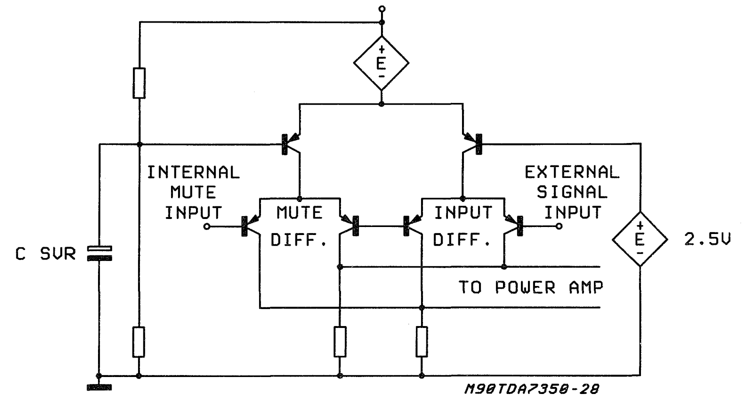


Figure 27: Block Diagram; Bridge Configuration

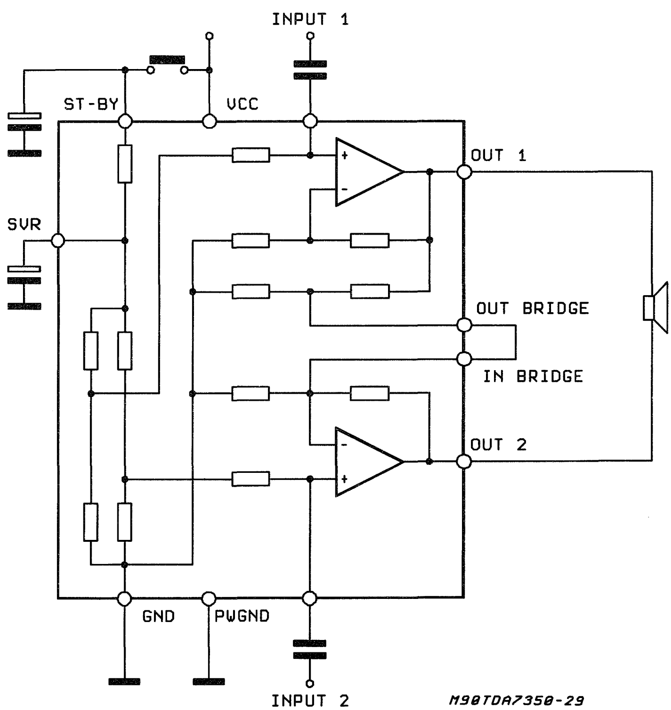


Figure 28: ICV - PNP Gain vs. I_C

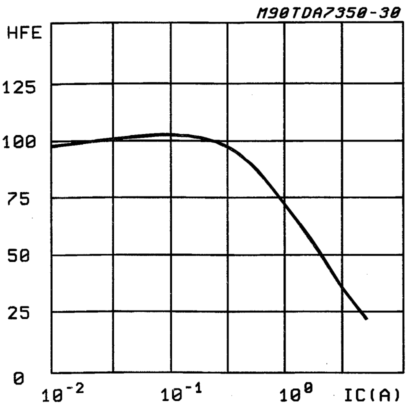


Figure 29: ICV - PNP $V_{CE(sat)}$ vs. I_C

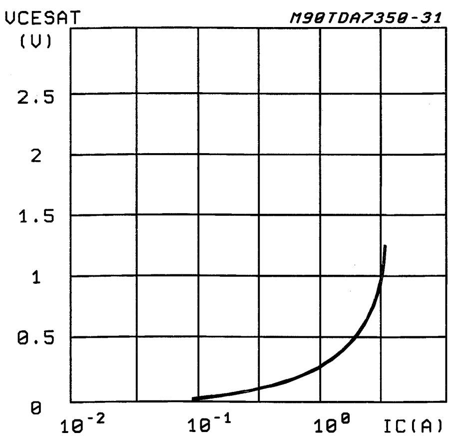
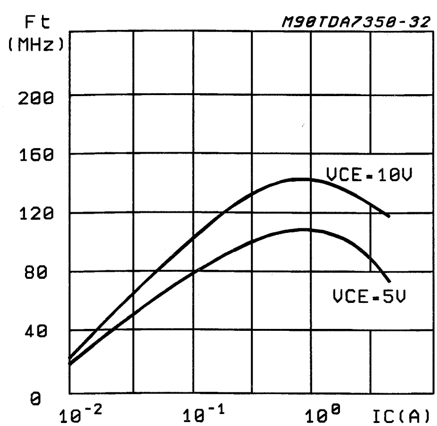


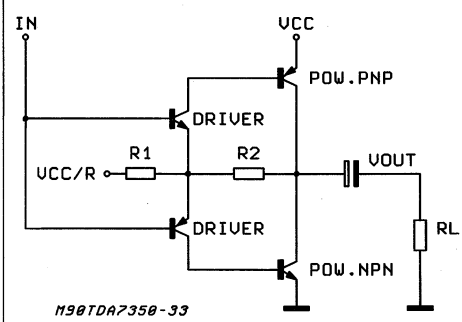
Figure 30: ICV - PNP cut-off frequency vs. I_C



OUTPUT STAGE

Poor current capability and low cutoff frequency are well known limits of the standard lateral PNP. Composite PNP-NPN power output stages have been widely used, regardless their high saturation drop. This drop can be overcome only at the expense of external components, namely, the bootstrap capacitors. The availability of 4A isolated collector PNP (ICV PNP) adds versatility to the design. The performance of this component, in terms of gain, V_{CEsat} and cut-off frequency, is shown in fig. 28, 29, 30 respectively. It is realized in a new bipolar technology, characterized by top-bottom isolation techniques, allowing the implementation of low leakage diodes, too. It guarantees BV_{CEO} > 20V and BV_{CBO} > 50V both for NPN and PNP transistors. Basically, the connection shown in fig. 31 has been chosen. First of all because its voltage swing is rail-to-rail, limited only by the VCEsat of the output transistors, which are in the range of 0.3Ω each. Then, the gain VOUT/VIN is greater than unity, approximately 1+R2/R1. (VCC/2 is fixed by an auxiliary amplifier common to both channel). It is possible, controlling the amount of this local feedback, to force the loop gain (A . β) to less than unity at frequencies for which the phase shift is 180°. This means that the output buffer is intrinsically stable and not prone to oscillation.

Figure 31: The New Output Stage



In contrast, with the circuit of fig. 32, the solution adopted to reduce the gain at high frequencies is the use of an external RC network.

AMPLIFIER BLOCK DIAGRAM

The block diagram of each voltage amplifier is shown in fig. 33. Regardless of production spread, the current in each final stage is kept low, with enough margin on the minimum, below which cross-over distortion would appear.

Figure 32: A Classical Output Stage

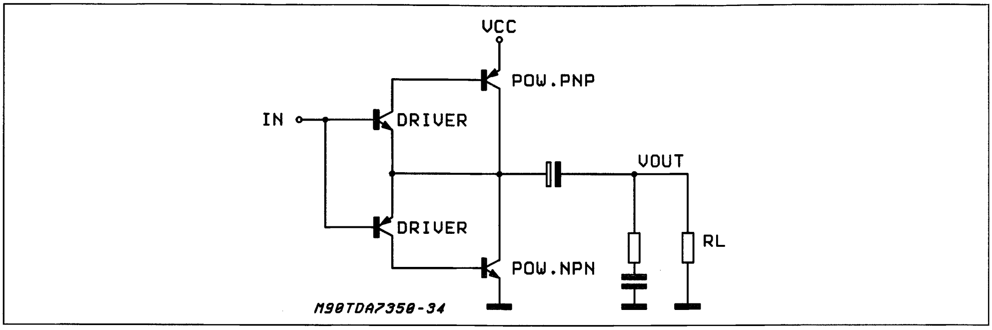
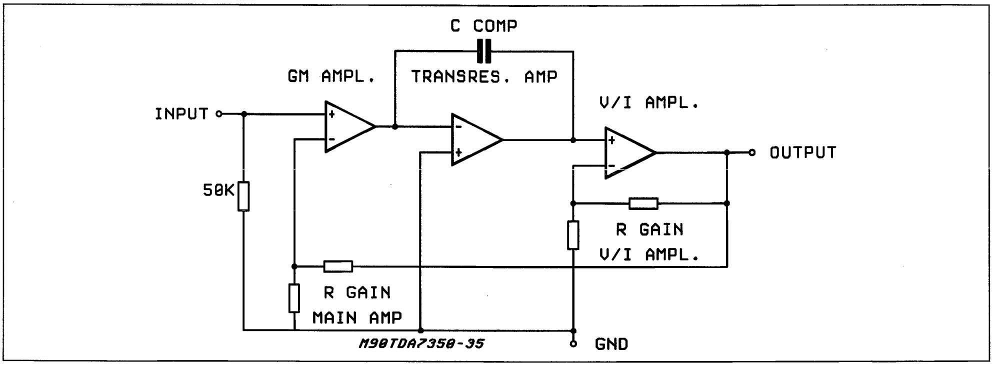


Figure 33: Amplifier Block Diagram



BUILT-IN PROTECTION SYSTEMS

Short Circuit Protection

The maximum current the device can deliver can be calculated by considering the voltage that may be present at the terminals of a car radio amplifier and the minimum load impedance.

Apart from consideration concerning the area of the power transistors it is not difficult to achieve peak currents of this magnitude (5A peak).
However, it becomes more complicated if AC and DC short circuit protection is also required.In particular,with a protection circuit which limits the output current following the SOA curve of the output transistors it is possible that in some conditions (highly reactive loads, for example) the protection circuit may intervene during normal operation. For this reason each amplifier has been equipped with a protection circuit that intervenes when the output current exceeds 4A.

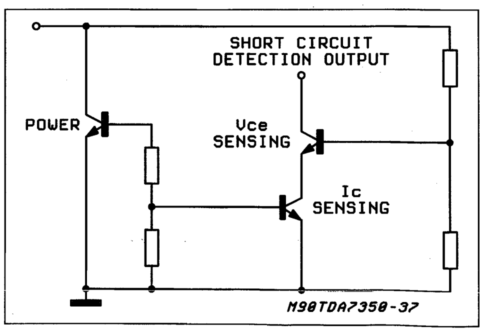
Fig 34 shows the protection circuit for an NPN power transistor (a symmetrical circuit applies to PNP).The VBE of the power is monitored and gives out a signal,available through a cascode.

This cascode is used to avoid the intervention of the short circuit protection when the saturation is below a given limit.

The signal sets a flip-flop which forces the amplifier outputs into a high impedance state.

In case of DC short circuit when the short circuit is removed the flip-flop is reset and restarts the circuit (fig. 38). In case of AC short circuit or load shorted in Bridge configuration, the device is continuously switched in ON/OFF conditions and the current is limited.

Figure 34: Circuitry for Short Circuit Detection



Load Dump Voltage Surge

The TDA 7350 has a circuit which enables it to withstand a voltage pulse train on pin 9, of the type shown in fig. 36.
If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.

A suggested LC network is shown in fig. 35.
With this network, a train of pulses with amplitude up to 120V and width of 2ms can be applied at point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Polarity Inversion

Figure 35

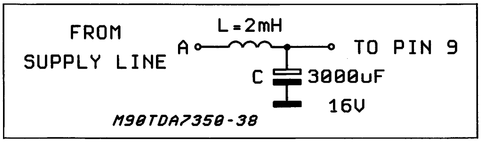
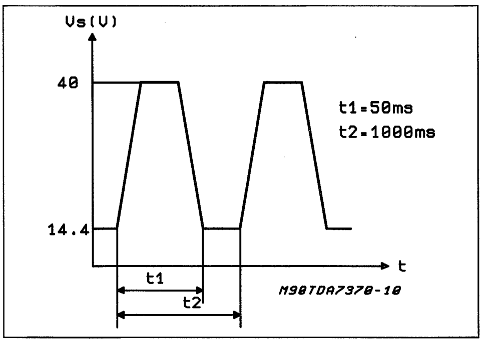


Figure 36



High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This features is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open Ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA7350 protection diodes are included to avoid any damage.

DC Voltage

The maximum operating DC voltage for the TDA7350 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

Thermal Shut-down

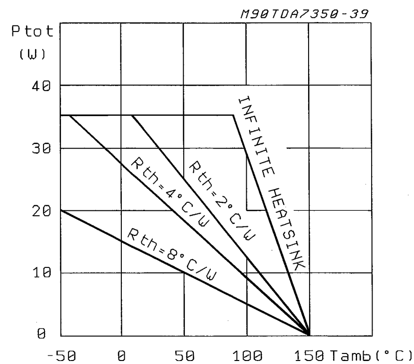
The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 37 shows the dissipable power as a function of ambient temperature for different thermal resistance.

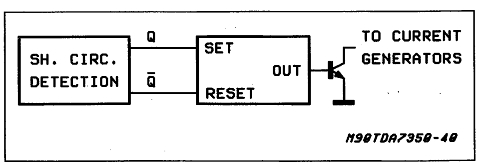
Figure 37: Maximum Allowable Power Dissipation vs. Ambient Temperature



Loudspeaker Protection

The TDA7350 guarantees safe operations even for the loudspeaker in case of accidental shortcircuit.
Whenever a single OUT to GND, OUT to V_S short circuit occurs both the outputs are switched OFF so limiting dangerous DC current flowing through the loudspeaker.

Figure 38: Restart Circuit



APPLICATION HINTS

This section explains briefly how to get the best from the TDA7350 and presents some application circuits with suggestions for the value of the components.These values can change depending on the characteristics that the designer of the car radio wants to obtain,or other parts of the car radio that are connected to the audio block.

To optimize the performance of the audio part it is useful (or indispensable) to analyze also the parts outside this block that can have an interconnection with the amplifier.

This method can provide components and system cost saving.

Reducing Turn On-Off Pop

The TDA7350 has been designed in a way that the turn on(off) transients are controlled through the charge(discharge) of the Csvr capacitor.

As a result of it, the turn on(off) transient spectrum contents is limited only to the subsonic range.The following section gives some brief notes to get the best from this design feature(it will refer mainly to the stereo application which appears to be in most cases the more critical from the pop viewpoint.The bridge connection in fact,due to the common mode waveform at the outputs,does not give pop effect).

TURN-ON

Fig 39 shows the output waveform (before and after the "A" weighting filter) compared to the value of Csvr.

Better pop-on performance is obtained with higher Csvr values (the recommended range is from 22uF to 220uF).

The turn-on delay (during which the amplifier is in mute condition) is a function essentially of : C_{out} , C_{svr} .

Being:

$$T1 \approx 120 \cdot C_{out}$$

$$T2 \approx 1200 \cdot C_{svr}$$

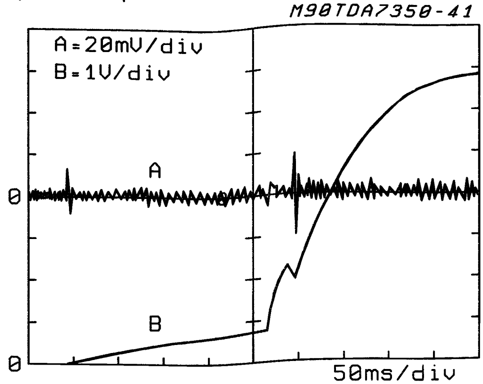
The turn-on delay is given by:

T1+T2 STEREO
T2 BRIDGE

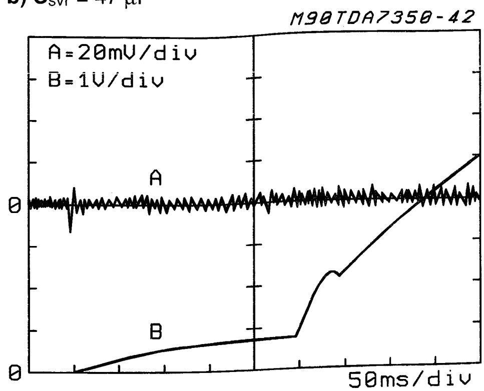
The best performance is obtained by driving the st-by pin with a ramp having a slope slower than 2V/ms

Figure 39:

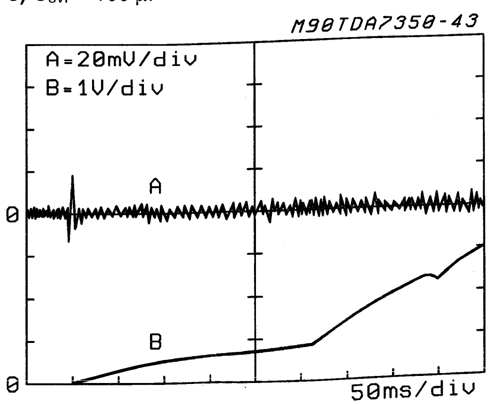
a) C_{svr} = 22 µF



b) C_{svr} = 47 µF



c) C_{svr} = 100 µF



TURN-OFF

A turn-off pop can occur if the st-by pin goes low with a short time constant (this can occur if other car radio sections, preamplifiers,radio.. are supplied through the same st-by switch).
This pop is due to the fast switch-off of the internal current generator of the amplifier.
If the voltage present across the load becomes rapidly zero (due to the fast switch off) a small pop occurs, depending also on Cout,Rload.

The parameters that set the switch off time constant of the st-by pin are:

- the st-by capacitor (Cst-by)
- the SVR capacitor (Csvr)
- resistors connected from st-by pin to ground (Rext)

The time constant is given by :

$T \approx Csvr \cdot 2000\Omega // Rext + Cst\text{-}by \cdot 2500\Omega // Rext$

The suggested time constants are :

$T > 120ms$ with $C_{out}=1000\mu F, R_L = 4ohm$,stereo

$T > 170ms$ with $C_{out}=2200\mu F, R_L = 4ohm$,stereo

If Rext is too low the Csvr can become too high and a different approach may be useful (see next section).

Figg 40, 41 show some types of electronic switches (µP compatible) suitable for supplying the st-by pin (it is important that Qsw is able to saturate with $V_{CE} \leq 150mV$).

Also for turn off pop the bridge configuration is superior, in particular the st-by pin can go low faster.

GLOBAL APPROACH TO SOLVING POP PROBLEM BY USING THE MUTING/TURN ON DELAY FUNCTION

In the real case turn-on and turn-off pop problems are generated not only by the power amplifier,but also (very often) by preamplifiers,tone controls,radios etc. and transmitted by the power amplifier to the loudspeaker.

A simple approach to solving these problems is to use the mute characteristics of the TDA7350.

If the SVR pin is at a voltage below 1.5 V, the mute attenuation (typ)is 30dB .The amplifier is in play mode when Vsvr overcomes 3.5 V.

With the circuit of fig 42 we can mute the amplifier for a time Ton after switch-on and for a time Toff after switch-off.During this period the circuitry that precedes the power amplifier can produce spurious spikes that are not transmitted to the loudspeaker. This can give back a very simple design of this circuitry from the pop point of view.

A timing diagram of this circuit is illustrated in fig 43. Other advantages of this circuit are:

- A reduced time constant allowance of stand-by pin turn off.Consequently it is possible to drive all the car-radio with the signal that drives this pin.

-A better turn-off noise with signal on the output.

To drive two stereo amplifiers with this circuit it is possible to use the circuit of fig 44.

Figure 40

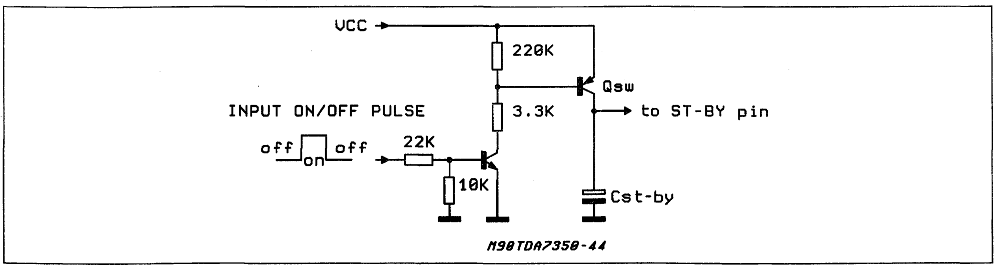


Figure 41

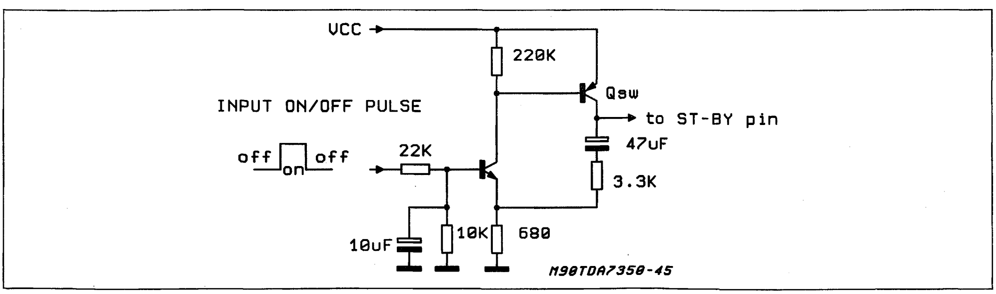


Figure 42

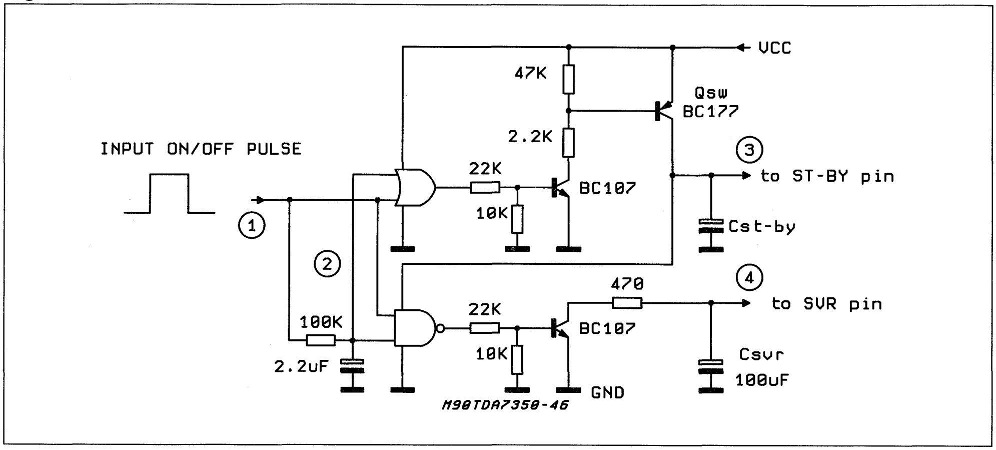


Figure 43

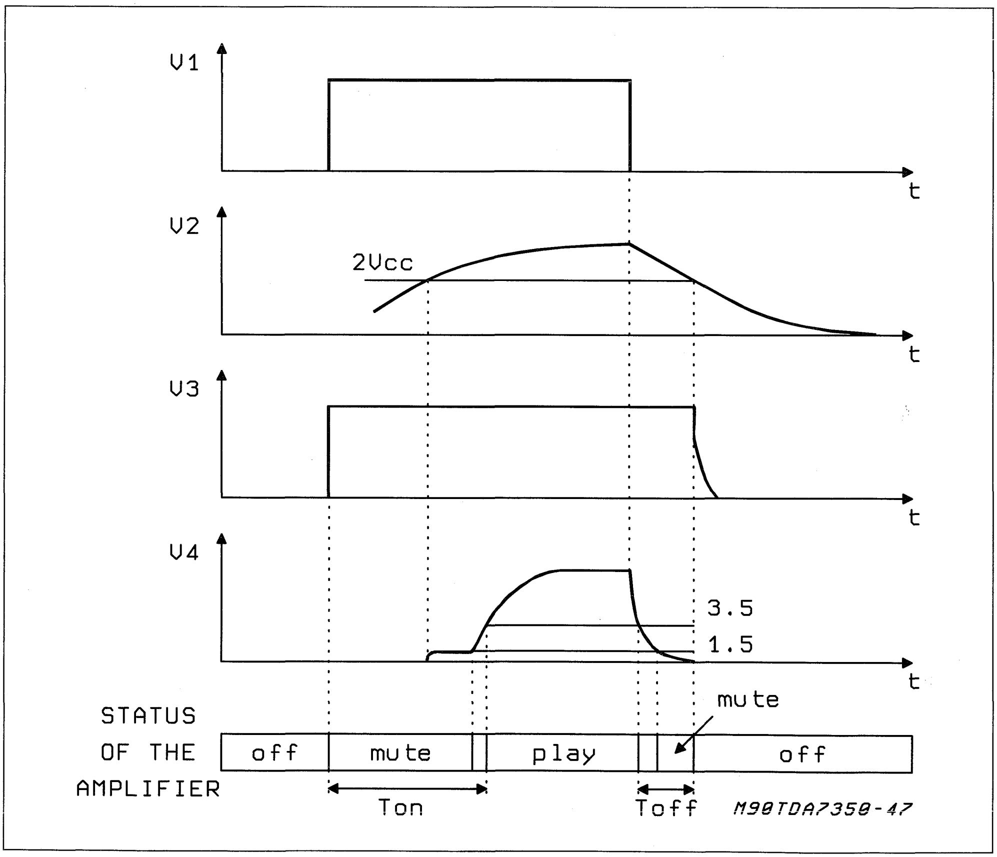
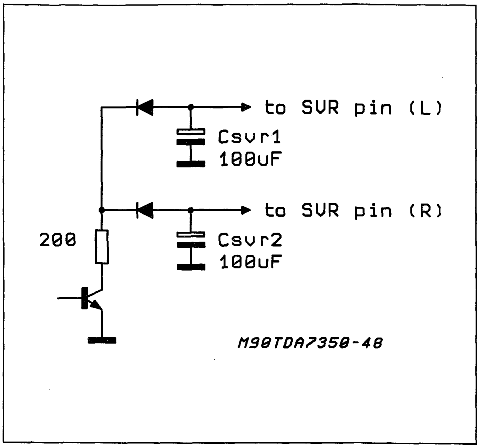


Figure 44



BALANCE INPUT IN BRIDGE CONFIGURATION

A helpful characteristic of the TDA7350 is that,in bridge configuration, a signal present on both the input capacitors is amplified by the same amount and it is present in phase at the outputs,so this signal does not produce effects on the load.The typical value of CMRR is 46 dB.

Looking at fig 45, we can see that a noise signal from the ground of the power amplifier to the ground of the hypothetical preamplifier is amplified of a factor equal to the gain of the amplifier (2 • Gv).

Using a configuration of fig. 46 the same ground noise is present at the output multiplied by the factor 2 • Gv/200.

This means less distortion,less noise (e.g. motor cassette noise) and/or a simplification of the layout of PC board.

The only limitation of this balanced input is the maximum amplitude of common mode signals (few tens of millivolt) to avoid a loss of output power due to the common mode signal on the output, but in a large number of cases this signal is within this range.

HIGH GAIN ,LOW NOISE APPLICATION

The following section describes a flexible preamplifier having the purpose to increase the gain of the TDA7350.

Figure 45

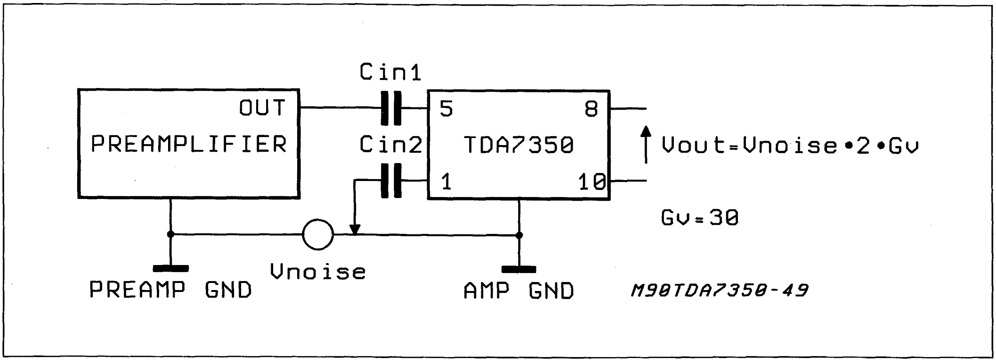
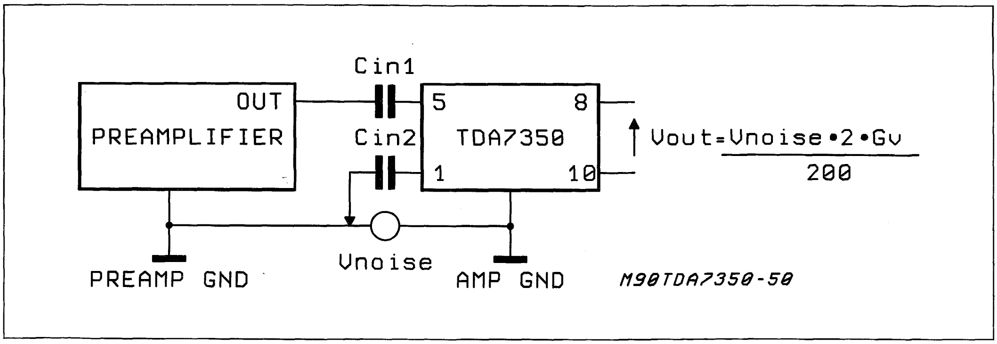


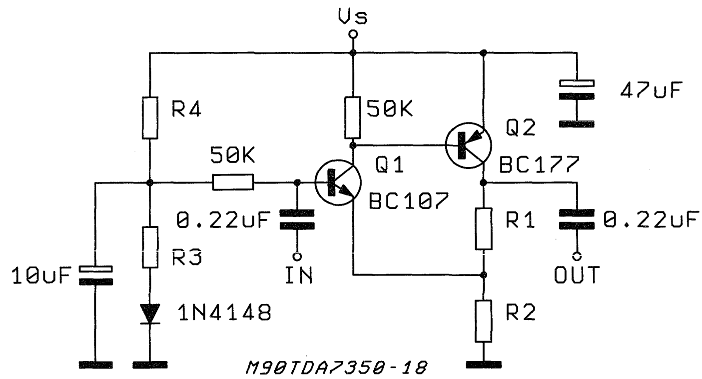
Figure 46



A two transistor network (fig. 47) has been adopted whose components can be changed in order to achieve the desired gain without affecting the good performances of the audio amplifier itself. The recommended values for 40 dB overall gain are :

Resistance	Stereo	Bridge
R1	10KΩ	10KW
R2	4.3KΩ	16KΩ
R3	10KΩ	24KΩ
R4	50KΩ	50KΩ

Figure 47



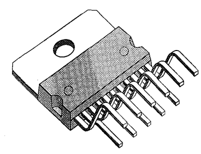
22W BRIDGE-STEREO AMPLIFIER FOR CAR RADIO

ADVANCE DATA

- VERY FEW EXTERNAL COMPONENTS
- NO BOUCHEROT CELLS
- NO BOOSTRAP CAPACITORS
- HIGH OUTPUT POWER
- NO SWITCH ON/OFF NOISE
- VERY LOW STAND-BY CURRENT
- FIXED GAIN (30dB STEREO)
- PROGRAMMABLE TURN-ON DELAY

Protections:

- OUTPUT AC-DC SHORT CIRCUIT TO GROUND AND TO SUPPLY VOLTAGE
- VERY INDUCTIVE LOADS
- LOUDSPEAKER PROTECTION
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GROUND
- ESD



Multiwatt - 11

ORDERING NUMBER: TDA7350A

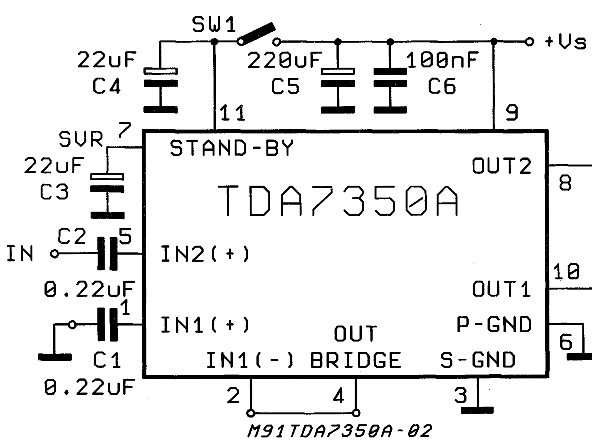
DESCRIPTION

The TDA7350A is a new technology class AB Audio Power Amplifier in the Multiwatt® package designed for car radio applications.

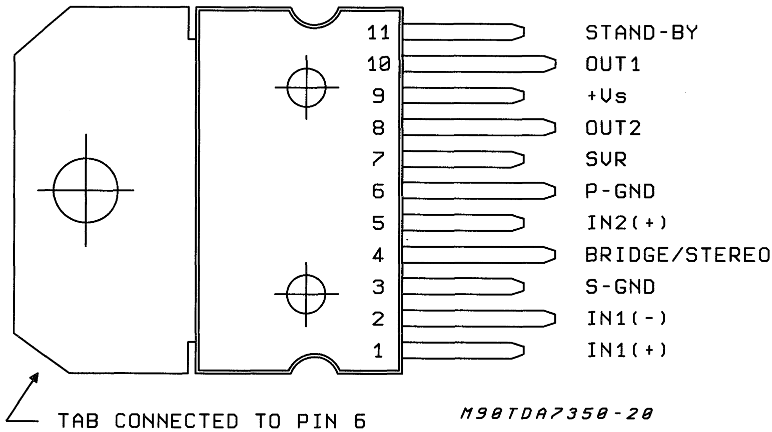
Thanks to the fully complementary PNP/NPN output configuration the high power performance of the TDA7350A is obtained without bootstrap capacitors.

A delayed turn-on mute circuit eliminates audible on/off noise, and a novel short circuit protection system prevents spurious intervention with highly inductive loads.

APPLICATION CIRCUIT BRIDGE



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Operating Supply Voltage	18	V
V_S	DC Supply Voltage	28	V
V_S	Peak Supply Voltage (for t = 50ms)	40	V
I_o	Output Peak Current (non rep. for t = 100µs)	5	A
I_o	Output Peak Current (rep. freq. > 10Hz)	4	A
P_{tot}	Power Dissipation at T_{case} = 85°C	36	W
$T_{stg,TJ}$	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, T_{amb} = 25°C, V_S = 14.4V, f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range		8		18	V
I_d	Total Quiescent Drain Current	stereo configuration			120	mA
A_{SB}	Stand-by attenuation		60	80		dB
I_{SB}	Stand-by Current				100	µA
T_{sd}	Thermal Shut-down Junction Temperature			150		°C

STEREO

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
P_o	Output Power (each channel)	d = 10% R_L = 2Ω R_L = 3.2Ω R_L = 4Ω	 7	 11 8 6.5		 W W W
		d = 10%; V_S = 13.2V R_L = 2Ω R_L = 3.2Ω R_L = 4Ω		 9 6.5 5.5		 W W W
d	Distortion	P_o = 0.1 to 4W; R_L = 3.2Ω			0.5	%
SVR	Supply Voltage Rejection	R_S = 10kΩ, f = 100Hz; C3 = 22µF C3 = 100µF	45	50 57		dB
CT	Crosstalk	f = 1KHz f = 10KHz	45	55 50		dB dB
R_I	Input Resistance		30	50		KΩ
G_V	Voltage Gain		27	29	31	dB
G_V	Voltage Gain Match				1	dB
E_{IN}	Input Noise Voltage	R_S = 50Ω (*) R_S = 10KΩ (*) R_S = 50Ω (**) R_S = 10KΩ (**)		1.5 2 2 2.7	 7	µV µV µV µV

BRIDGE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
P_o	Output Power	d = 10%; R_L = 4Ω d = 10%; R_L = 3.2Ω	 16	20 22		W W
		d = 10%; V_S = 13.2V R_L = 4Ω R_L = 3.2Ω		 17.5 19		 W W
d	Distortion	P_o = 0.1 to 10W; R_L = 4Ω			1	%
V_{OS}	Output Offset Voltage				250	mV
SVR	Supply Voltage Rejection	R_S = 10KΩ, f = 100Hz; C3 = 22µF C3 = 100µF	45	50 57		dB
R_I	Input Resistance			50		KΩ
G_V	Voltage Gain		33	35	37	dB
E_{IN}	Input Noise Voltage	R_S = 50Ω (*) R_S = 10KΩ (*) R_S = 50Ω (**) R_S = 10KΩ (**)		2 2.5 2.7 3.2		µV µV µV µV

(*) Curve A
(**) 22Hz to 22KHz

Figure 1: STEREO Test and Appication Circuit

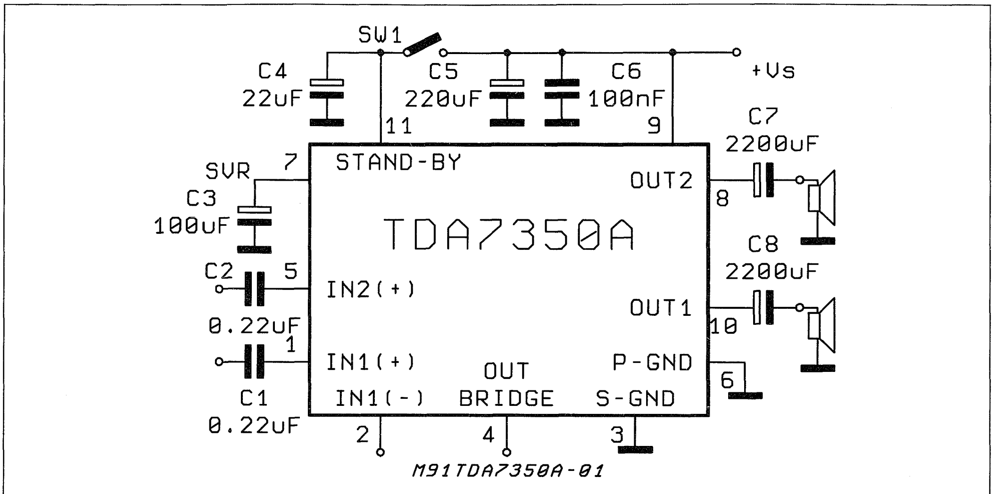


Figure 2: P.C. Board and Layout (STEREO) of the circuit of fig. 1 (1:1 scale)

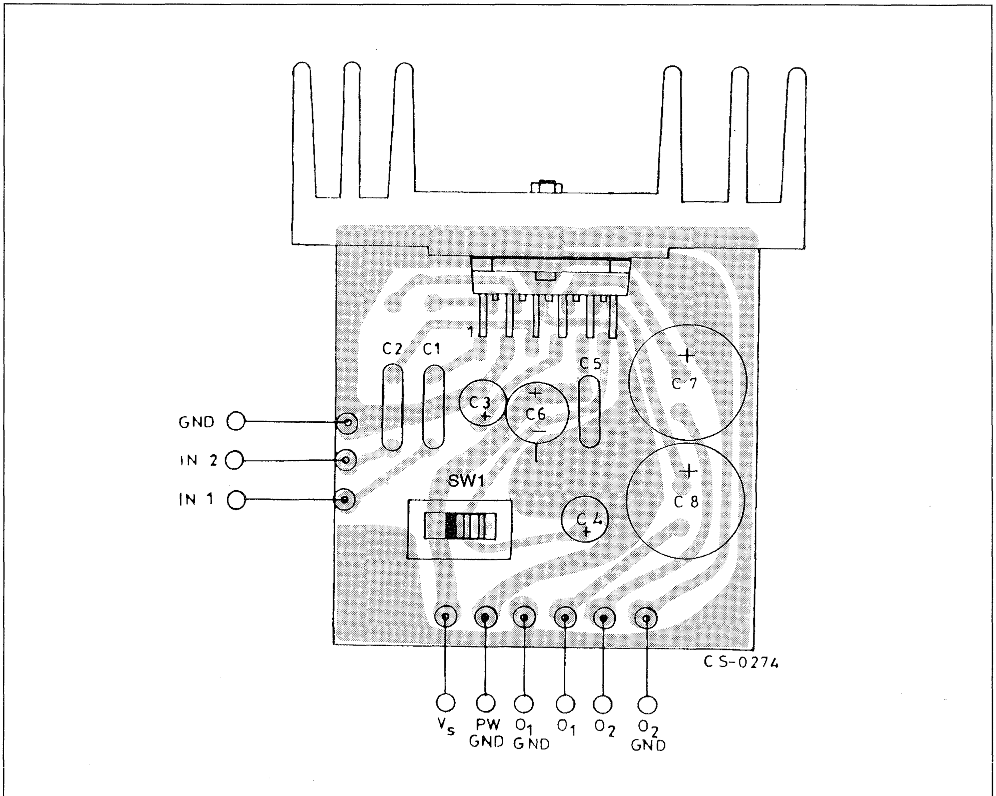


Figure 3: BRIDGE Test and Appication Circuit

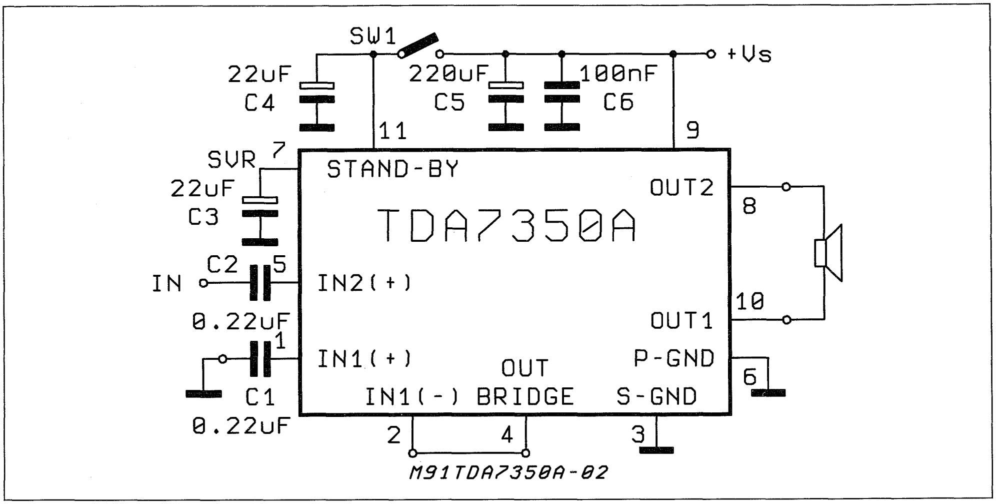
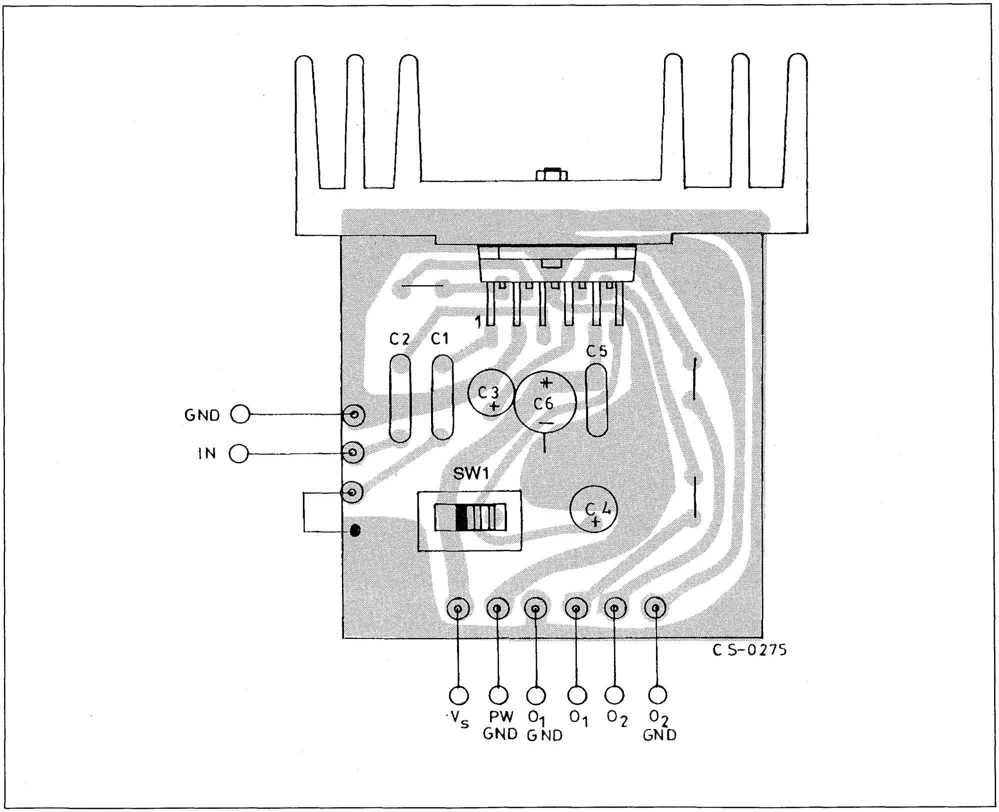


Figure 4: P.C. Board and Layout (BRIDGE) of the circuit of fig. 3 (1:1 scale)



RECOMMENDED VALUES OF THE EXTERNAL COMPONENTS (ref to the Stereo Test and Application Circuit)

Component	Recommended Value	Purpose	Larger than the Recomm. Value	Smaller than the Recomm. Value
C1	0.22µF	Input Decoupling (CH1)	—	—
C2	0.22µF	Input Decoupling (CH2)	—	—
C3	100µF	Supply Voltage Rejection Filtering Capacitor	Longer Turn-On Delay Time	Worse Supply Voltage Rejection. Shorter Turn-On Delay Time Danger of Noise (POP)
C4	22µF	Stand-By ON/OFF Delay	Delayed Turn-Off by Stand-By Switch	Danger of Noise (POP)
C5	220µF (min)	Supply By-Pass		Danger of Oscillations
C6	100nF (min)	Supply By-Pass		Danger of Oscillations
C7	2200µF	Output Decoupling CH2	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay
C8	2200µF	Output Decoupling CH1	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay

Figure 5: Output Power vs. Supply Voltage (Stereo)

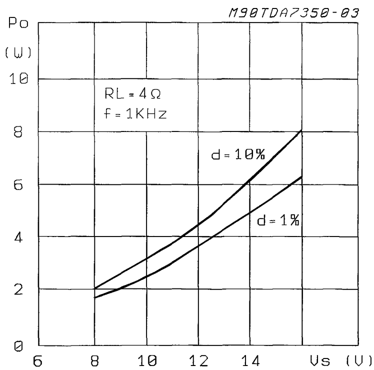


Figure 6: Output Power vs. Supply Voltage (Stereo)

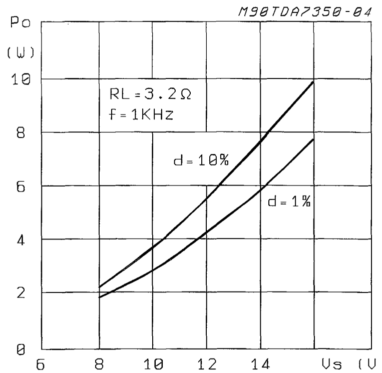


Figure 7: Output Power vs. Supply Voltage (Stereo)

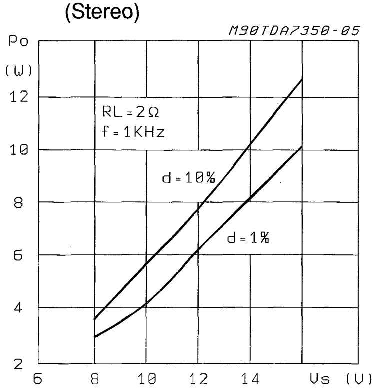


Figure 8: Output Power vs. Supply Voltage (Bridge)

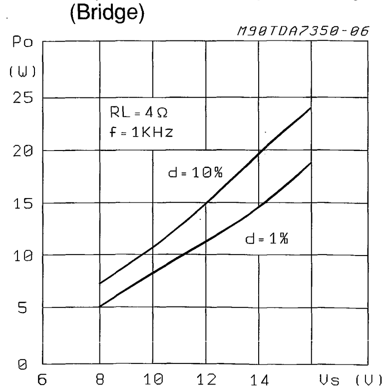


Figure 9: Output Power vs. Supply Voltage (Bridge)

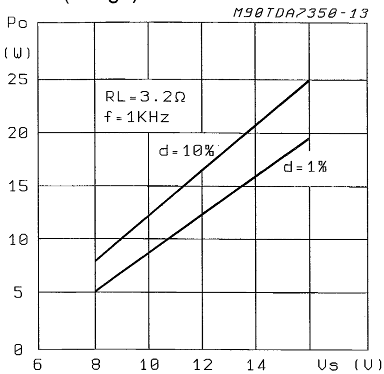


Figure 10: Drain Current vs Supply Voltage (Stereo)

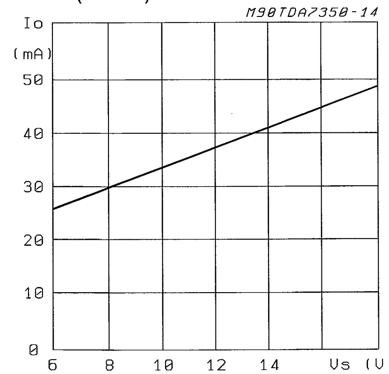


Figure 11: Distortion vs Output Power (Stereo)

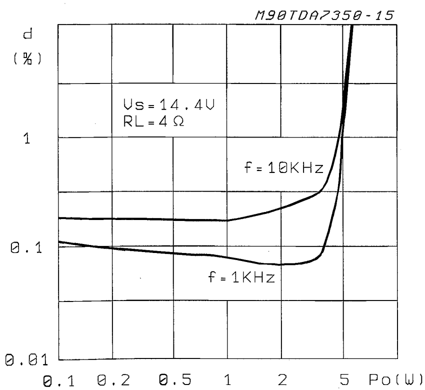


Figure 12: Distortion vs Output Power (Stereo)

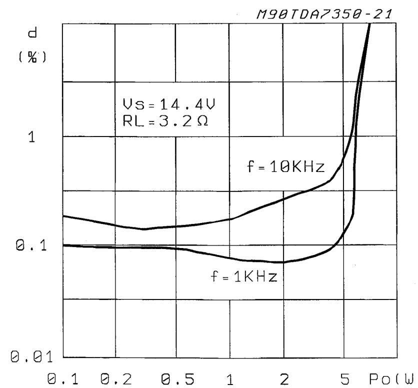


Figure 13: Distortion vs Output Power (Stereo)

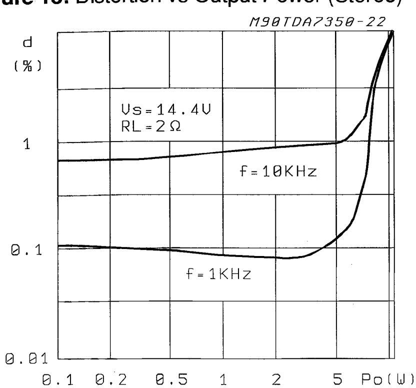


Figure 14: Distortion vs Output Power (Bridge)

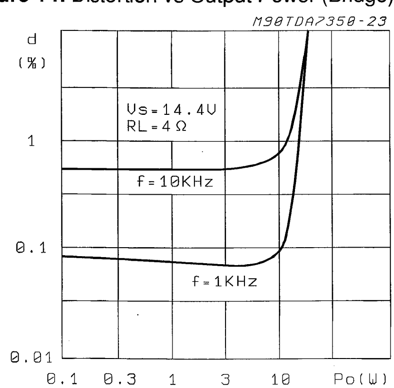


Figure 15: SVR vs. Frequency & C_{SVR} (Stereo)

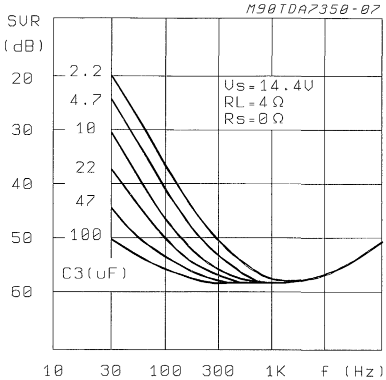


Figure 16: SVR vs. Frequency & C_{SVR}; (Stereo)

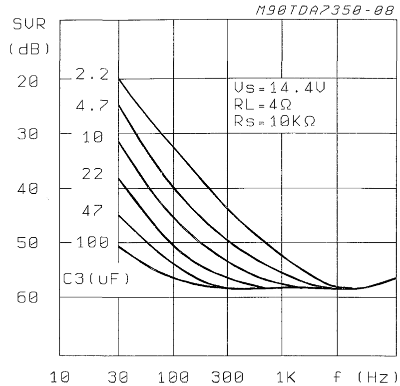


Figure 17: SVR vs. Frequency & C_{SVR}; (Bridge)

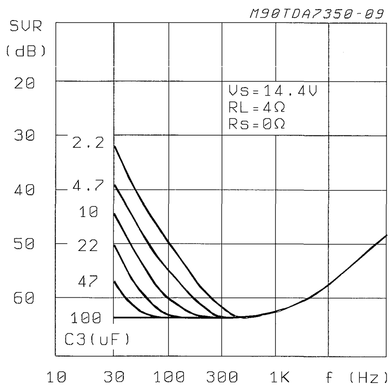


Figure 18: SVR vs. Frequency & C_{SVR}; (Bridge)

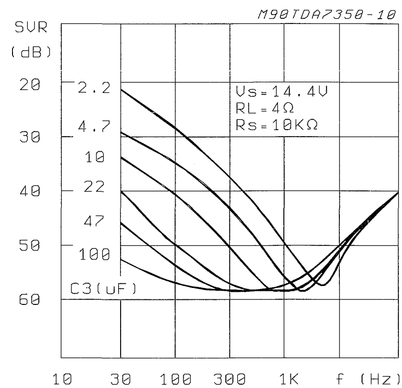


Figure 19: Crosstalk vs. Frequency (Stereo)

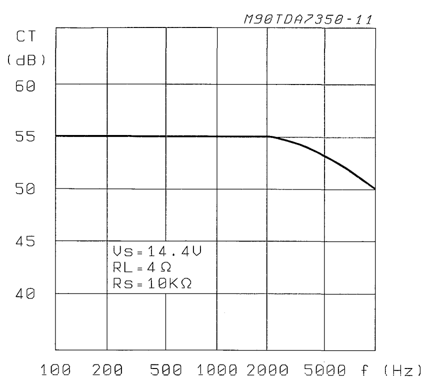


Figure 20: Power Dissipation & Efficiency vs. Output Power (Stereo)

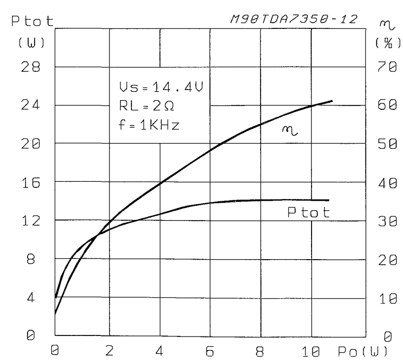


Figure 21: Power Dissipation & Efficiency vs. Output Power (Stereo)

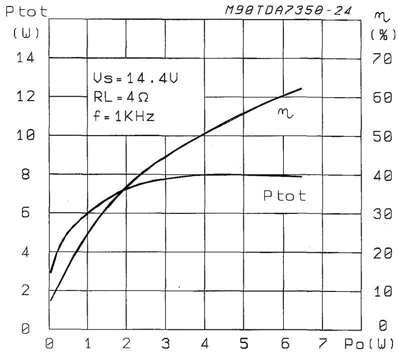


Figure 22: Power Dissipation & Efficiency vs. Output Power (Bridge)

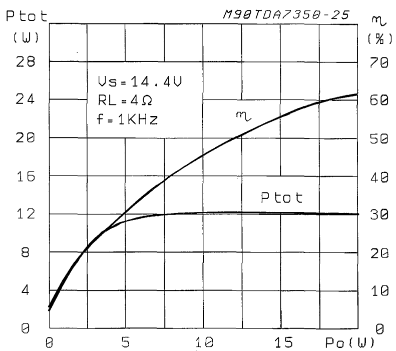
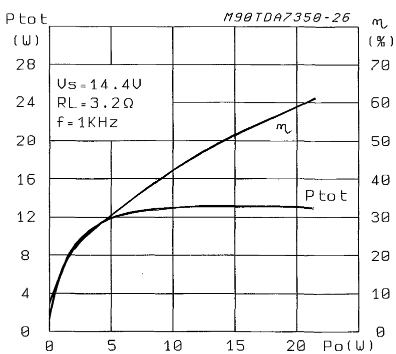


Figure 23: Power Dissipation & Efficiency vs. Output Power (Bridge)



AMPLIFIER ORGANIZATION

The TDA7350A has been developed taking care of the key concepts of the modern power audio amplifier for car radio such as: space and costs saving due to the minimized external count, excellent electrical performances, flexibility in use, superior reliability thanks to a built-in array of protections. As a result the following performances has been achieved:

- NO NEED OF BOOTSTRAP CAPACITORS EVEN AT THE HIGHEST OUTPUT POWER LEVELS
- ABSOLUTE STABILITY WITHOUT EXTERNAL COMPENSATION THANKS TO THE INNOVATIVE OUT STAGE CONFIGURATION, ALSO ALLOWING INTERNALLY FIXED CLOSED LOOP LOWER THAN COMPETITORS
- LOW GAIN (30dB STEREO FIXED WITHOUT ANY EXTERNAL COMPONENTS) IN ORDER TO MINIMIZE THE OUTPUT NOISE AND OPTIMIZE SVR
- SILENT MUTE/ST-BY FUNCTION FEATURING ABSENCE OF POP ON/OFF NOISE
- HIGH SVR
- STEREO/BRIDGE OPERATION WITHOUT ADDITION OF EXTERNAL COMPONENT
- AC/DC SHORT CIRCUIT PROTECTION (TO GND, TO V_S, ACROSS THE LOAD)
- LOUDSPEAKER PROTECTION
- DUMP PROTECTION
- ESD PROTECTION

BLOCK DESCRIPTION

Polarization

The device is organized with the gain resistors directly connected to the signal ground pin i.e. without gain capacitors (fig. 24).

The non inverting inputs of the amplifiers are connected to the SVR pin by means of resistor dividers, equal to the feedback networks. This allows the outputs to track the SVR pin which is sufficiently slow to avoid audible turn-on and turn-off transients.

SVR

The voltage ripple on the outputs is equal to the one on SVR pin: with appropriate selection of C_{SVR}, more than 55dB of ripple rejection can be obtained.

Delayed Turn-on (muting)

The C_{SVR} sets a signal turn-on delay too. A circuit is included which mutes the device until the voltage on SVR pin reaches ~2.5V typ (fig. 25). The mute function is obtained by duplicating the input differential pair (fig. 26): it can be switched to the signal source or to an internal mute input. This feature is necessary to prevent transients at the inputs reaching the loudspeaker(s) immediately

after power-on).
Fig. 25 represents the detailed turn-on transient with reference to the stereo configuration.
At the power-on the output decoupling capacitors are charged through an internal path but the device itself remains switched off (Phase 1 of the represented diagram).
When the outputs reach the voltage level of about 1V (this means that there is no presence of short circuits) the device switches on, the SVR capacitor starts charging itself and the output tracks exactly the SVR pin.
During this phase the device is muted until the SVR reaches the "Play" threshold (~2.5V typ.), after that the music signal starts being played.

Stereo/Bridge Switching
There is also no need for external components for changing from stereo to bridge configuration (figg. 24-27).
A simple short circuit between two pins allows phase reversal at one output, yet maintaining the quiescent output voltage.

Stand-by
The device is also equipped with a stand-by function, so that a low current, and hence low cost switch, can be used for turn on/off.

Stability
The device is provided with an internal compensation wich allows to reach low values of closed loop gain.
In this way better performances on S/N ratio and SVR can be obtained.

Figure 24: Block Diagram; Stereo Configuration

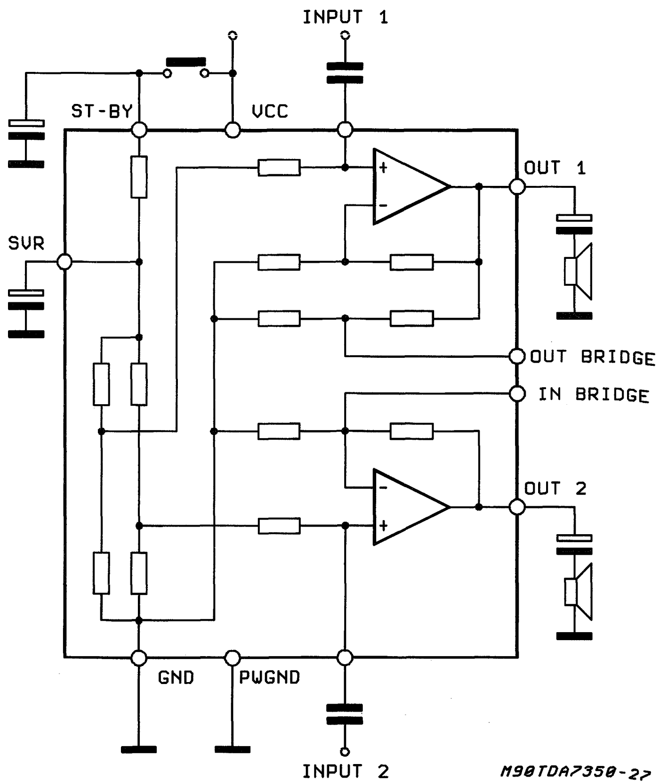


Figure 25: Turn-on Delay Circuit

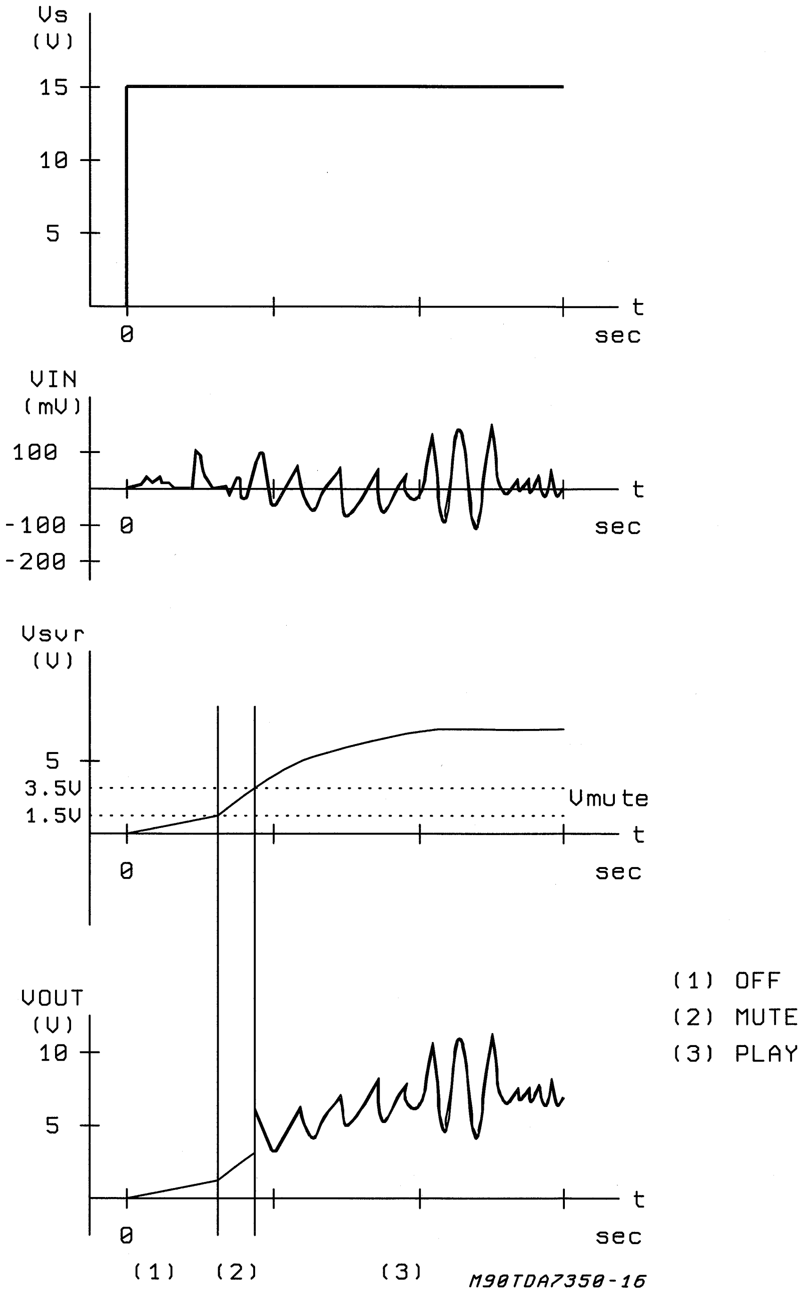


Figure 26: Mute Function Diagram

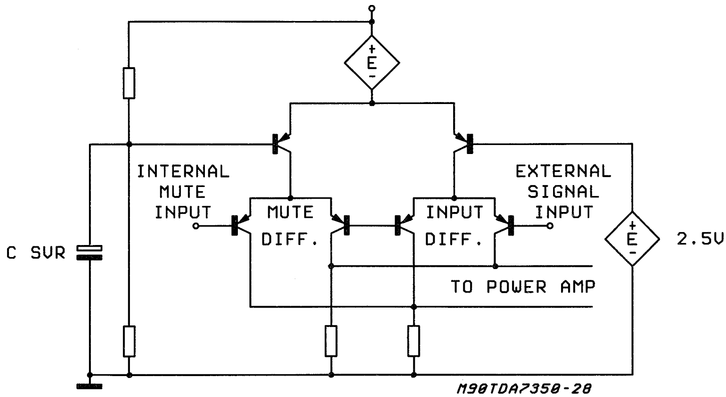


Figure 27: Block Diagram; Bridge Configuration

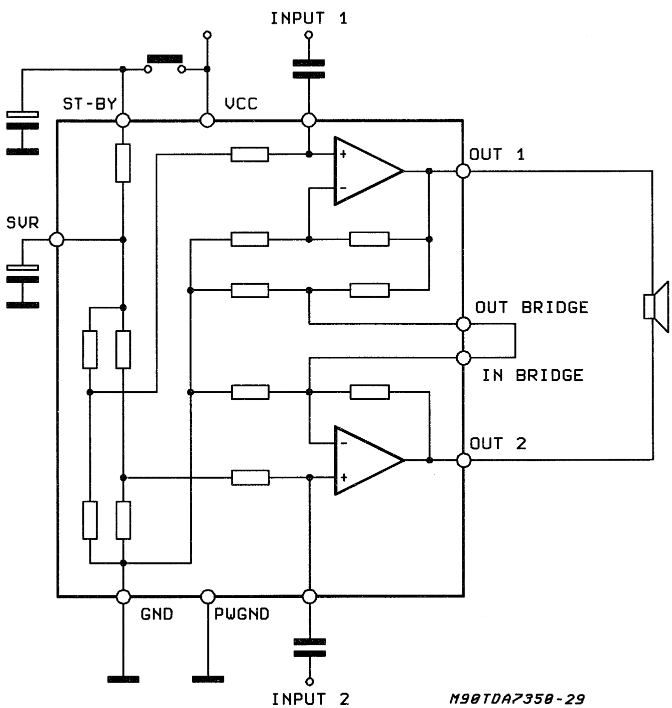


Figure 28: ICV - PNP Gain vs. I_C

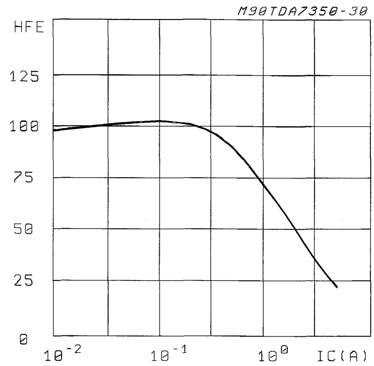


Figure 29: ICV - PNP $V_{CE(sat)}$ vs. I_C

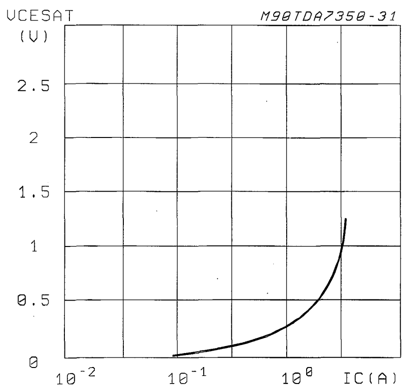
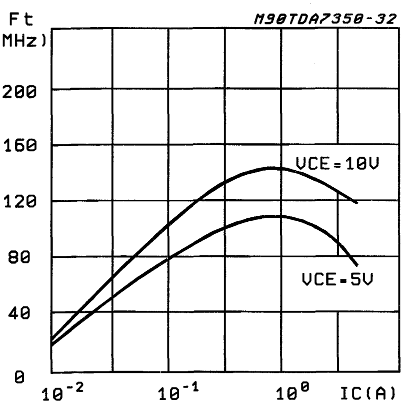


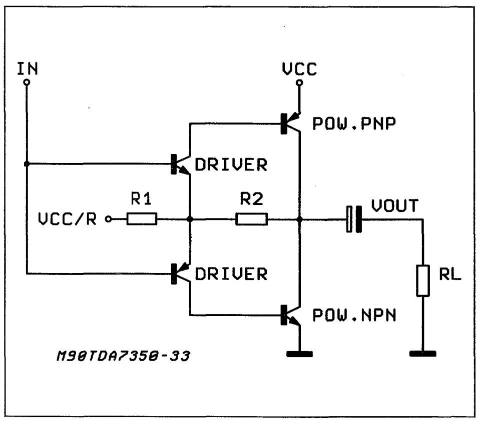
Figure 30: ICV - PNP cut-off frequency vs. I_C



OUTPUT STAGE

Poor current capability and low cutoff frequency are well known limits of the standard lateral PNP. Composite PNP-NPN power output stages have been widely used, regardless their high saturation drop. This drop can be overcome only at the expense of external components, namely, the bootstrap capacitors. The availability of 4A isolated collector PNP (ICV PNP) adds versatility to the design. The performance of this component, in terms of gain, V_{CEsat} and cut-off frequency, is shown in fig. 28, 29, 30 respectively. It is realized in a new bipolar technology, characterized by top-bottom isolation techniques, allowing the implementation of low leakage diodes, too. It guarantees BV_{CEO} > 20V and BV_{CBO} > 50V both for NPN and PNP transistors. Basically, the connection shown in fig. 31 has been chosen. First of all because its voltage swing is rail-to-rail, limited only by the VCEsat of the output transistors, which are in the range of 0.3Ω each. Then, the gain VOUT/VIN is greater than unity, approximately 1+R2/R1. (VCC/2 is fixed by an auxiliary amplifier common to both channel). It is possible, controlling the amount of this local feedback, to force the loop gain (A . β) to less than unity at frequencies for which the phase shift is 180˚. This means that the output buffer is intrinsically stable and not prone to oscillation.

Figure 31: The New Output Stage



In contrast, with the circuit of fig. 32, the solution adopted to reduce the gain at high frequencies is the use of an external RC network.

AMPLIFIER BLOCK DIAGRAM

The block diagram of each voltage amplifier is shown in fig. 33. Regardless of production spread, the current in each final stage is kept low, with enough margin on the minimum, below which cross-over distortion would appear.

Figure 32: A Classical Output Stage

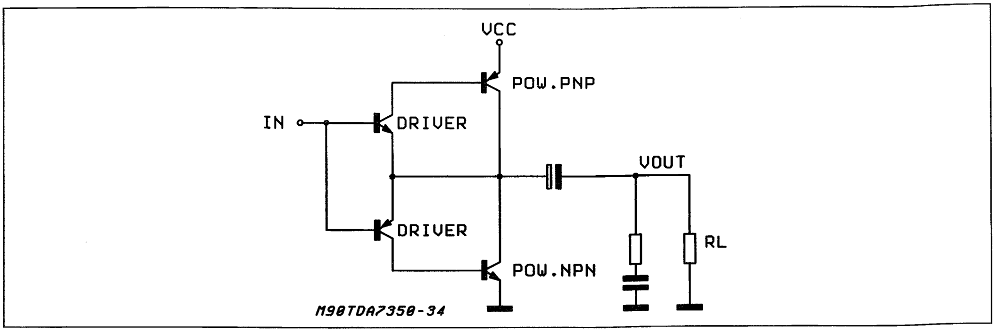
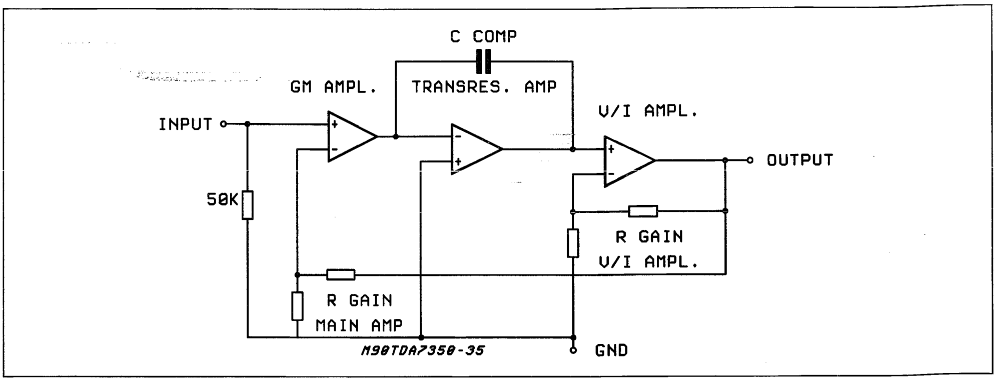


Figure 33: Amplifier Block Diagram



BUILT-IN PROTECTION SYSTEMS

Short Circuit Protection

The maximum current the device can deliver can be calculated by considering the voltage that may be present at the terminals of a car radio amplifier and the minimum load impedance.

Apart from consideration concerning the area of the power transistors it is not difficult to achieve peak currents of this magnitude (5A peak).
However, it becomes more complicated if AC and DC short circuit protection is also required.In particular,with a protection circuit which limits the output current following the SOA curve of the output transistors it is possible that in some conditions (highly reactive loads, for example) the protection circuit may intervene during normal operation. For this reason each amplifier has been equipped with a protection circuit that intervenes when the output current exceeds 4A.

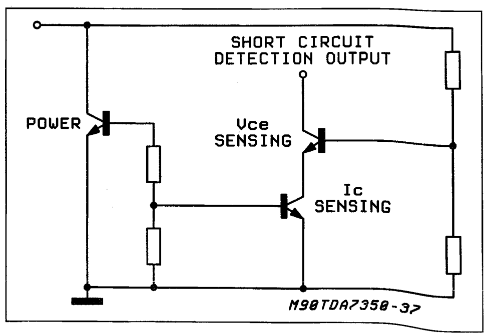
Fig 34 shows the protection circuit for an NPN power transistor (a symmetrical circuit applies to PNP).The VBE of the power is monitored and gives out a signal,available through a cascode.

This cascode is used to avoid the intervention of the short circuit protection when the saturation is below a given limit.

The signal sets a flip-flop which forces the amplifier outputs into a high impedance state.

In case of DC short circuit when the short circuit is removed the flip-flop is reset and restarts the circuit (fig. 38). In case of AC short circuit or load shorted in Bridge configuration, the device is continuously switched in ON/OFF conditions and the current is limited.

Figure 34: Circuitry for Short Circuit Detection



Load Dump Voltage Surge

The TDA 7350A has a circuit which enables it to withstand a voltage pulse train on pin 9, of the type shown in fig. 36.
If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.

A suggested LC network is shown in fig. 35.
With this network, a train of pulses with amplitude up to 120V and width of 2ms can be applied at point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Polarity Inversion

Figure 35

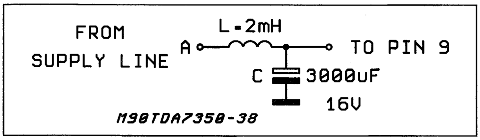
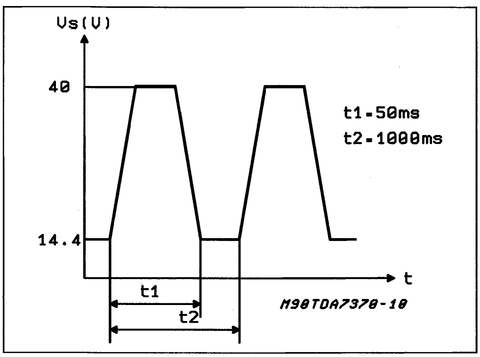


Figure 36



High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This features is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open Ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA7350A protection diodes are included to avoid any damage.

DC Voltage

The maximum operating DC voltage for the TDA7350A is 18V. However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

Thermal Shut-down

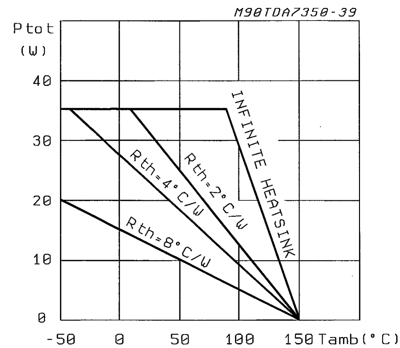
The presence of a thermal limiting circuit offers the following advantages:

1)an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2)the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 37 shows the dissipable power as a function of ambient temperature for different thermal resistance.

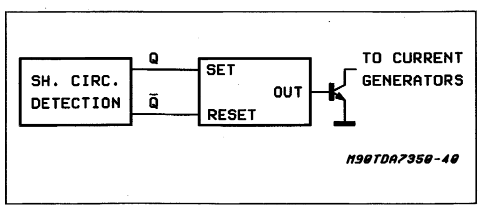
Figure 37: Maximum Allowable Power Dissipation vs. Ambient Temperature



Loudspeaker Protection

The TDA7350A guarantees safe operations even for the loudspeaker in case of accidental shortcircuit.
Whenever a single OUT to GND, OUT to V_S short circuit occurs both the outputs are switched OFF so limiting dangerous DC current flowing through the loudspeaker.

Figure 38: Restart Circuit



APPLICATION HINTS

This section explains briefly how to get the best from the TDA7350A and presents some application circuits with suggestions for the value of the components.These values can change depending on the characteristics that the designer of the car radio wants to obtain,or other parts of the car radio that are connected to the audio block.

To optimize the performance of the audio part it is useful (or indispensable) to analyze also the parts outside this block that can have an interconnection with the amplifier.

This method can provide components and system cost saving.

Reducing Turn On-Off Pop

The TDA7350A has been designed in a way that the turn on(off) transients are controlled through the charge(discharge) of the Csvr capacitor.

As a result of it, the turn on(off) transient spectrum contents is limited only to the subsonic range.The following section gives some brief notes to get the best from this design feature(it will refer mainly to the stereo application which appears to be in most cases the more critical from the pop viewpoint.The bridge connection in fact,due to the common mode waveform at the outputs,does not give pop effect).

TURN-ON

Fig. 39 shows the output waveform (before and after the "A" weighting filter) compared to the value of Csvr.

Better pop-on performance is obtained with higher Csvr values (the recommended range is from 22uF to 220uF).

The turn-on delay (during which the amplifier is in mute condition) is a function essentially of : C_{out}, C_{svr}.

Being:

$$T1 \approx 120 \cdot C_{out}$$

$$T2 \approx 1200 \cdot C_{svr}$$

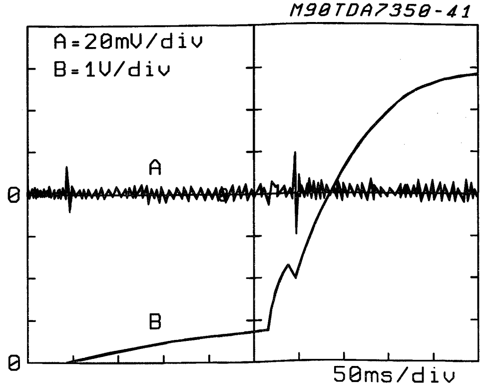
The turn-on delay is given by:

T1+T2	STEREO
T2	BRIDGE

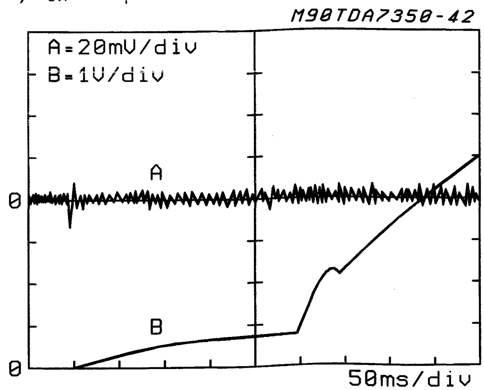
The best performance is obtained by driving the st-by pin with a ramp having a slope slower than 2V/ms

Figure 39:

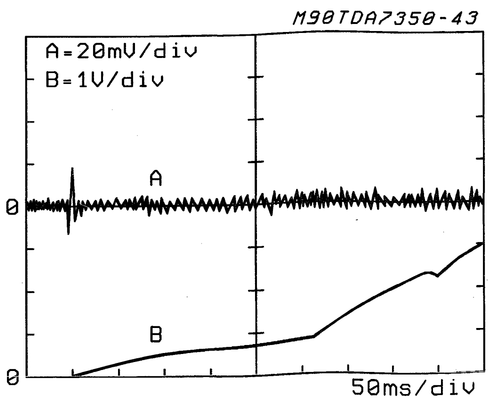
a) C_{svr} = 22 µF



b) C_{svr} = 47 µF



c) C_{svr} = 100 µF



TURN-OFF

A turn-off pop can occur if the st-by pin goes low with a short time constant (this can occur if other car radio sections, preamplifiers,radio.. are supplied through the same st-by switch).
This pop is due to the fast switch-off of the internal current generator of the amplifier.
If the voltage present across the load becomes rapidly zero (due to the fast switch off) a small pop occurs, depending also on Cout,Rload.

The parameters that set the switch off time constant of the st-by pin are:

- the st-by capacitor (Cst-by)
- the SVR capacitor (Csvr)
- resistors connected from st-by pin to ground (Rext)

The time constant is given by :

$T \approx Csvr \cdot 2000\Omega // Rext + Cst\text{-}by \cdot 2500\Omega // Rext$

The suggested time constants are :

$T > 120ms$ with $C_{out}=1000\mu F, R_L = 4ohm$,stereo

$T > 170ms$ with $C_{out}=2200\mu F, R_L = 4ohm$,stereo

If Rext is too low the Csvr can become too high and a different approach may be useful (see next section).

Figg 40, 41 show some types of electronic switches (µP compatible) suitable for supplying the st-by pin (it is important that Qsw is able to saturate with $V_{CE} \leq 150mV$).

Also for turn off pop the bridge configuration is superior, in particular the st-by pin can go low faster.

GLOBAL APPROACH TO SOLVING POP PROBLEM BY USING THE MUTING/TURN ON DELAY FUNCTION

In the real case turn-on and turn-off pop problems are generated not only by the power amplifier,but also (very often) by preamplifiers,tone controls,radios etc. and transmitted by the power amplifier to the loudspeaker.

A simple approach to solving these problems is to use the mute characteristics of the TDA7350.

If the SVR pin is at a voltage below 1.5 V, the mute attenuation (typ)is 30dB .The amplifier is in play mode when Vsvr overcomes 3.5 V.

With the circuit of fig 42 we can mute the amplifier for a time Ton after switch-on and for a time Toff after switch-off.During this period the circuitry that precedes the power amplifier can produce spurious spikes that are not transmitted to the loudspeaker. This can give back a very simple design of this circuitry from the pop point of view.

A timing diagram of this circuit is illustrated in fig 43. Other advantages of this circuit are:

- A reduced time constant allowance of stand-by pin turn off.Consequently it is possible to drive all the car-radio with the signal that drives this pin.

-A better turn-off noise with signal on the output.

To drive two stereo amplifiers with this circuit it is possible to use the circuit of fig 44.

Figure 40

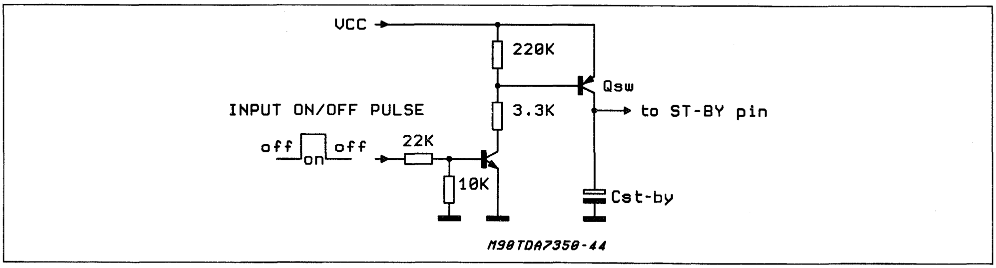


Figure 41

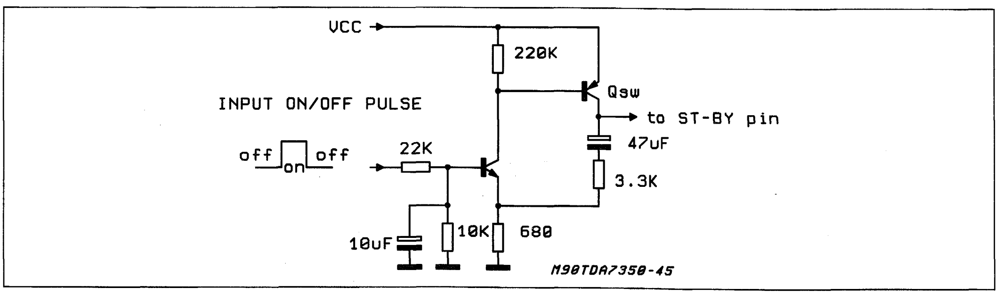


Figure 42

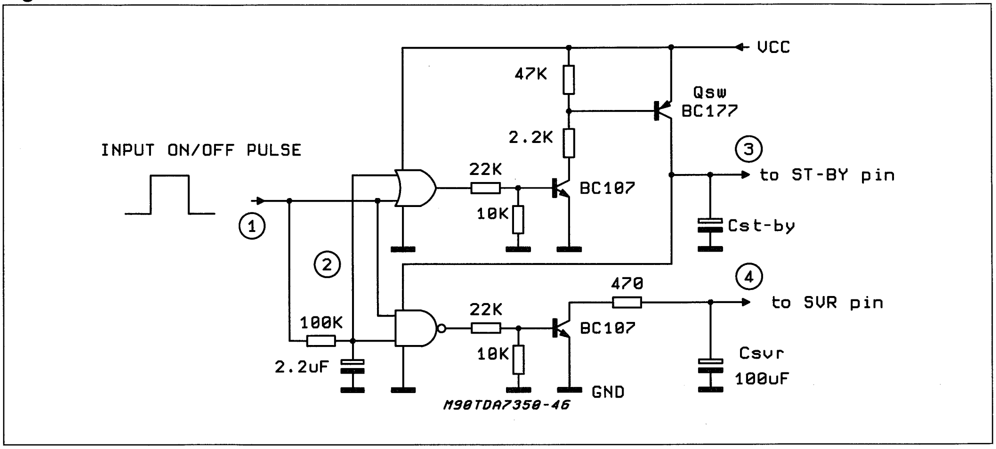


Figure 43

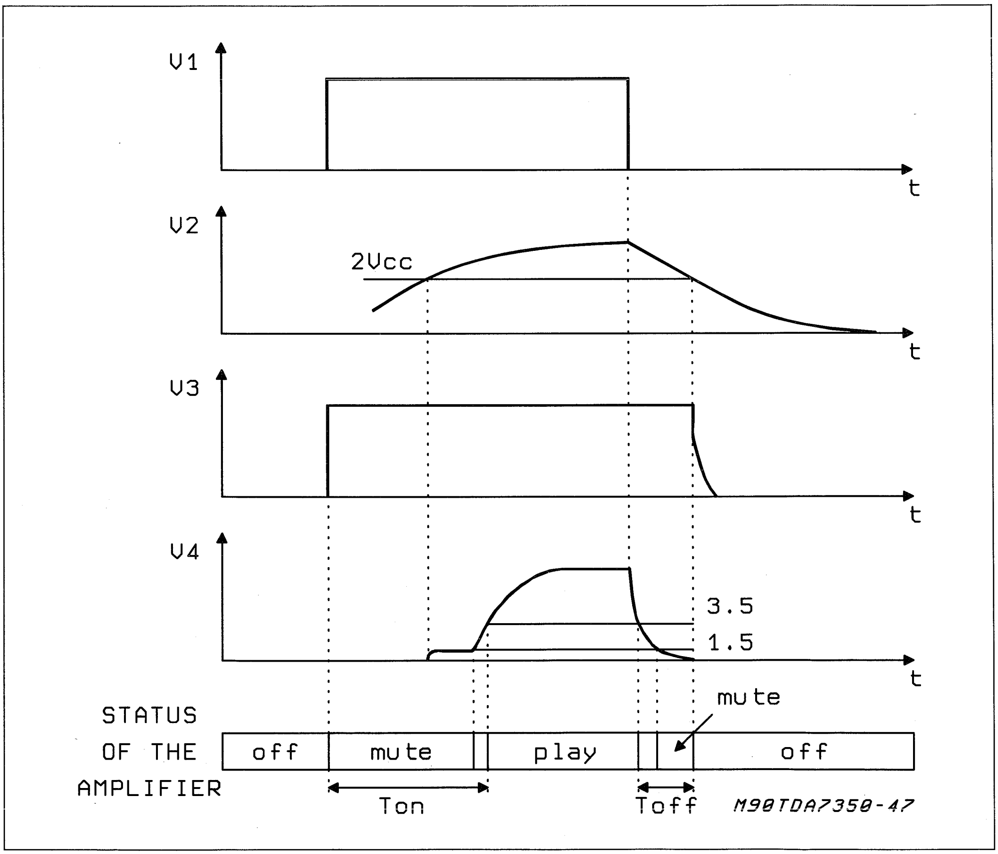
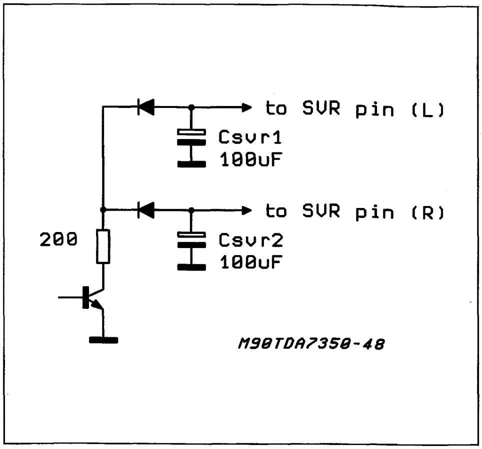


Figure 44



BALANCE INPUT IN BRIDGE CONFIGURATION

A helpful characteristic of the TDA7350A is that,in bridge configuration, a signal present on both the input capacitors is amplified by the same amount and it is present in phase at the outputs,so this signal does not produce effects on the load.The typical value of CMRR is 46 dB.

Looking at fig 45, we can see that a noise signal from the ground of the power amplifier to the ground of the hypothetical preamplifier is amplified of a factor equal to the gain of the amplifier (2 • Gv).

Using a configuration of fig. 46 the same ground noise is present at the output multiplied by the factor 2 • Gv/200.

This means less distortion,less noise (e.g. motor cassette noise) and/or a simplification of the layout of PC board.

The only limitation of this balanced input is the maximum amplitude of common mode signals (few tens of millivolt) to avoid a loss of output power due to the common mode signal on the output, but in a large number of cases this signal is within this range.

HIGH GAIN ,LOW NOISE APPLICATION

The following section describes a flexible preamplifier having the purpose to increase the gain of the TDA7350A.

Figure 45

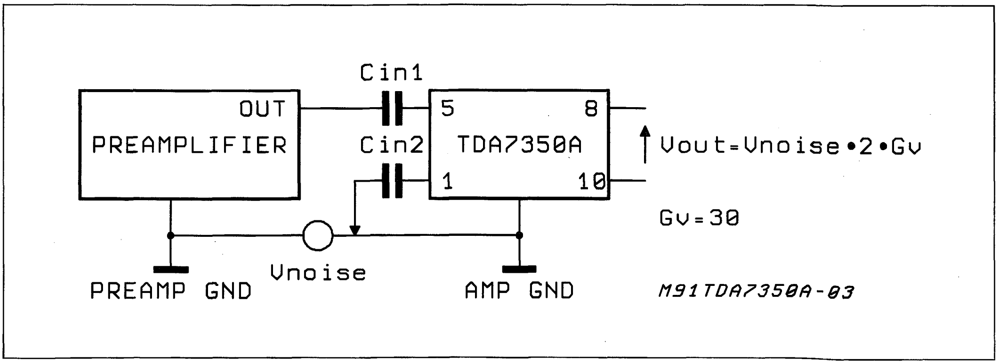
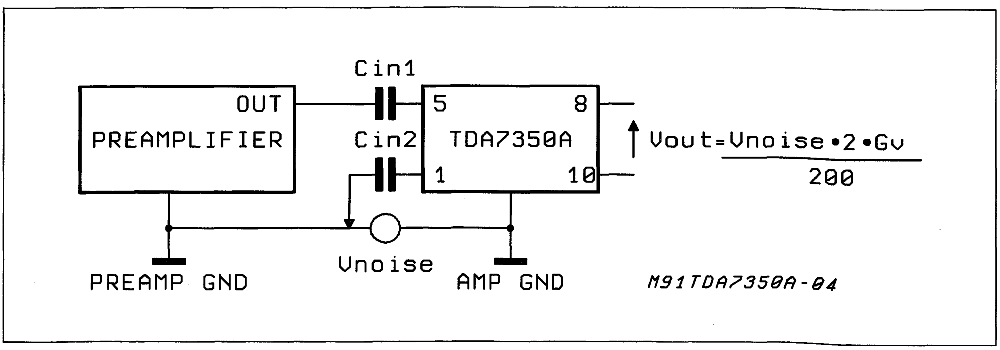


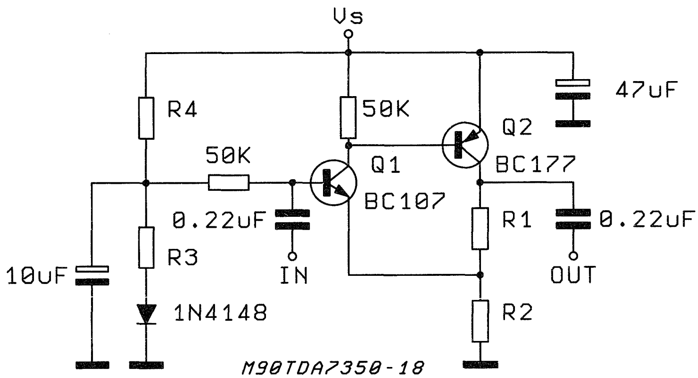
Figure 46



A two transistor network (fig. 47) has been adopted whose components can be changed in order to achieve the desired gain without affecting the good performances of the audio amplifier itself. The recommended values for 40 dB overall gain are :

Resistance	Stereo	Bridge
R1	10KΩ	10KW
R2	4.3KΩ	16KΩ
R3	10KΩ	24KΩ
R4	50KΩ	50KΩ

Figure 47

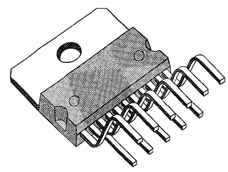


24W BRIDGE-STEREO AMPLIFIER FOR CAR RADIO

ADVANCE DATA

- VERY FEW EXTERNAL COMPONENTS
- NO BOUCHEROT CELLS
- NO BOOSTRAP CAPACITORS
- HIGH OUTPUT POWER
- NO SWITCH ON/OFF NOISE
- VERY LOW STAND-BY CURRENT
- FIXED GAIN (30dB STEREO)
- PROGRAMMABLE TURN-ON DELAY

Protections:
- OUTPUT AC-DC SHORT CIRCUIT TO GROUND AND TO SUPPLY VOLTAGE
- VERY INDUCTIVE LOADS
- LOUDSPEAKER PROTECTION
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GROUND
- ESD



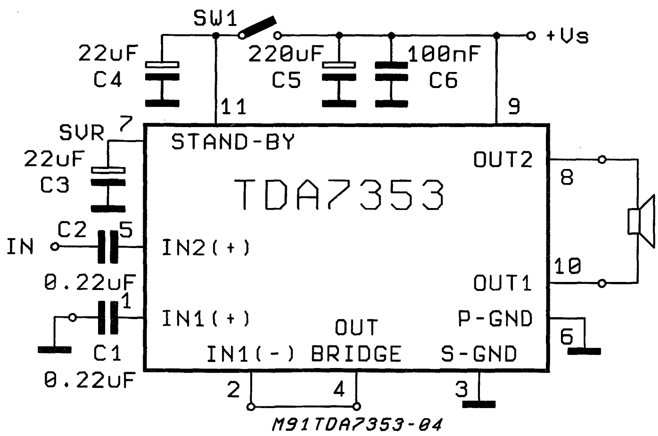
Multiwatt - 11

ORDERING NUMBER: TDA7353

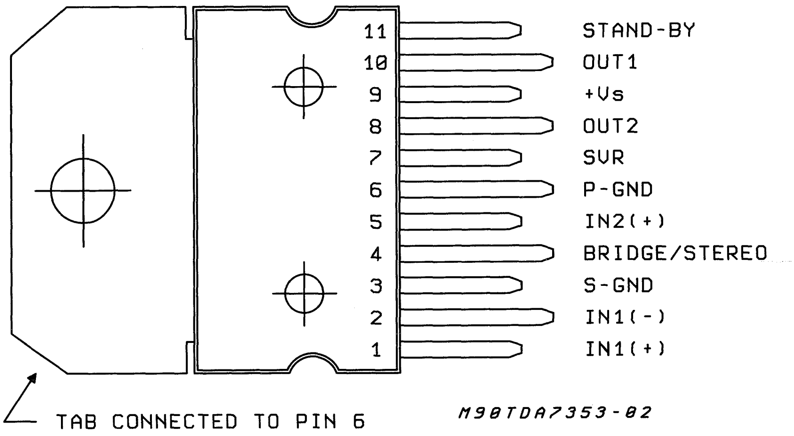
DESCRIPTION

The TDA7353 is a new technology class AB Audio Power Amplifier in the Multiwatt® package designed for car radio applications.
Thanks to the fully complementary PNP/NPN output configuration the high power performance of the TDA7353 is obtained without bootstrap capacitors.
A delayed turn-on mute circuit eliminates audible on/off noise, and a novel short circuit protection system prevents spurious intervention with highly inductive loads.

BRIDGE APPLICATION CIRCUIT



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Operating Supply Voltage	18	V
V_S	DC Supply Voltage	28	V
V_S	Peak Supply Voltage (for t = 50ms)	40	V
I_o	Output Peak Current (non rep. for t = 100µs)	5	A
I_o	Output Peak Current (rep. freq. > 10Hz)	4	A
P_{tot}	Power Dissipation at T_{case} = 85°C	36	W
T_{stg}, T_J	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, T_{amb} = 25°C, V_S = 14.4V, f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range		8		18	V
I_d	Total Quiescent Drain Current	stereo configuration			120	mA
A_{SB}	Stand-by attenuation		60	80		dB
I_{SB}	Stand-by Current				100	µA
T_{sd}	Thermal Shut-down Junction Temperature			150		°C

STEREO

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
P_o	Output Power (each channel)	d = 10% R_L = 1.6Ω R_L = 2Ω R_L = 3.2Ω R_L = 4Ω	 7	 13 11 8 6.5		 W W W W
		d = 10%; V_S = 13.2V R_L = 1.6Ω R_L = 2Ω R_L = 3.2Ω R_L = 4Ω		 10 9 6.5 5.5		 W W W W
d	Distortion	P_o = 0.1 to 4W; R_L = 3.2Ω		0.03	0.5	%
SVR	Supply Voltage Rejection	R_S = 10kΩ, f = 100Hz; C3 = 22µF C3 = 100µF	45	50 57		dB
CT	Crosstalk	f = 1KHz f = 10KHz	45	55 50		dB dB
R_I	Input Resistance			50		KΩ
G_V	Voltage Gain			30		dB
G_V	Voltage Gain Match				1	dB
E_{IN}	Input Noise Voltage	R_S = 50Ω (*) R_S = 10KΩ (*) R_S = 50Ω (**) R_S = 10KΩ (**)		1.5 2 2 2.7	 7	µV µV µV µV

BRIDGE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
P_o	Output Power	d = 10%; R_L = 4Ω d = 10%; R_L = 3.2Ω	20	24 28		W W
		d = 10%; V_S = 13.2V R_L = 4Ω R_L = 3.2Ω		 20 24		 W W
d	Distortion	P_o = 0.1 to 10W; R_L = 4Ω		0.04	1	%
V_{OS}	Output Offset Voltage				250	mV
SVR	Supply Voltage Rejection	R_S = 10KΩ, f = 100Hz; C3 = 22µF C3 = 100µF	45	50 57		dB dB
R_I	Input Resistance			50		KΩ
G_V	Voltage Gain			36		dB
E_{IN}	Input Noise Voltage	R_S = 50Ω (*) R_S = 10KΩ (*) R_S = 50Ω (**) R_S = 10KΩ (**)		2 2.5 2.7 3.2		µV µV µV µV

(*) Curve A
(**) 22Hz to 22KHz

Figure 1: STEREO Test and Appication Circuit

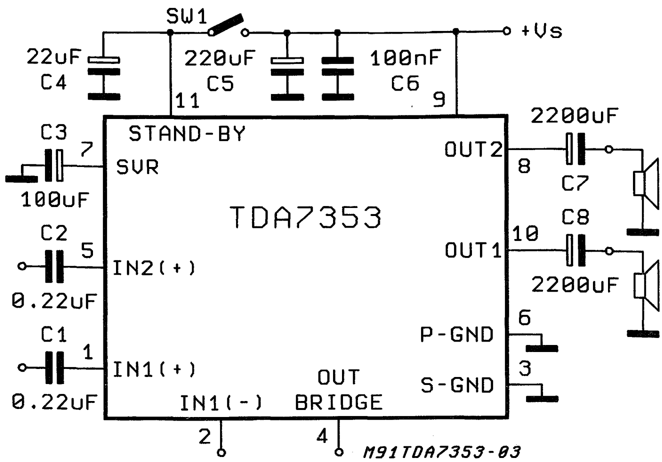


Figure 2: P.C. Board and Layout (STEREO) of the circuit of fig. 1 (1:1 scale)

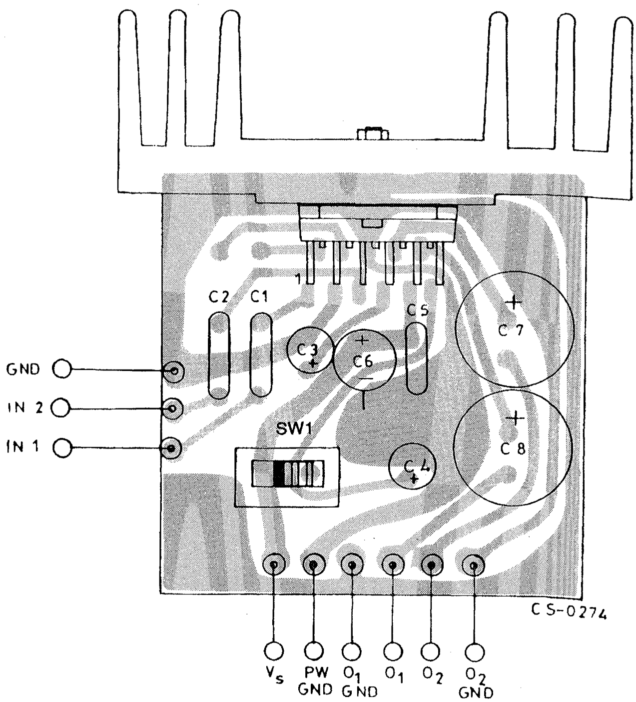


Figure 3: BRIDGE Test and Appication Circuit

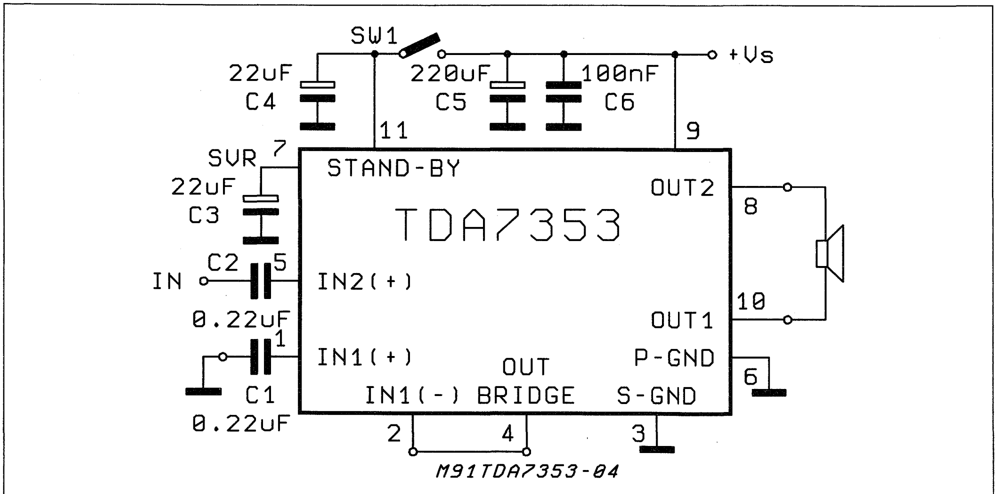
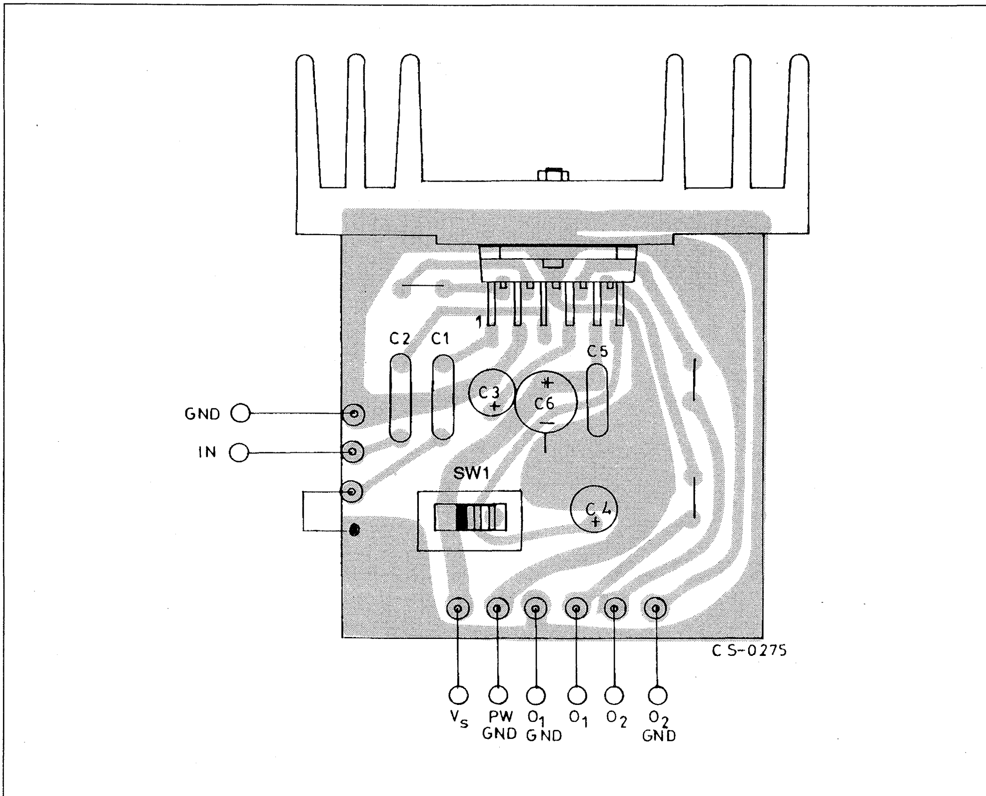


Figure 4: P.C. Board and Layout (BRIDGE) of the circuit of fig. 3 (1:1 scale)



RECOMMENDED VALUES OF THE EXTERNAL COMPONENTS (ref to the Stereo Test and Application Circuit)

Component	Recommended Value	Purpose	Larger than the Recomm. Value	Smaller than the Recomm. Value
C1	0.22µF	Input Decoupling (CH1)	—	—
C2	0.22µF	Input Decoupling (CH2)	—	—
C3	100µF	Supply Voltage Rejection Filtering Capacitor	Longer Turn-On Delay Time	Worse Supply Voltage Rejection. Shorter Turn-On Delay Time Danger of Noise (POP)
C4	22µF	Stand-By ON/OFF Delay	Delayed Turn-Off by Stand-By Switch	Danger of Noise (POP)
C5	220µF (min)	Supply By-Pass		Danger of Oscillations
C6	100nF (min)	Supply By-Pass		Danger of Oscillations
C7	2200µF	Output Decoupling CH2	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay
C8	2200µF	Output Decoupling CH1	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay

Figure 5: Output Power vs. Supply Voltage (Stereo)

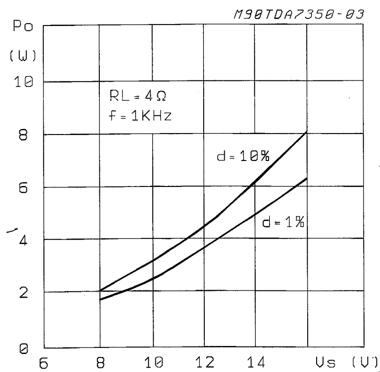


Figure 6: Output Power vs. Supply Voltage (Stereo)

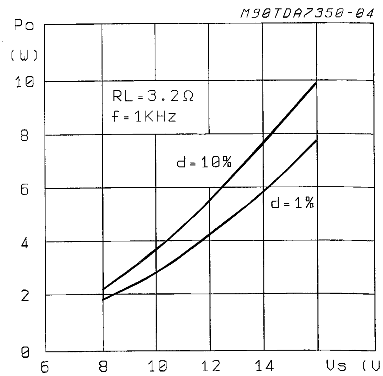


Figure 7: Output Power vs. Supply Voltage (Stereo)

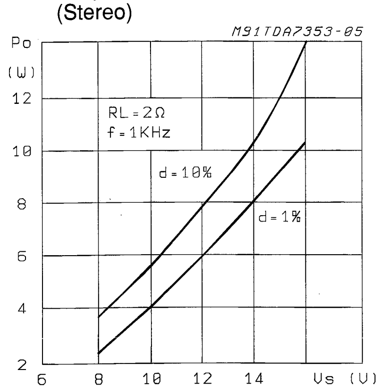


Figure 8: Output Power vs. Supply Voltage (Stereo)

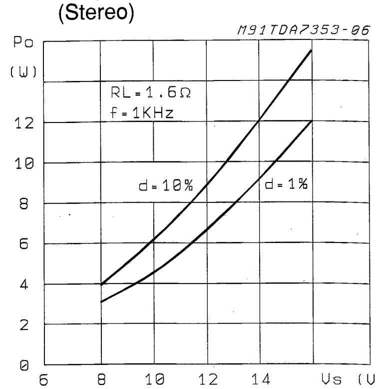


Figure 9: Output Power vs. Supply Voltage (Bridge)

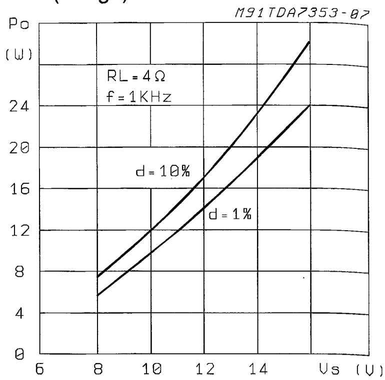


Figure 10: Output Power vs Supply Voltage (Bridge)

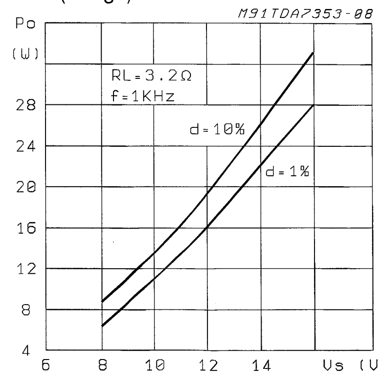


Figure 11: Quiescent Drain Current vs. Supply Voltage

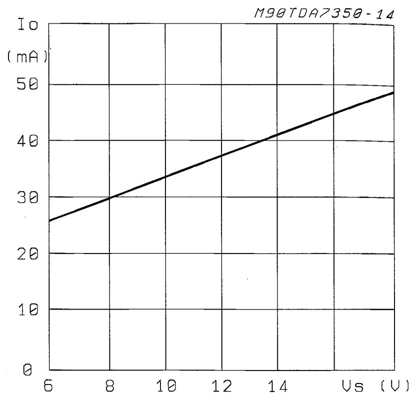


Figure 12: Distortion vs Output Power (Stereo)

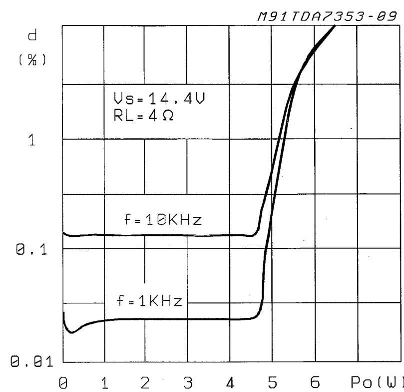


Figure 13: Distortion vs Output Power (Stereo)

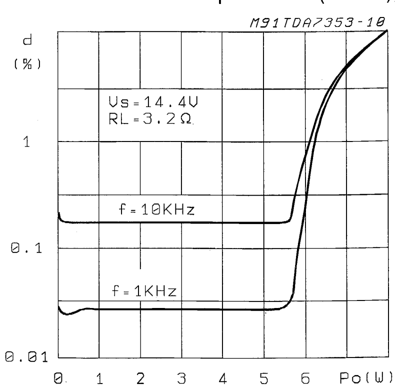


Figure 14: Distortion vs Output Power (Stereo)

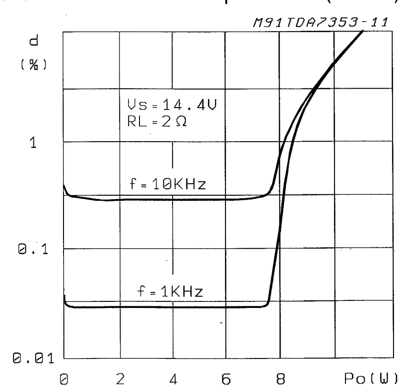


Figure 15: Distortion vs. Output Power (Stereo)

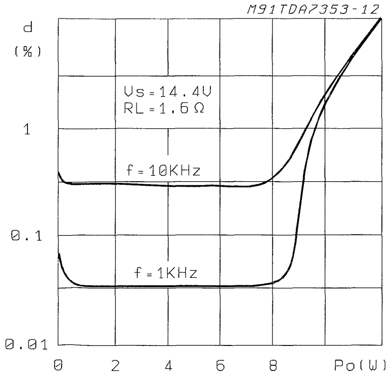


Figure 16: Distortion vs. Output Power (Bridge)

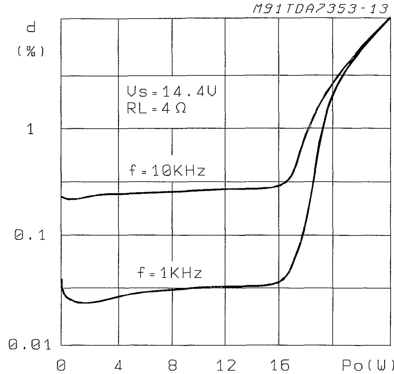


Figure 17: Distortion vs. Output Power (Bridge)

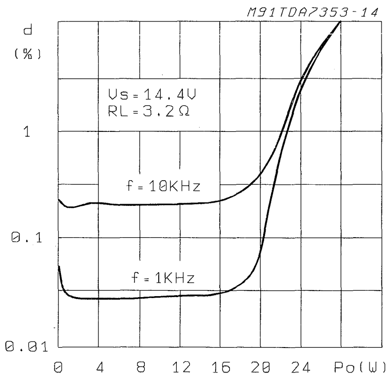


Figure 18: SVR vs. Frequency & C3; (Stereo)

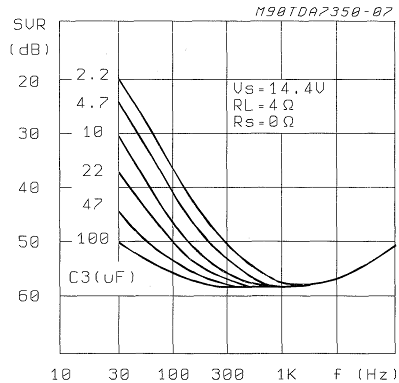


Figure 19: SVR vs. Frequency & C3; (Stereo)

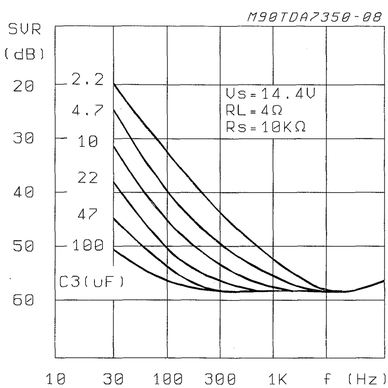


Figure 20: SVR vs. Frequency & C3; (Bridge)

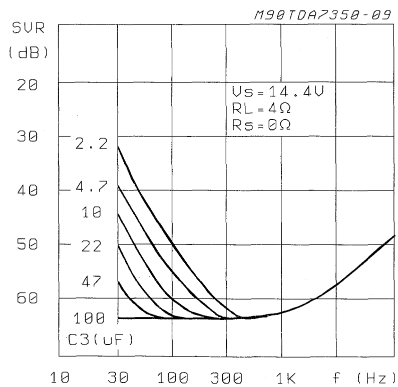


Figure 21: SVR vs. Frequency & C3; (Bridge)

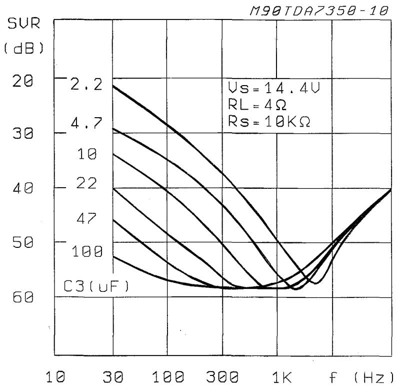


Figure 22: Power Dissipation & Efficiency vs. Output Power (Stereo)

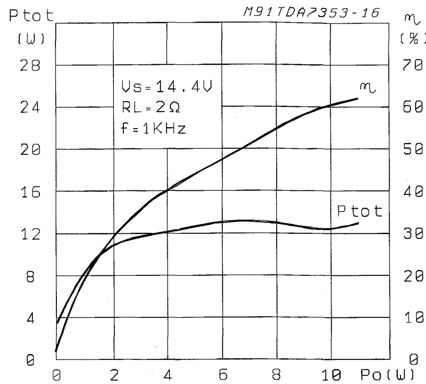


Figure 23: Power Dissipation & Efficiency vs. Output Power (Stereo)

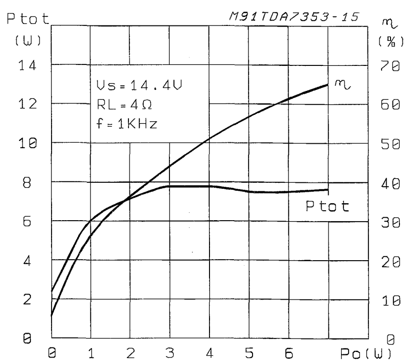


Figure 24: Power Dissipation & Efficiency vs. Output Power (Bridge)

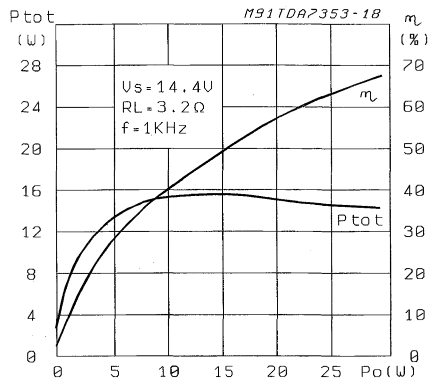
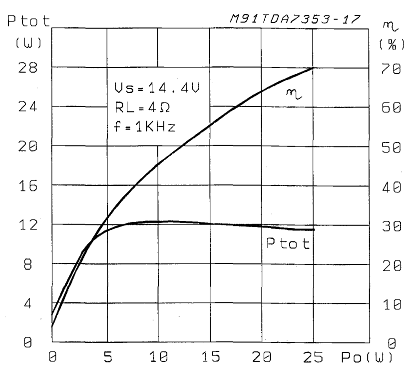


Figure 25: Power Dissipation & Efficiency vs. Output Power (Bridge)



AMPLIFIER ORGANIZATION

The TDA7353 has been developed taking care of the key concepts of the modern power audio amplifier for car radio such as: space and costs saving due to the minimized external count, excellent electrical performances, flexibility in use, superior reliability thanks to a built-in array of protections. As a result the following performances has been achieved:

- NO NEED OF BOOTSTRAP CAPACITORS EVEN AT THE HIGHEST OUTPUT POWER LEVELS

- ABSOLUTE STABILITY WITHOUT EXTERNAL COMPENSATION THANKS TO THE INNOVATIVE OUT STAGE CONFIGURATION, ALSO ALLOWING INTERNALLY FIXED CLOSED LOOP LOWER THAN COMPETITORS
- LOW GAIN (30dB STEREO FIXED WITHOUT ANY EXTERNAL COMPONENTS) IN ORDER TO MINIMIZE THE OUTPUT NOISE AND OPTIMIZE SVR
- SILENT MUTE/ST-BY FUNCTION FEATURING ABSENCE OF POP ON/OFF NOISE
- HIGH SVR
- STEREO/BRIDGE OPERATION WITHOUT ADDITION OF EXTERNAL COMPONENT
- AC/DC SHORT CIRCUIT PROTECTION (TO GND, TO V_S, ACROSS THE LOAD)
- LOUDSPEAKER PROTECTION
- DUMP PROTECTION
- ESD PROTECTION

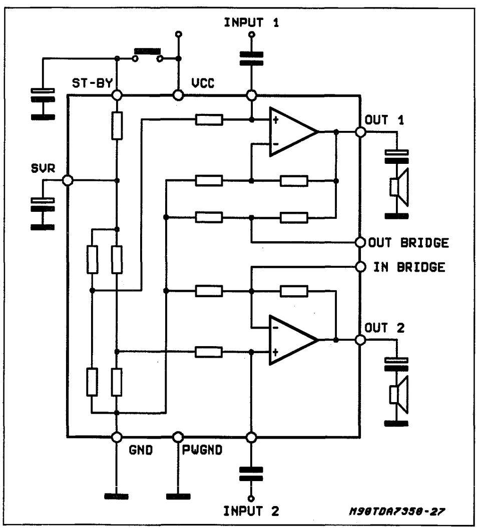
BLOCK DESCRIPTION

Polarization

The device is organized with the gain resistors directly connected to the signal ground pin i.e. without gain capacitors (fig. 26).

The non inverting inputs of the amplifiers are connected to the SVR pin by means of resistor dividers, equal to the feedback networks. This allows the outputs to track the SVR pin which is sufficiently slow to avoid audible turn-on and turn-off transients.

Figure 26: Block Diagram; Stereo Configuration



SVR

The voltage ripple on the outputs is equal to the one on SVR pin: with appropriate selection of C_{SVR}, more than 55dB of ripple rejection can be obtained.

Delayed Turn-on (muting)

The C_{SVR} sets a signal turn-on delay too. A circuit is included which mutes the device until the voltage on SVR pin reaches ~2V typ. (fig. 27). The mute function is obtained by duplicating the input differential pair (fig. 28): it can be switched to the signal source or to an internal mute input. This feature is necessary to prevent transients at the inputs reaching the loudspeaker(s) immediately after power-on).

Fig. 27 represents the detailed turn-on transient with reference to the stereo configuration.

At the power-on the output decoupling capacitors are charged through an internal path but the device itself remains switched off (phase 1 of the represented diagram).

When the outputs reach the voltage level of about 1V (this means that there is no presence of short circuits) the device switches on, the SVR capacitor starts charging itself and the output tracks exactly the SVR pin.

During this phase the device is muted until the SVR reaches the "Play" threshold (~2V typ.), after that the music signal starts being played.

Stereo/Bridge Switching

There is also no need for external components for changing from stereo to bridge configuration (figg. 26-29). A simple short circuit between two pins allows phase reversal at one output, yet maintaining the quiescent output voltage.

Stand-by

The device is also equipped with a stand-by function, so that a low current, and hence low cost switch, can be used for turn on/off.

Stability

The device is provided with an internal compensation wich allows to reach low values of closed loop gain.

In this way better performances on S/N ratio and SVR can be obtained.

Figure 27: Turn-on Delay Circuit

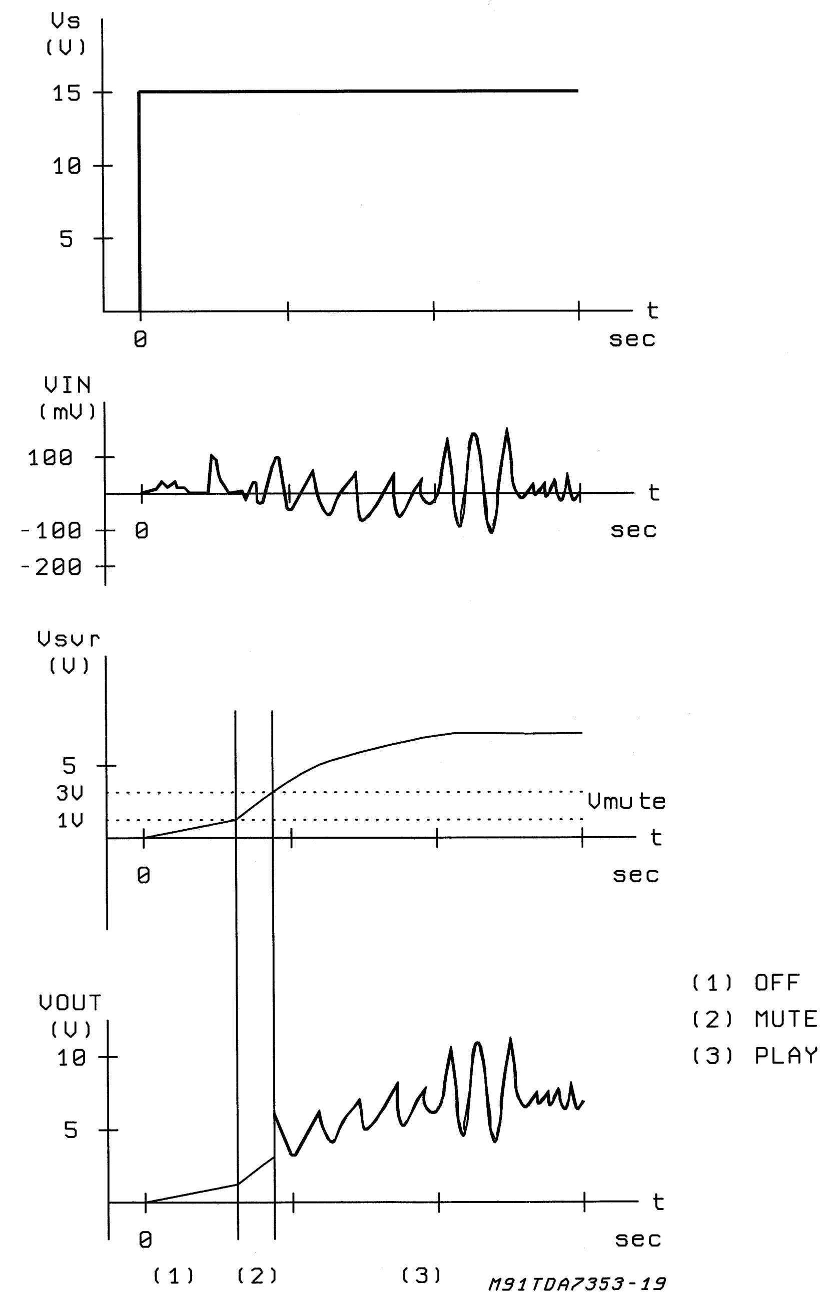


Figure 28: Mute Function Diagram

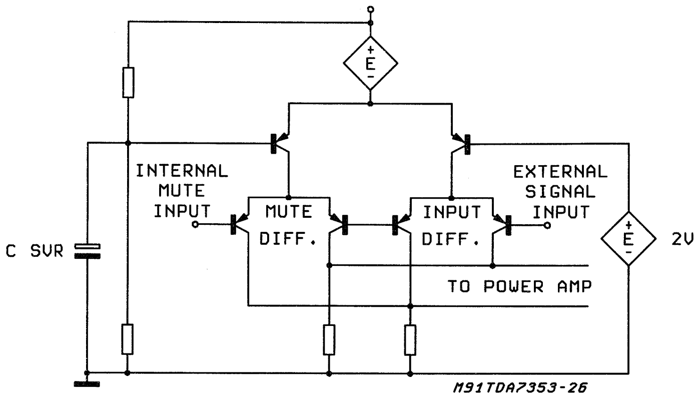


Figure 29: Block Diagram; Bridge Configuration

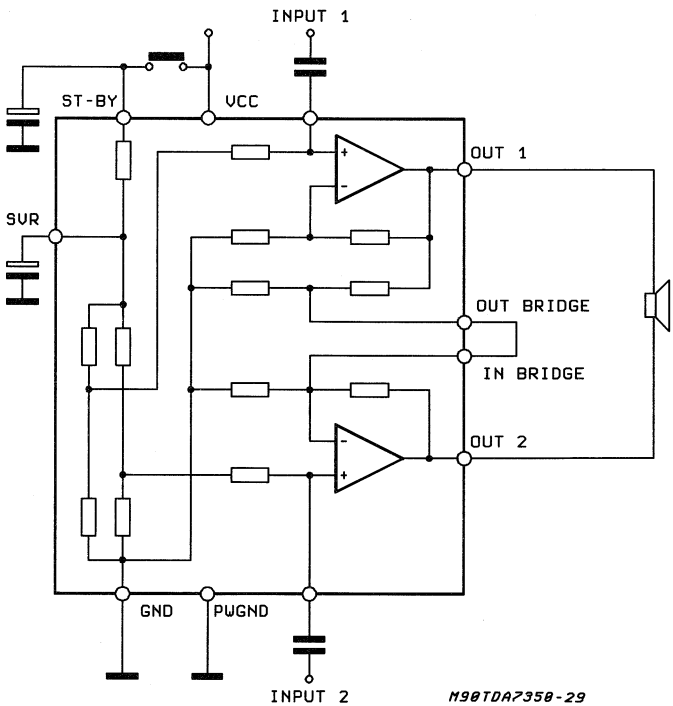


Figure 30: ICV - PNP Gain vs. Ic

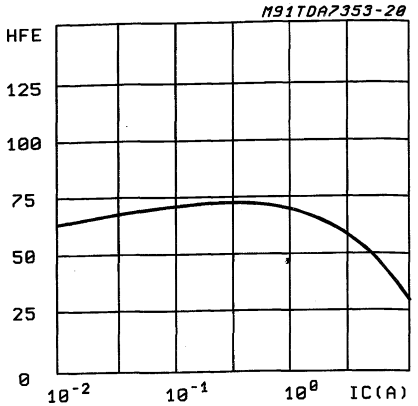


Figure 31: ICV - PNP $V_{CE(sat)}$ vs. Ic

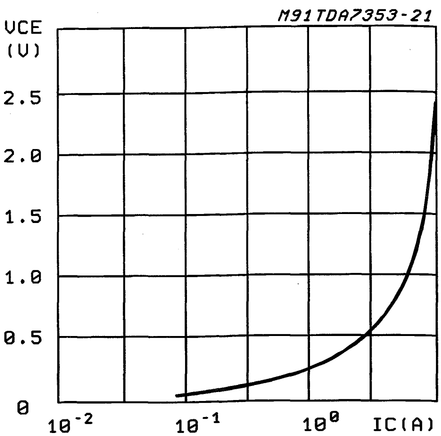
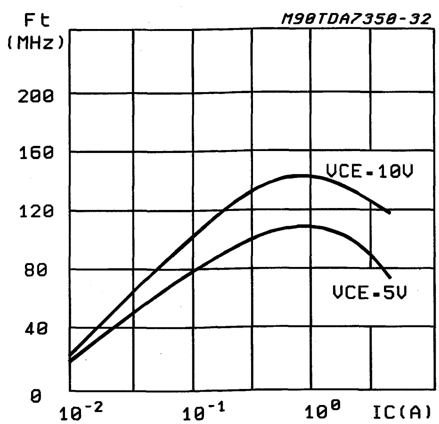


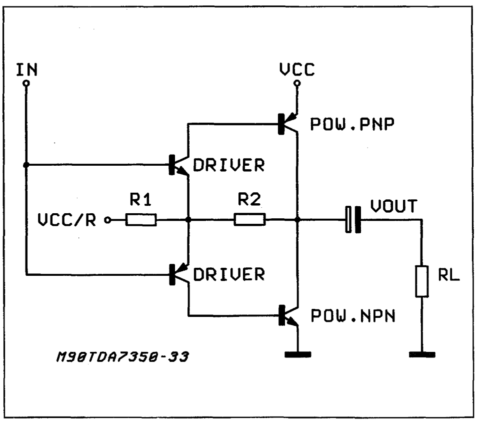
Figure 32: ICV - PNP cut-off frequency vs. Ic



OUTPUT STAGE

Poor current capability and low cutoff frequency are well known limits of the standard lateral PNP. Composite PNP-NPN power output stages have been widely used, regardless their high saturation drop. This drop can be overcome only at the expense of external components, namely, the bootstrap capacitors. The availability of a new 4A isolated collector PNP (ICV PNP) adds versatility to the design. The performance of this component, in terms of gain, V_{CEsat} and cut-off frequency, is shown in fig. 30, 31, 32 respectively. It is realized in a new bipolar technology, characterized by top-bottom isolation techniques, allowing the implementation of low leakage diodes, too. It guarantees BV_{CEO} > 20V and BV_{CBO} > 50V both for NPN and PNP transistors. Basically, the connection shown in fig. 33 has been chosen. First of all because its voltage swing is rail-to-rail, limited only by the VCEsat of the output transistors, which are in the range of 0.3Ω each. Then, the gain VOUT/VIN is greater than unity, approximately 1+R2/R1. (VCC/2 is fixed by an auxiliary amplifier common to both channel). It is possible, controlling the amount of this local feedback, to force the loop gain (A * β) to less than unity at frequencies for which the phase shift is 180°. This means that the output buffer is intrinsically stable and not prone to oscillation.

Figure 33: The New Output Stage



In contrast, with the circuit of fig. 34, the solution adopted to reduce the gain at high frequencies is the use of an external RC network.

AMPLIFIER BLOCK DIAGRAM

The block diagram of each voltage amplifier is shown in fig. 35. Regardless of production spread, the current in each final stage is kept low, with enough margin on the minimum, below which cross-over distortion would appear.

Figure 34: A Classical Output Stage

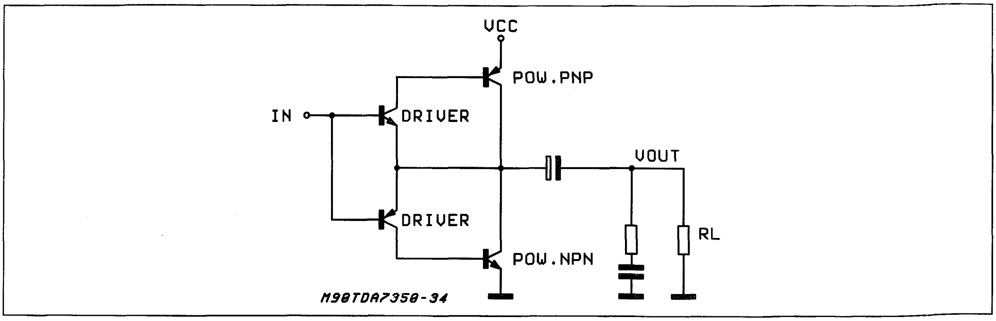
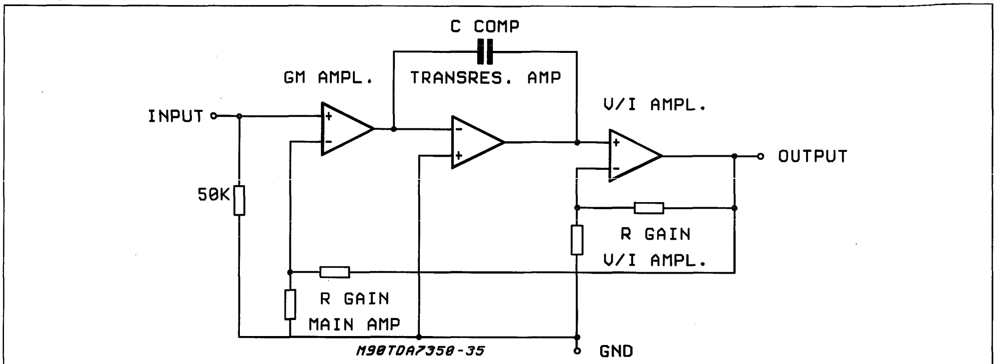


Figure 35: Amplifier Block Diagram



BUILT-IN PROTECTION SYSTEMS

Short Circuit Protection

The maximum current the device can deliver can be calculated by considering the voltage that may be present at the terminals of a car radio amplifier and the minimum load impedance.

Apart from consideration concerning the area of the power transistors it is not difficult to achieve peak currents of this magnitude (5A peak).
However, it becomes more complicated if AC and DC short circuit protection is also required.In particular,with a protection circuit which limits the output current following the SOA curve of the output transistors it is possible that in some conditions (highly reactive loads, for example) the protection circuit may intervene during normal operation. For this reason each amplifier has been equipped with a protection circuit that intervenes when the output current exceeds 4.5A.

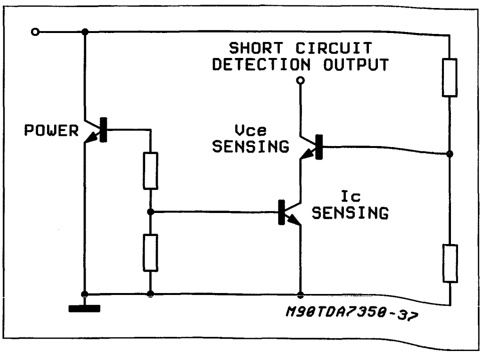
Fig 36 shows the protection circuit for an NPN power transistor (a symmetrical circuit applies to PNP).The VBE of the power is monitored and gives out a signal,available through a cascode.

This cascode is used to avoid the intervention of the short circuit protection when the saturation is below a given limit.

The signal sets a flip-flop which forces the amplifier outputs into a high impedance state.

In case of DC short circuit when the short circuit is removed the flip-flop is reset and restarts the circuit (fig. 40). In case of AC short circuit or load shorted in Bridge configuration, the device is continuously switched in ON/OFF conditions and the current is limited.

Figure 36: Circuitry for Short Circuit Detection



Load Dump Voltage Surge

The TDA 7353 has a circuit which enables it to withstand a voltage pulse train on pin 9, of the type shown in fig. 38.

If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.

A suggested LC network is shown in fig. 37.

With this network, a train of pulses with amplitude up to 120V and width of 2ms can be applied at point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Figure 37.

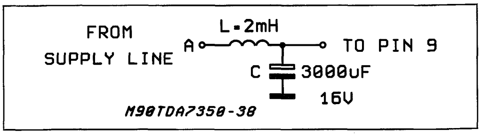
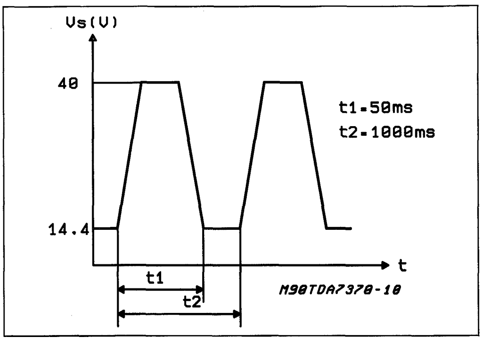


Figure 38.



Polarity Inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This features is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open Ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA7353 protection diodes are included to avoid any damage.

DC Voltage

The maximum operating DC voltage for the TDA7353 is 18V.

However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

Thermal Shut-down

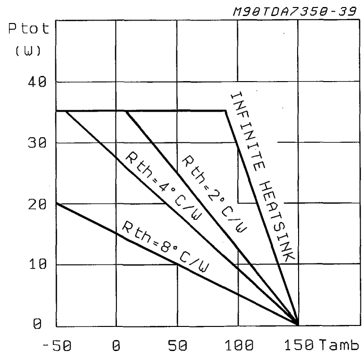
The presence of a thermal limiting circuit offers the following advantages:

1)an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2)the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 39 shows the dissipable power as a function of ambient temperature for different thermal resistance.

Figure 39: Maximum Allowable Power Dissipation vs. Ambient Temperature

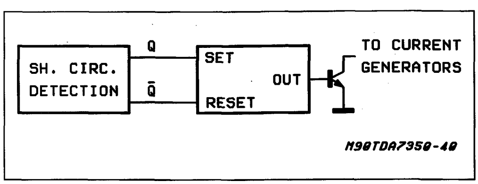


Loudspeaker Protection

The TDA7353 guarantees safe operations even for the loudspeaker in case of accidental shortcircuit.

Whenever a single OUT to GND, OUT to Vs short circuit occurs both the outputs are switched OFF so limiting dangerous DC current flowing through the loudspeaker.

Figure 40: Restart Circuit



APPLICATION HINTS

This section explains briefly how to get the best from the TDA7353 and presents some application circuits with suggestions for the value of the components.These values can change depending on the characteristics that the designer of the car radio wants to obtain,or other parts of the car radio that are connected to the audio block.

To optimize the performance of the audio part it is useful (or indispensable) to analyze also the parts outside this block that can have an interconnection with the amplifier.

This method can provide components and system cost saving.

Reducing Turn On-Off Pop

The TDA7353 has been designed in a way that the turn on(off) transients are controlled through the charge(discharge) of the Csvr capacitor.

As a result of it, the turn on(off) transient spectrum contents is limited only to the subsonic range.The following section gives some brief notes to get the best from this design feature(it will refer mainly to the stereo application which appears to be in most cases the more critical from the pop viewpoint.The bridge connection in fact,due to the common mode waveform at the outputs,does not give pop effect).

TURN-ON

Fig 41 shows the output waveform (before and after the "A" weighting filter) compared to the value of Csvr.

Better pop-on performance is obtained with higher Csvr values (the recommended range is from 22uF to 220uF).

The turn-on delay (during which the amplifier is in mute condition) is a function essentially of : C_{out}, C_{svr}.

Being:

$$T1 \approx 120 \cdot C_{out}$$
$$T2 \approx 1200 \cdot C_{svr}$$

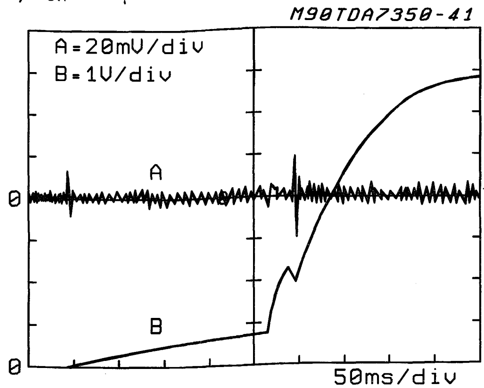
The turn-on delay is given by:

T1+T2 STEREO
T2 BRIDGE

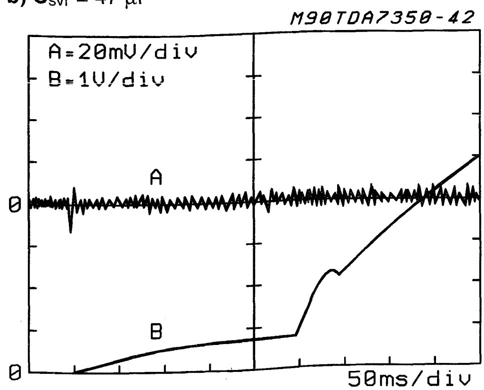
The best performance is obtained by driving the st-by pin with a ramp having a slope slower than 2V/ms

Figure 41:

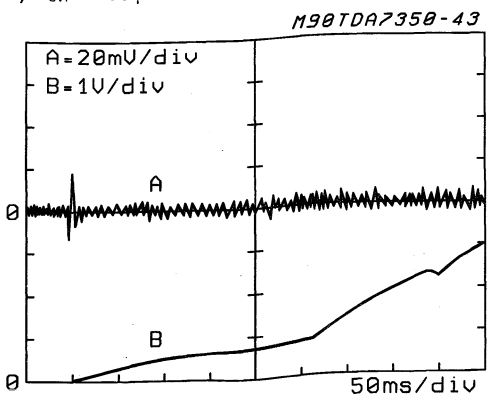
a) C_{svr} = 22 µF



b) C_{svr} = 47 µF



c) C_{svr} = 100 µF



TURN-OFF

A turn-off pop can occur if the st-by pin goes low with a short time constant (this can occur if other car radio sections, preamplifiers,radio.. are supplied through the same st-by switch).
This pop is due to the fast switch-off of the internal current generator of the amplifier.
If the voltage present across the load becomes rapidly zero (due to the fast switch off) a small pop occurs, depending also on Cout,Rload.

The parameters that set the switch off time constant of the st-by pin are:

- the st-by capacitor (Cst-by)
- the SVR capacitor (Csvr)
- resistors connected from st-by pin to ground (Rext)

The time constant is given by :

$T \approx Csvr \cdot 2000\Omega // Rext + Cst\text{-}by \cdot 2500\Omega // Rext$

The suggested time constants are :

T > 120ms with C_{out}=1000µF,R_L = 4ohm,stereo

T > 170ms with C_{out}=2200µF,R_L = 4ohm,stereo

If Rext is too low the Csvr can become too high and a different approach may be useful (see next section).

Figg 42, 43 show some types of electronic switches (µP compatible) suitable for supplying the st-by pin (it is important that Qsw is able to saturate with $V_{CE} \leq 150mV$).

Also for turn off pop the bridge configuration is superior, in particular the st-by pin can go low faster.

GLOBAL APPROACH TO SOLVING POP PROBLEM BY USING THE MUTING/TURN ON DELAY FUNCTION

In the real case turn-on and turn-off pop problems are generated not only by the power amplifier,but also (very often) by preamplifiers,tone controls,radios etc. and transmitted by the power amplifier to the loudspeaker.

A simple approach to solving these problems is to use the mute characteristics of the TDA7353.

If the SVR pin is at a voltage below 1V, the mute attenuation (typ) is 30dB .The amplifier is in play mode when Vsvr overcomes about 3V.

With the circuit of fig 44 we can mute the amplifier for a time Ton after switch-on and for a time Toff after switch-off.During this period the circuitry that precedes the power amplifier can produce spurious spikes that are not transmitted to the loudspeaker. This can give back a very simple design of this circuitry from the pop point of view.

A timing diagram of this circuit is illustrated in fig 45. Other advantages of this circuit are:

- A reduced time constant allowance of stand-by pin turn off.Consequently it is possible to drive all the car-radio with the signal that drives this pin.

-A better turn-off noise with signal on the output.

To drive two stereo amplifiers with this circuit it is possible to use the circuit of fig 46.

Figure 42

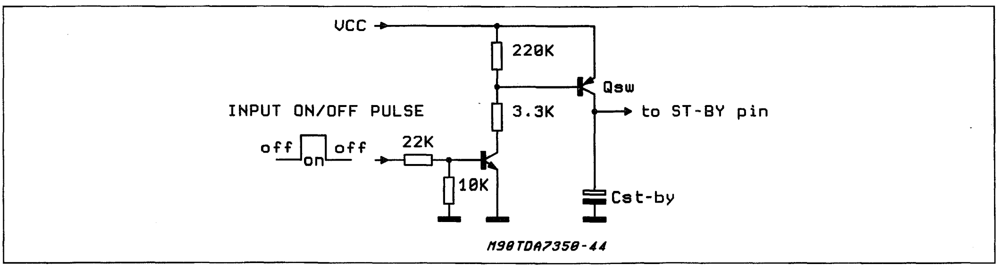


Figure 43

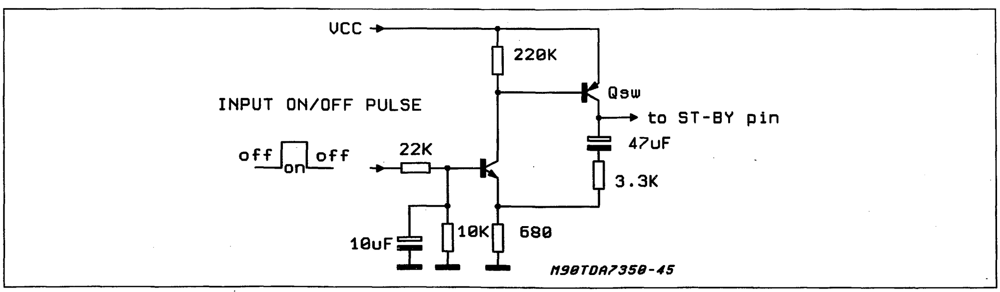


Figure 44

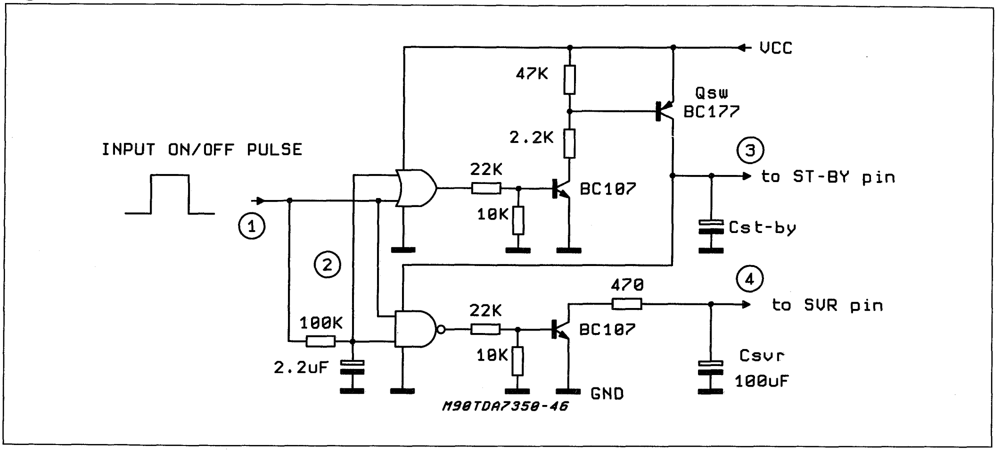


Figure 45

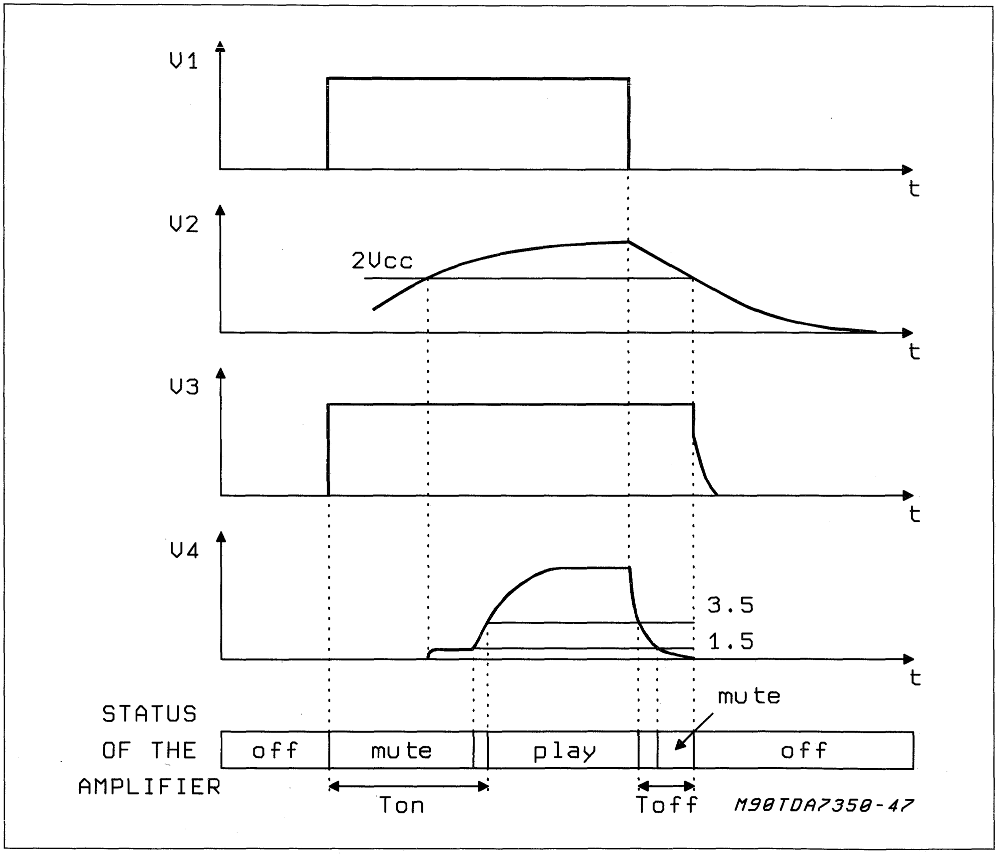
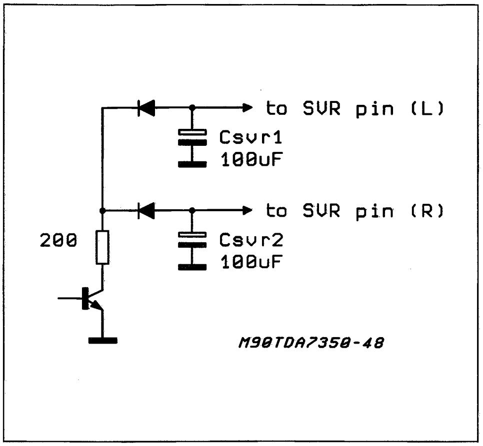


Figure 46



BALANCE INPUT IN BRIDGE CONFIGURATION

A helpful characteristic of the TDA7353 is that,in bridge configuration, a signal present on both the input capacitors is amplified by the same amount and it is present in phase at the outputs,so this signal does not produce effects on the load.The typical value of CMRR is 46 dB.

Looking at fig 47, we can see that a noise signal from the ground of the power amplifier to the ground of the hypothetical preamplifier is amplified of a factor equal to the gain of the amplifier (2 • Gv).

Using a configuration of fig. 48 the same ground noise is present at the output multiplied by the factor 2 • Gv/200.

This means less distortion,less noise (e.g. motor cassette noise) and/or a simplification of the layout of PC board.

The only limitation of this balanced input is the maximum amplitude of common mode signals (few tens of millivolt) to avoid a loss of output power due to the common mode signal on the output, but in a large number of cases this signal is within this range.

HIGH GAIN ,LOW NOISE APPLICATION

The following section describes a flexible preamplifier having the purpose to increase the gain of the TDA7353.

Figure 47

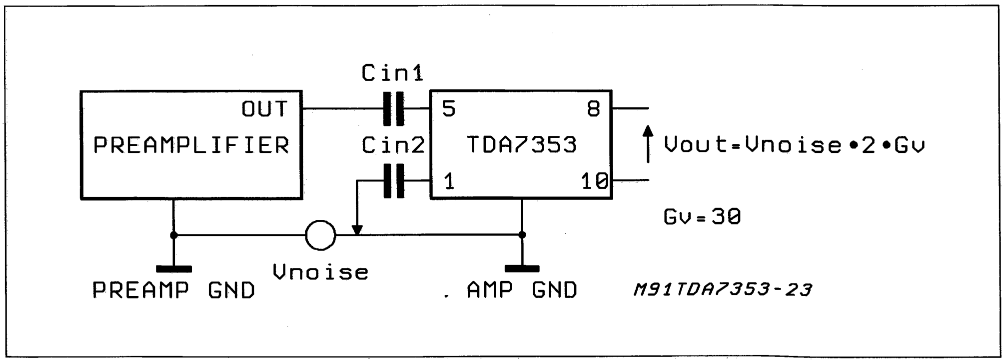
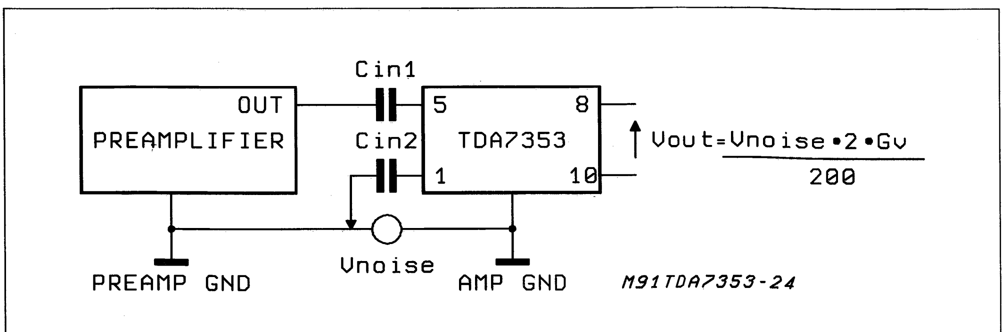


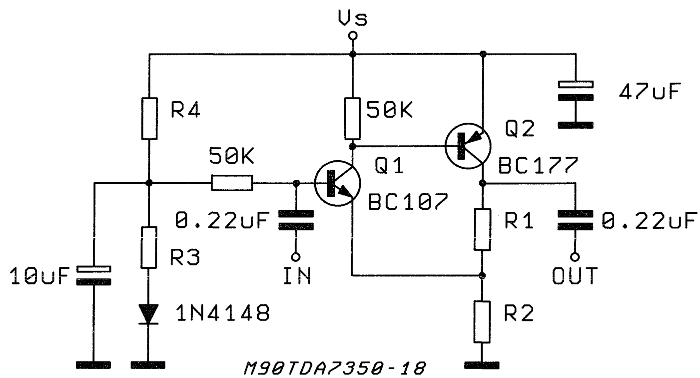
Figure 48



A two transistor network (fig. 49) has been adopted whose components can be changed in order to achieve the desired gain without affecting the good performances of the audio amplifier itself. The recommended values for 40 dB overall gain are :

Resistance	Stereo	Bridge
R1	10KΩ	10KW
R2	4.3KΩ	16KΩ
R3	10KΩ	24KΩ
R4	50KΩ	50KΩ

Figure 49



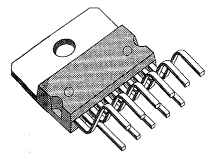
TDA7360

22W BRIDGE / STEREO AUDIO AMPLIFIER WITH CLIPPING DETECTOR

PRELIMINARY DATA

- VERY FEW EXTERNAL COMPONENTS
- NO BOUCHEROT CELLS
- NO BOOSTRAP CAPACITORS
- HIGH OUTPUT POWER
- NO SWITCH ON/OFF NOISE
- VERY LOW STAND-BY CURRENT
- FIXED GAIN (20dB STEREO)
- PROGRAMMABLE TURN-ON DELAY
- CLIPPING DETECTOR

Protections:
- OUTPUT AC-DC SHORT CIRCUIT TO GROUND AND TO SUPPLY VOLTAGE
- VERY INDUCTIVE LOADS
- LOUDSPEAKER PROTECTION
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GROUND
- ESD



Multiwatt - 11

ORDERING NUMBER: TDA7360

DESCRIPTION

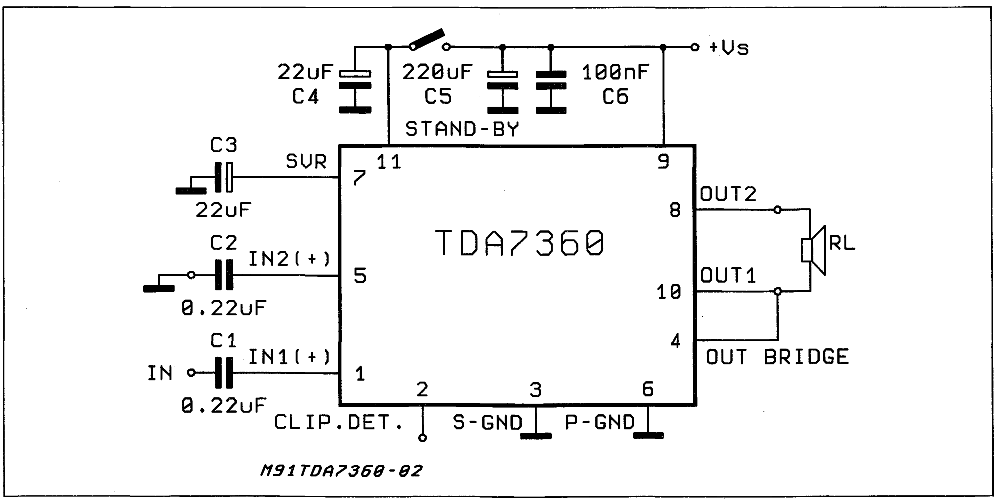
The TDA7360 is a new technology class AB Audio Power Amplifier in the Multiwatt® package designed for car radio applications.

Thanks to the fully complementary PNP/NPN output configuration the high power performance of the TDA7360 is obtained without bootstrap capacitors.

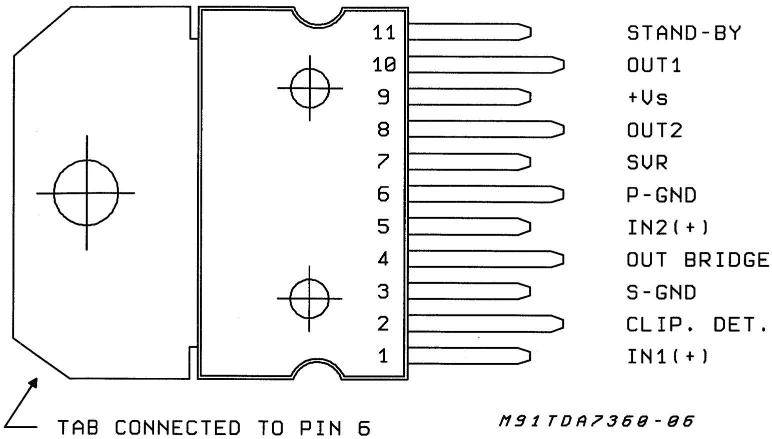
A delayed turn-on mute circuit eliminates audible on/off noise, and a novel short circuit protection system prevents spurious intervention with highly inductive loads.

The device provides a circuit for the detection of clipping in the output stages. The output, an open collector, is able to drive systems with automatic volume control.

APPLICATION CIRCUIT (BRIDGE)



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Operating Supply Voltage	18	V
V_S	DC Supply Voltage	28	V
V_S	Peak Supply Voltage (for t = 50ms)	50	V
I_o	Output Peak Current (non rep. for t = 100µs)	5	A
I_o	Output Peak Current (rep. freq. > 10Hz)	4	A
P_{tot}	Power Dissipation at T_{case} = 85°C	36	W
T_{stg}, T_J	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, T_{amb} = 25°C, V_S = 14.4V, f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range		8		18	V
I_d	Total Quiescent Drain Current	stereo configuration			120	mA
A_{SB}	Stand-by attenuation		60	80		dB
I_{SB}	Stand-by Current				100	μA
I_{CO}	Clip Detector Average Current	Pin 2 pull up to 5V with 10KΩ d = 1% d = 5%		70 130		μA μA

STEREO

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
P_O	Output Power (each channel)	d = 10% R_L = 1.6Ω R_L = 2Ω R_L = 3.2Ω R_L = 4Ω	 7 	 12 11 8 6.5		 W W W W
d	Distortion	P_O = 0.1 to 4W R_L = 3.2Ω		0.05	0.5	%
SVR	Supply Voltage Rejection	R_S = 10KΩ, f = 100Hz; C3 = 22μF C3 = 100μF	45 	 62		dB dB
CT	Crosstalk	f = 1KHz f = 10KHz	45 	 55		dB dB
R_I	Input Resistance			50		KΩ
G_V	Voltage Gain			20		dB
G_V	Voltage Gain Match				1	dB
E_{IN}	Input Noise Voltage	22 Hz to 22KHz RS = 50Ω R_S = 10KΩ		2.5 3	 7	μV μV

BRIDGE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OS}	Output Offset Voltage				250	mV
P_o	Output Power	d = 10%; R_L = 4Ω d = 10%; R_L = 3.2Ω	 16	20 22		W W
d	Distortion	P_o = 0.1 to 10W; R_L = 3.2Ω		0.05	1	%
SVR	Supply Voltage Rejection	R_S = 10KΩ, f = 100Hz; C3 = 22μF C3 = 100μF	45 	 62		dB dB
R_I	Input Resistance			50		KΩ
G_V	Voltage Gain			26		dB
E_{IN}	Input Noise Voltage	22Hz to 22KHz R_S = 50Ω R_S = 10KΩ		3.5 4		μV μV

Figure 1: STEREO Test and Appication Circuit

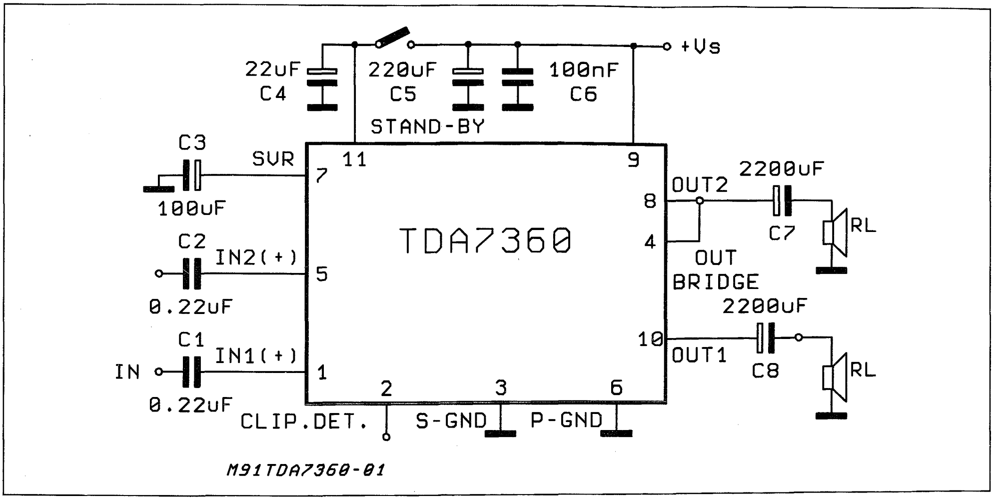


Figure 2: P.C. Board and Component Layout (STEREO) of the circuit of fig. 1 (1:1 scale)

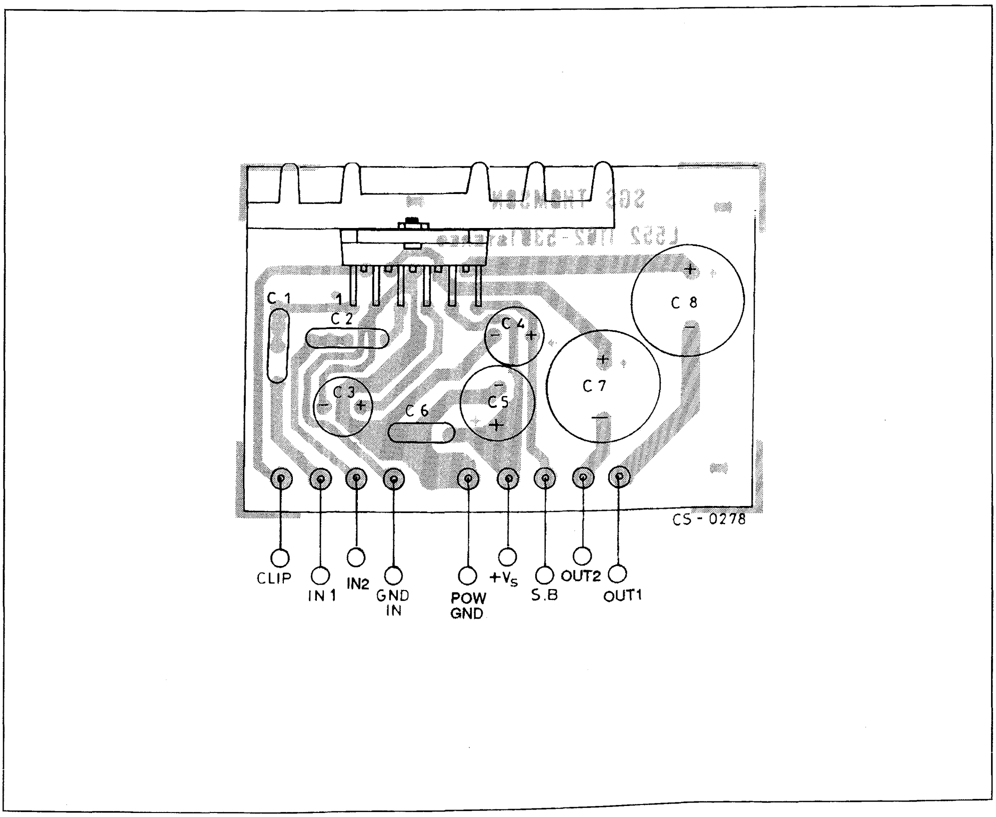


Figure 3: BRIDGE Test and Appication Circuit

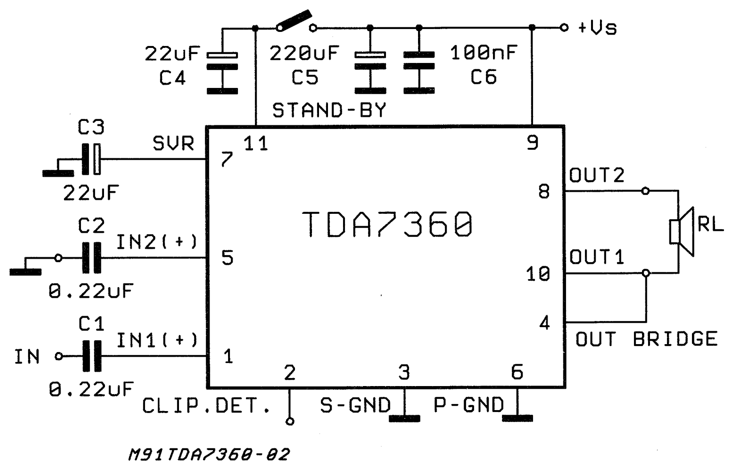
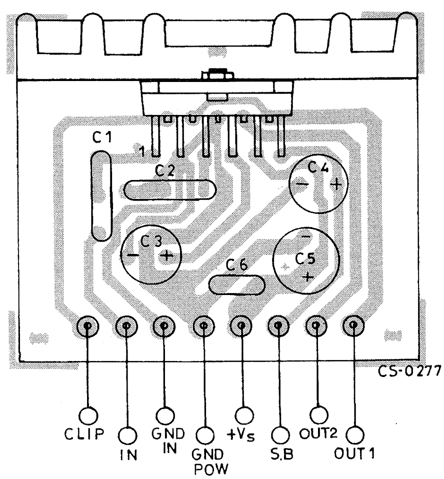


Figure 4: P.C. Board and Layout (BRIDGE) of the circuit of fig. 3 (1:1 scale)



RECOMMENDED VALUES OF THE EXTERNAL COMPONENTS (ref to the Stereo Test and Application Circuit)

Component	Recommended Value	Purpose	Larger than the Recomm. Value	Smaller than the Recomm. Value
C1	0.22µF	Input Decoupling (CH1)	—	—
C2	0.22µF	Input Decoupling (CH2)	—	—
C3	100µF	Supply Voltage Rejection Filtering Capacitor	Longer Turn-On Delay Time	- Worse Supply Voltage Rejection. - Shorter Turn-On Delay Time - Danger of Noise (POP)
C4	22µF	Stand-By ON/OFF Delay	Delayed Turn-Off by Stand-By Switch	Danger of Noise (POP)
C5	220µF (min)	Supply By-Pass		Danger of Oscillations
C6	100nF (min)	Supply By-Pass		Danger of Oscillations
C7	2200µF	Output Decoupling CH2	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay
C8	2200µF	Output Decoupling CH1	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay

Figure 5: Output Power vs. Supply Voltage (Stereo)

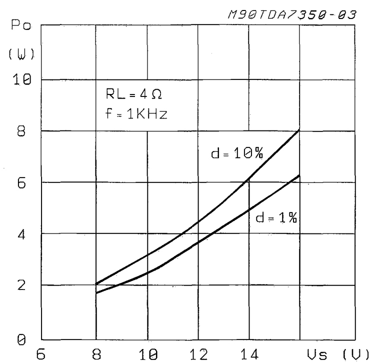


Figure 6: Output Power vs. Supply Voltage (Stereo)

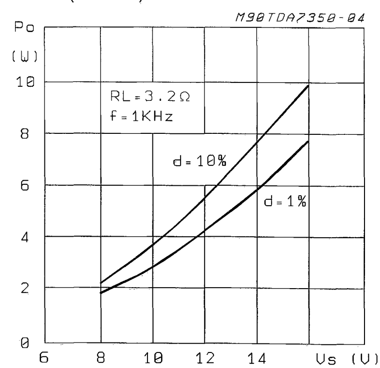


Figure 7: Output Power vs. Supply Voltage (Stereo)

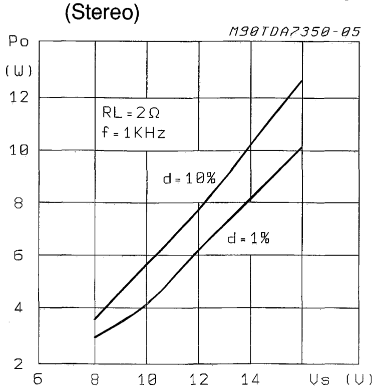


Figure 8: Output Power vs. Supply Voltage (Bridge)

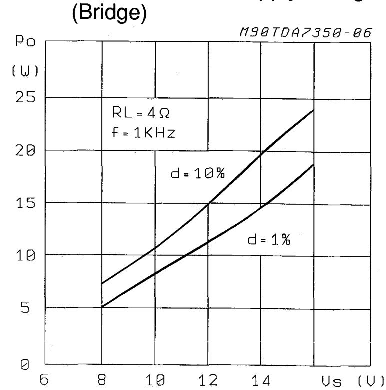


Figure 9: Output Power vs. Supply Voltage (Bridge)

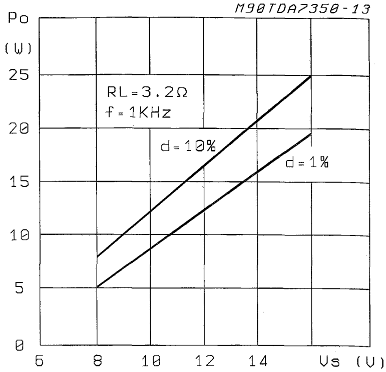


Figure 10: Drain Current vs Supply Voltage (Stereo)

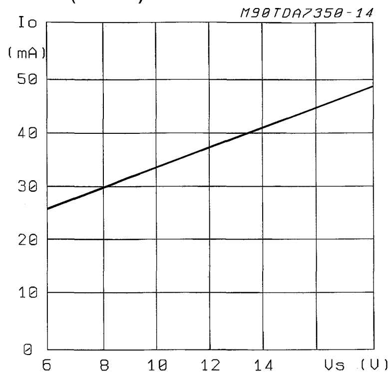


Figure 11: Distortion vs Output Power (Stereo)

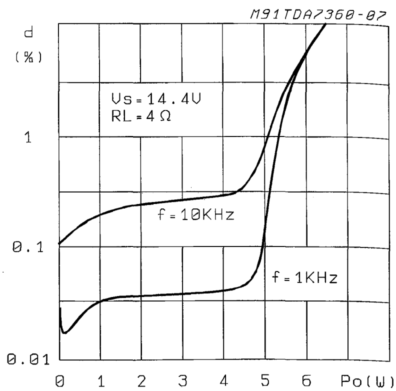


Figure 12: Distortion vs Output Power (Stereo)

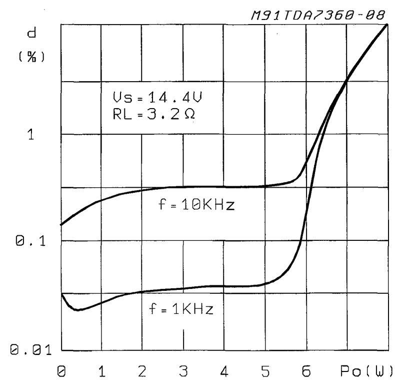


Figure 13: Distortion vs Output Power (Stereo)

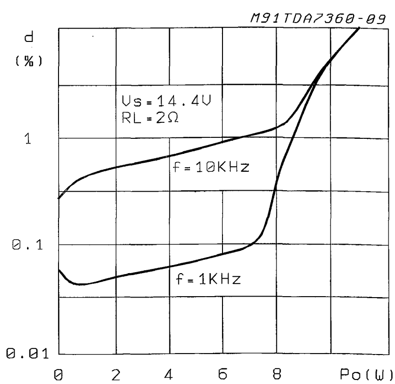


Figure 14: Distortion vs Output Power (Bridge)

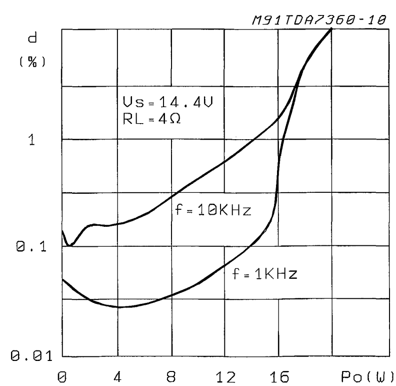


Figure 15: Distortion vs. Output Power

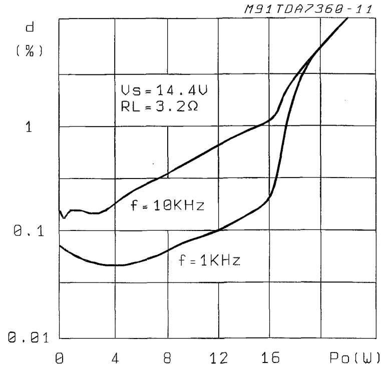


Figure 16: SVR vs. Frequency & C3 (Stereo)

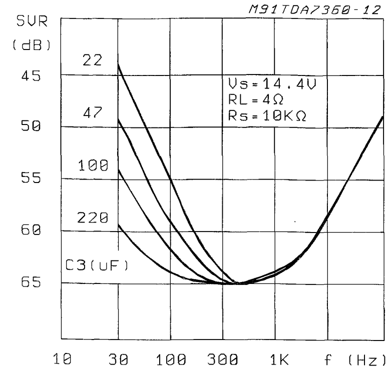


Figure 17: SVR vs. Frequency & C3 (Bridge)

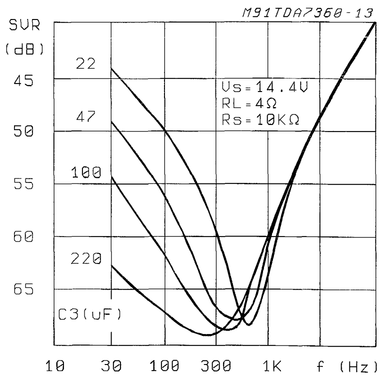


Figure 18: Crosstalk vs. Frequency (Stereo)

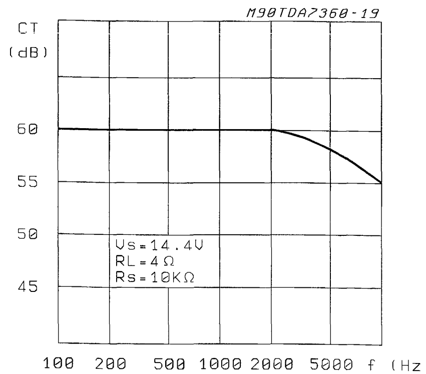


Figure 19: Power Dissipation & Efficiency vs. Output Power (Stereo)

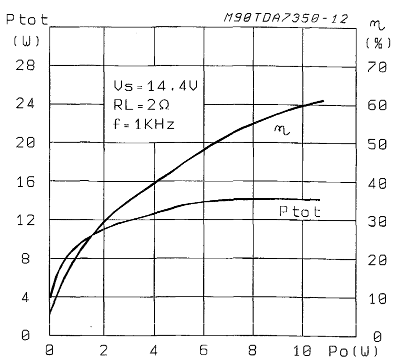


Figure 20: Power Dissipation & Efficiency vs. Output Power (Stereo)

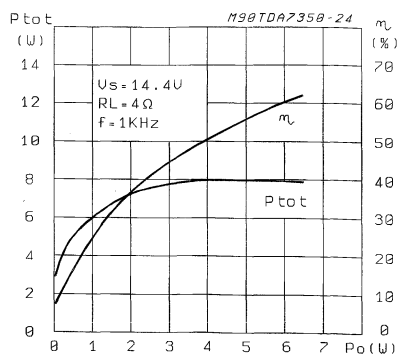


Figure 21: Power Dissipation & Efficiency vs. Output Power (Bridge)

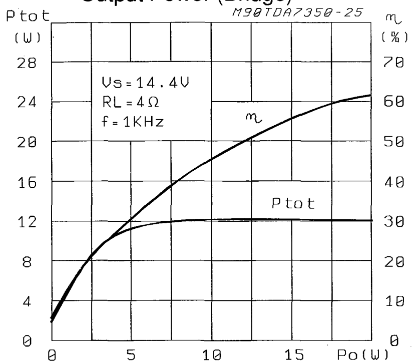
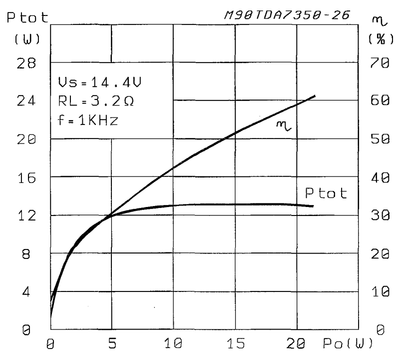


Figure 22: Power Dissipation & Efficiency vs. Output Power (Bridge)



AMPLIFIER ORGANIZATION

The TDA7360 has been developed taking care of the key concepts of the modern power audio amplifier for car radio such as: space and costs saving due to the minimized external count, excellent electrical performances, flexibility in use, superior reliability thanks to a built-in array of protections. As a result the following performances has been achieved:

- NO NEED OF BOOTSTRAP CAPACITORS EVEN AT THE HIGHEST OUTPUT POWER LEVELS
- ABSOLUTE STABILITY WITHOUT EXTERNAL COMPENSATION THANKS TO THE INNOVATIVE OUT STAGE CONFIGURATION, ALSO ALLOWING INTERNALLY FIXED CLOSED LOOP LOWER THAN COMPETITORS
- LOW GAIN (20dB STEREO FIXED WITHOUT ANY EXTERNAL COMPONENTS) IN ORDER TO MINIMIZE THE OUTPUT NOISE AND OPTIMIZE SVR
- SILENT MUTE/ST-BY FUNCTION FEATURING ABSENCE OF POP ON/OFF NOISE
- HIGH SVR
- STEREO/BRIDGE OPERATION WITHOUT ADDITION OF EXTERNAL COMPONENT
- AC/DC SHORT CIRCUIT PROTECTION (TO GND, TO V_S, ACROSS THE LOAD)
- LOUDSPEAKER PROTECTION
- DUMP PROTECTION
- ESD PROTECTION

BLOCK DESCRIPTION

Polarization

The device is organized with the gain resistors directly connected to the signal ground pin i.e. without gain capacitors (fig. 23).

The non inverting inputs of the amplifiers are connected to the SVR pin by means of resistor dividers, equal to the feedback networks. This allows the outputs to track the SVR pin which is sufficiently slow to avoid audible turn-on and turn-off transients.

SVR

The voltage ripple on the outputs is equal to the one on SVR pin: with appropriate selection of C_{SVR}, more than 60dB of ripple rejection can be obtained.

Delayed Turn-on (muting)

The C_{SVR} sets a signal turn-on delay too. A circuit is included which mutes the device until the voltage on SVR pin reaches ~2.5V typ. (fig. 25). The mute function is obtained by duplicating the input differential pair (fig. 24): it can be switched to the signal source or to an internal mute input. This feature is necessary to prevent transients at the inputs reaching the loudspeaker(s) immediately after power-on).

Fig. 25 represents the detailed turn-on transient with reference to the stereo configuration.

At the power-on the output decoupling capacitors are charged through an internal path but the device itself remains switched off (phase 1 of the represented diagram).

When the outputs reach the voltage level of about 1V (this means that there is no presence of short circuits) the device switches on, the SVR capacitor starts charging itself and the output tracks exactly the SVR pin.

During this phase the device is muted until the SVR reaches the "Play" threshold (~2.5V typ.), after that the music signal starts being played.

Stereo/Bridge Switching
There is also no need for external components for changing from stereo to bridge configuration (figg. 23-26). A simple short circuit between two pins allows phase reversal at one output, yet maintaining the quiescent output voltage.

Stand-by
The device is also equipped with a stand-by function, so that a low current, and hence low cost switch, can be used for turn on/off.

Stability
The device is provided with an internal compensation wich allows to reach low values of closed loop gain.
In this way better performances on S/N ratio and SVR can be obtained.

Figure 23: Block Diagram; Stereo Configuration

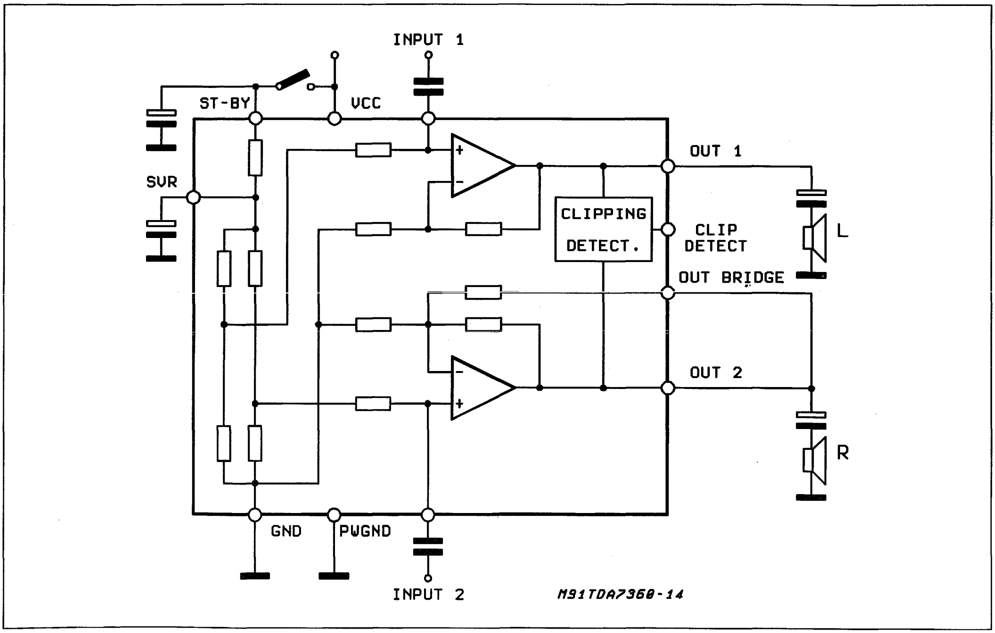


Figure 24: Mute Function Diagram

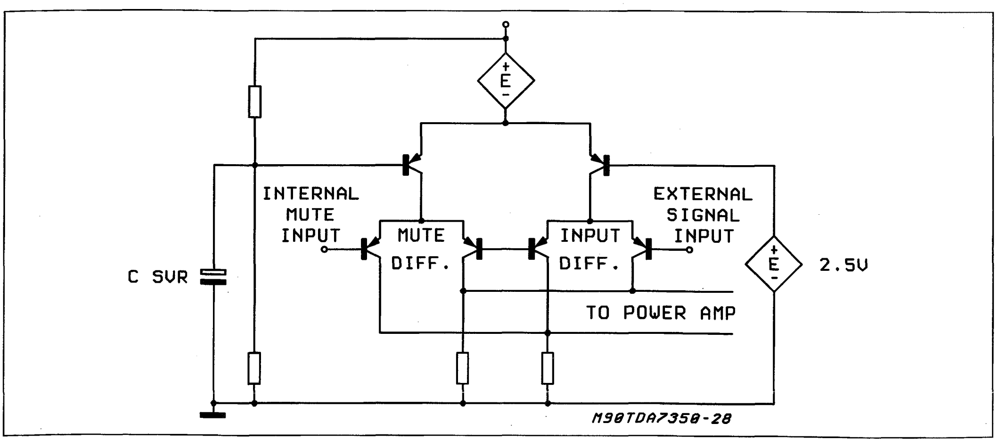


Figure 25: Turn-on Delay Circuit

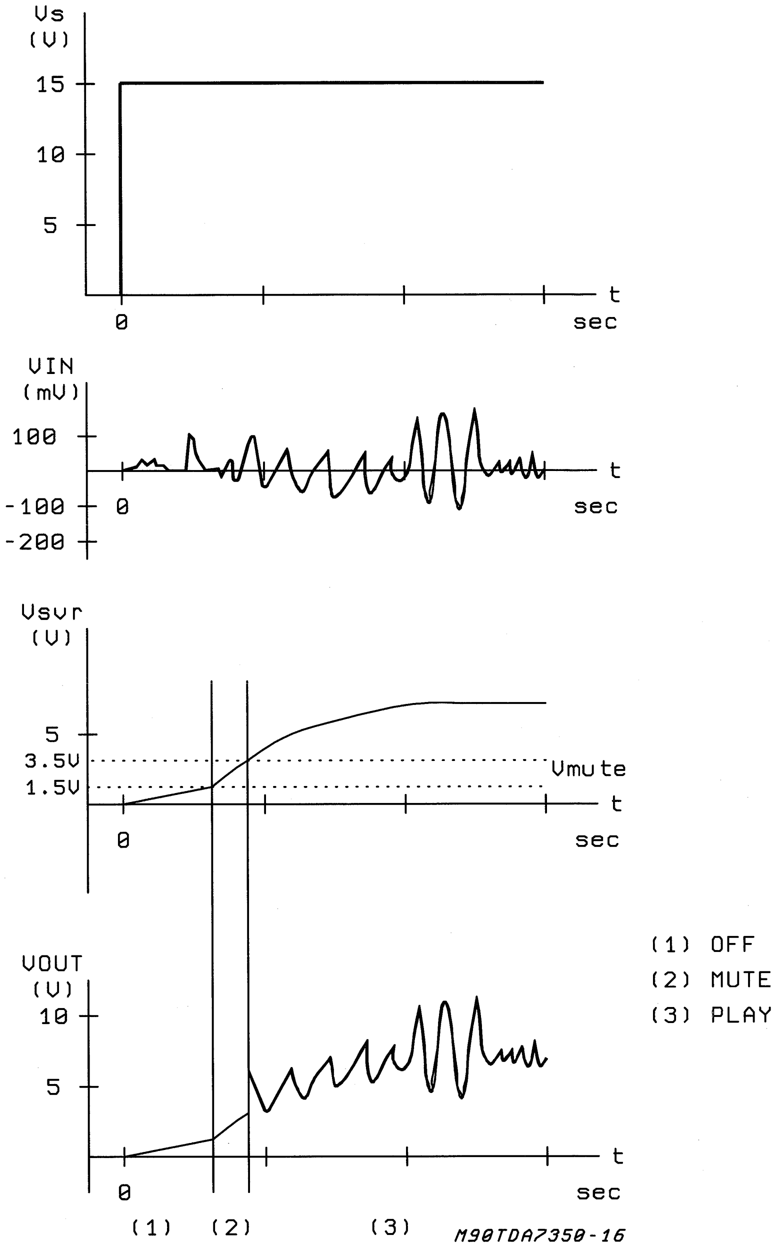
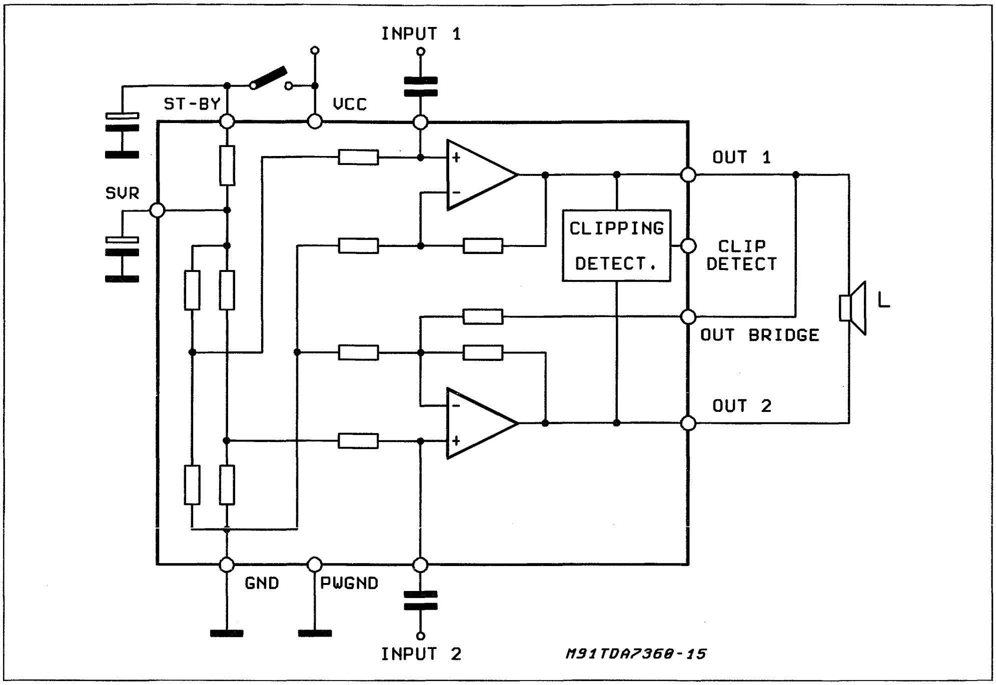


Figure 26: Block Diagram; Bridge Configuration



CLIP DETECTOR

The TDA7360 is equipped with an internal circuit able to detect the output stage saturation providing a proper current sinking into an open collector out. (pin2) when a certain distortion level is reached at each output. This particular function allows compression facility whenever the amplifier is overdriven, so obtaining high quality sound at all listening levels.

Figure 27: Dual Channel Distortion Detector

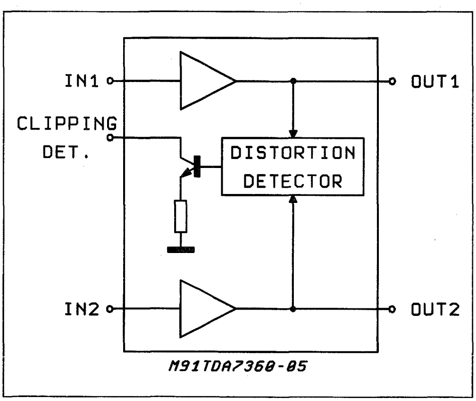


Figure 28: Output at Clipping Detector Pin vs. Signal Distortion

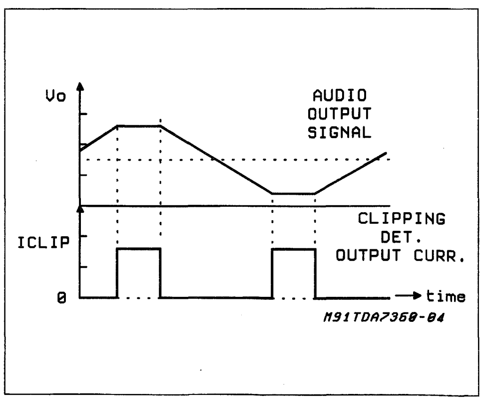


Figure 29: ICV - PNP Gain vs. I_C

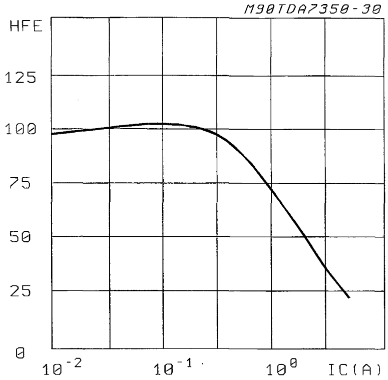


Figure 30: ICV - PNP $V_{CE(sat)}$ vs. I_C

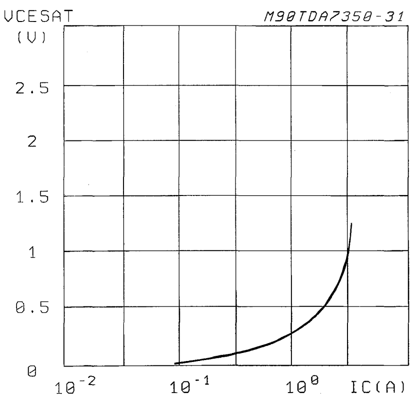
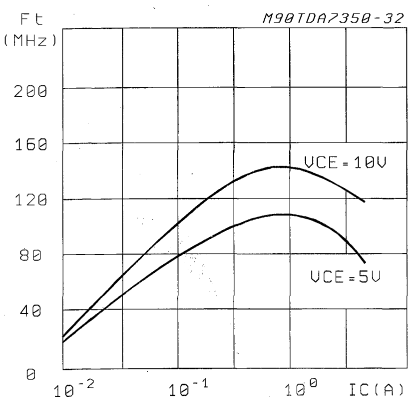


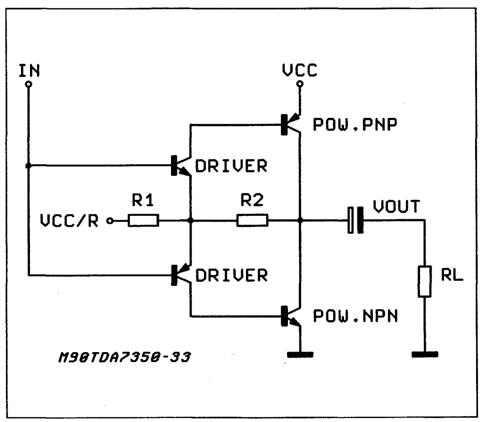
Figure 31: ICV - PNP cut-off frequency vs. I_C



OUTPUT STAGE

Poor current capability and low cutoff frequency are well known limits of the standard lateral PNP. Composite PNP-NPN power output stages have been widely used, regardless their high saturation drop. This drop can be overcome only at the expense of external components, namely, the bootstrap capacitors. The availability of 4A isolated collector PNP (ICV PNP) adds versatility to the design. The performance of this component, in terms of gain, V_{CEsat} and cut-off frequency, is shown in fig. 29, 30, 31 respectively. It is realized in a new bipolar technology, characterized by top-bottom isolation techniques, allowing the implementation of low leakage diodes, too. It guarantees BV_{CEO} > 20V and BV_{CBO} > 50V both for NPN and PNP transistors. Basically, the connection shown in fig. 32 has been chosen. First of all because its voltage swing is rail-to-rail, limited only by the VCEsat of the output transistors, which are in the range of 0.3Ω each. Then, the gain VOUT/VIN is greater than unity, approximately 1+R2/R1. (VCC/2 is fixed by an auxiliary amplifier common to both channel). It is possible, controlling the amount of this local feedback, to force the loop gain (A * β) to less than unity at frequencies for which the phase shift is 180°. This means that the output buffer is intrinsically stable and not prone to oscillation.

Figure 32: The New Output Stage



In contrast, with the circuit of fig. 33, the solution adopted to reduce the gain at high frequencies is the use of an external RC network.

AMPLIFIER BLOCK DIAGRAM

The block diagram of each voltage amplifier is shown in fig. 34. Regardless of production spread, the current in each final stage is kept low, with enough margin on the minimum, below which cross-over distortion would appear.

Figure 33: A Classical Output Stage

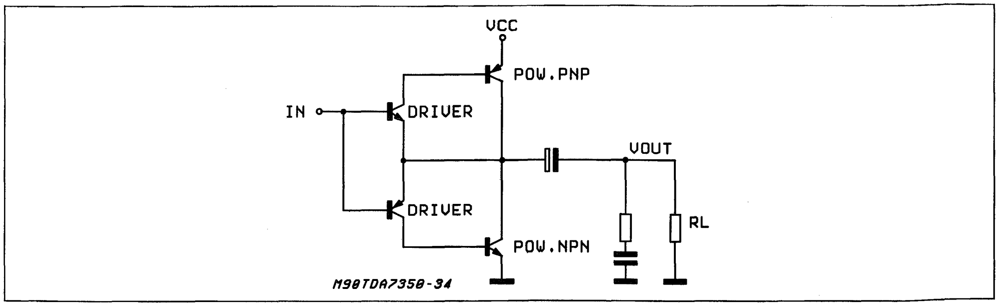
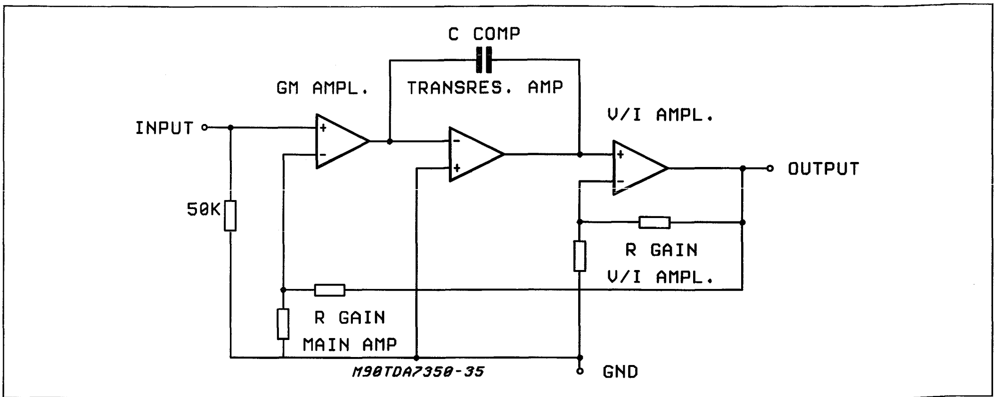


Figure 34: Amplifier Block Diagram



BUILT-IN PROTECTION SYSTEMS

Short Circuit Protection

The maximum current the device can deliver can be calculated by considering the voltage that may be present at the terminals of a car radio amplifier and the minimum load impedance.

Apart from consideration concerning the area of the power transistors it is not difficult to achieve peak currents of this magnitude (5 A peak).
However, it becomes more complicated if AC and DC short circuit protection is also required.In particular, with a protection circuit which limits the output current following the SOA curve of the output transistors it is possible that in some conditions (highly reactive loads, for example) the protection circuit may intervene during normal operation. For this reason each amplifier has been equipped with a protection circuit that intervenes when the output current exceeds 4A

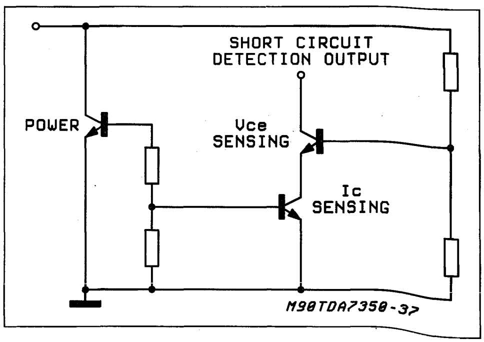
Fig 35 shows the protection circuit for an NPN power transistor (a symmetrical circuit applies to PNP).The VBE of the power is monitored and gives out a signal,available through a cascode.

This cascode is used to avoid the intervention of the short circuit protection when the saturation is below a given limit.

The signal sets a flip-flop which forces the amplifier outputs into a high impedance state.

In case of DC short circuit when the short circuit is removed the flip-flop is reset and restarts the circuit (fig. 39). In case of AC short circuit or load shorted in Bridge configuration, the device is continuously switched in ON/OFF conditions and the current is limited.

Figure 35: Circuitry for Short Circuit Detection



Load Dump Voltage Surge

The TDA 7360 has a circuit which enables it to withstand a voltage pulse train on pin 9, of the type shown in fig. 37.
If the supply voltage peaks to more than 50V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.

A suggested LC network is shown in fig. 36.
With this network, a train of pulses with amplitude up to 120V and width of 2ms can be applied at point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Figure 36

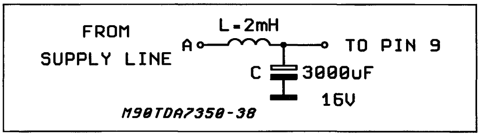
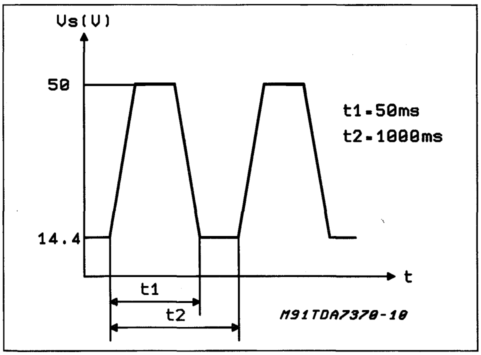


Figure 37



Polarity Inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This features is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open Ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA7360 protection diodes are included to avoid any damage.

DC Voltage

The maximum operating DC voltage for the TDA7360 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

Thermal Shut-down

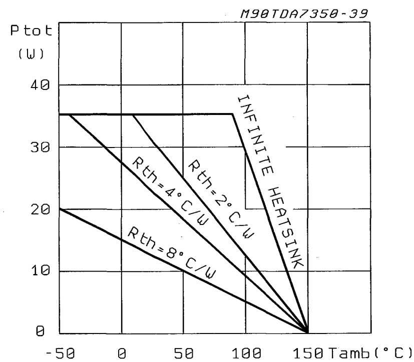
The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 38 shows the dissipable power as a function of ambient temperature for different thermal resistance.

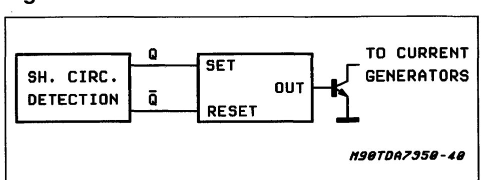
Figure 38: Maximum Allowable Power Dissipation vs. Ambient Temperature



Loudspeaker Protection

The TDA7360 guarantees safe operations even for the loudspeaker in case of accidental shortcircuit.
Whenever a single OUT to GND, OUT to V_S short circuit occurs both the outputs are switched OFF so limiting dangerous DC current flowing through the loudspeaker.

Figure 39: Restart Circuit



APPLICATION HINTS

This section explains briefly how to get the best from the TDA7360 and presents some application circuits with suggestions for the value of the components.These values can change depending on the characteristics that the designer of the car radio wants to obtain,or other parts of the car radio that are connected to the audio block.

To optimize the performance of the audio part it is useful (or indispensable) to analyze also the parts outside this block that can have an interconnection with the amplifier.

This method can provide components and system cost saving.

Reducing Turn On-Off Pop

The TDA7360 has been designed in a way that the turn on(off) transients are controlled through the charge(discharge) of the Csvr capacitor.

As a result of it, the turn on(off) transient spectrum contents is limited only to the subsonic range.The following section gives some brief notes to get the best from this design feature(it will refer mainly to the stereo application which appears to be in most cases the more critical from the pop viewpoint.The bridge connection in fact,due to the common mode waveform at the outputs,does not give pop effect).

TURN-ON

Fig 40 shows the output waveform (before and after the "A" weighting filter) compared to the value of Csvr.

Better pop-on performance is obtained with higher Csvr values (the recommended range is from 22uF to 220uF).

The turn-on delay (during which the amplifier is in mute condition) is a function essentially of : C_{out}, C_{svr}.

Being:

$$T1 \approx 120 \cdot C_{out}$$

$$T2 \approx 1200 \cdot C_{svr}$$

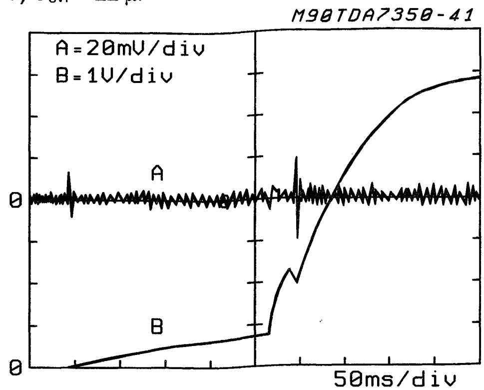
The turn-on delay is given by:

T1+T2	STEREO
T2	BRIDGE

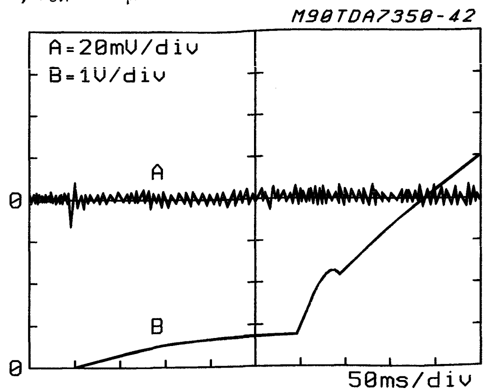
The best performance is obtained by driving the st-by pin with a ramp having a slope slower than 2V/ms

Figure 40:

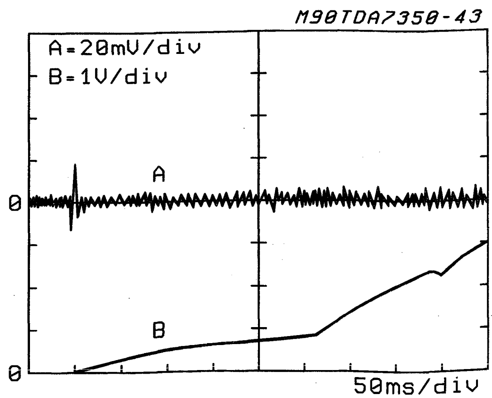
a) C_{svr} = 22 μF



b) C_{svr} = 47 μF



c) C_{svr} = 100 μF



TURN-OFF

A turn-off pop can occur if the st-by pin goes low with a short time constant (this can occur if other car radio sections, preamplifiers,radio.. are supplied through the same st-by switch).
This pop is due to the fast switch-off of the internal current generator of the amplifier.
If the voltage present across the load becomes rapidly zero (due to the fast switch off) a small pop occurs, depending also on Cout,Rload.

The parameters that set the switch off time constant of the st-by pin are:

- the st-by capacitor (Cst-by)
- the SVR capacitor (Csvr)
- resistors connected from st-by pin to ground (Rext)

The time constant is given by :

$T \approx Csvr \cdot 2000\Omega // Rext + Cst\text{-}by \cdot 2500\Omega // Rext$

The suggested time constants are :

$T > 120ms$ with $C_{out}=1000\mu F, R_L = 4ohm$,stereo

$T > 170ms$ with $C_{out}=2200\mu F, R_L = 4ohm$,stereo

If Rext is too low the Csvr can become too high and a different approach may be useful (see next section).

Figg 41, 42 show some types of electronic switches (µP compatible) suitable for supplying the st-by pin (it is important that Qsw is able to saturate with $V_{CE} \leq 150mV$).

Also for turn off pop the bridge configuration is superior, in particular the st-by pin can go low faster.

GLOBAL APPROACH TO SOLVING POP PROBLEM BY USING THE MUTING/TURN ON DELAY FUNCTION

In the real case turn-on and turn-off pop problems are generated not only by the power amplifier,but also (very often) by preamplifiers,tone controls,radios etc. and transmitted by the power amplifier to the loudspeaker.

A simple approach to solving these problems is to use the mute characteristics of the TDA7360.

If the SVR pin is at a voltage below 1.5 V, the mute attenuation (typ) is 30dB .The amplifier is in play mode when Vsvr overcomes 3.5 V.

With the circuit of fig 43 we can mute the amplifier for a time Ton after switch-on and for a time Toff after switch-off.During this period the circuitry that precedes the power amplifier can produce spurious spikes that are not transmitted to the loudspeaker. This can give back a very simple design of this circuitry from the pop point of view.

A timing diagram of this circuit is illustrated in fig 44. Other advantages of this circuit are:

- A reduced time constant allowance of stand-by pin turn off.Consequently it is possible to drive all the car-radio with the signal that drives this pin.

-A better turn-off noise with signal on the output.

To drive two stereo amplifiers with this circuit it is possible to use the circuit of fig 45.

Figure 41

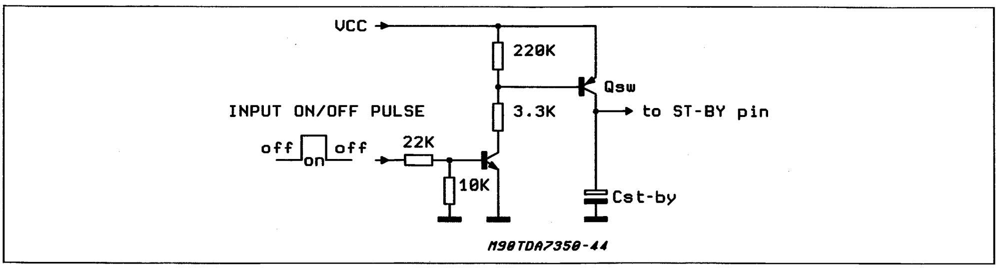


Figure 42

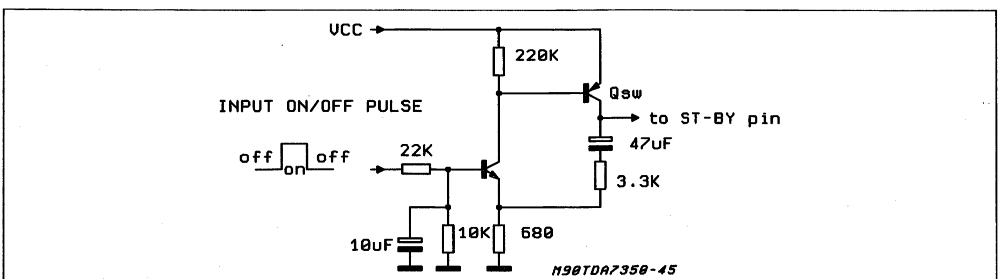


Figure 43

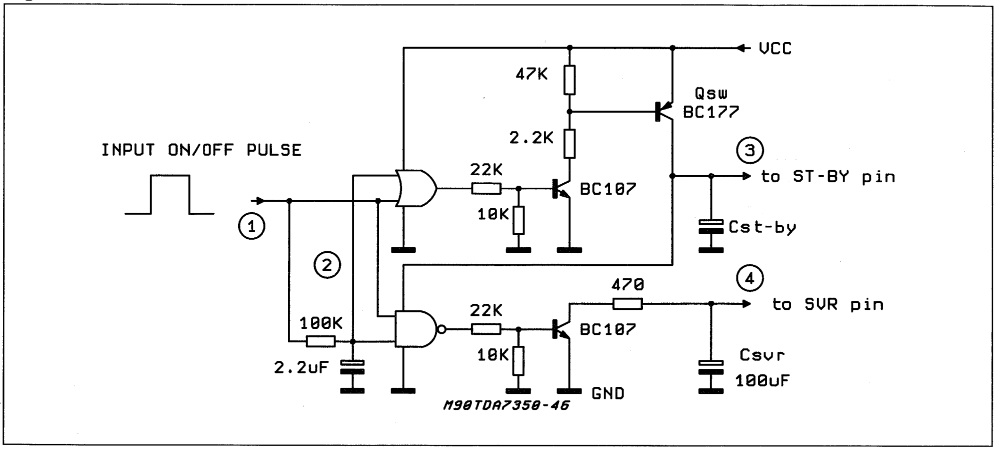


Figure 44

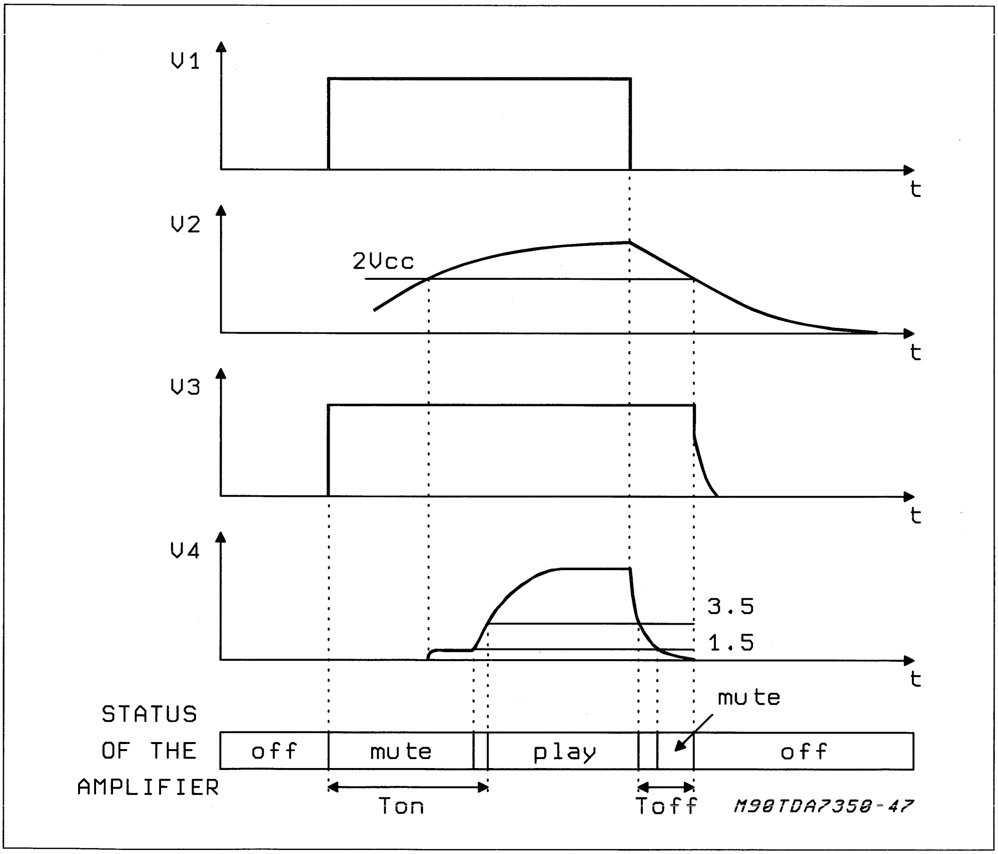
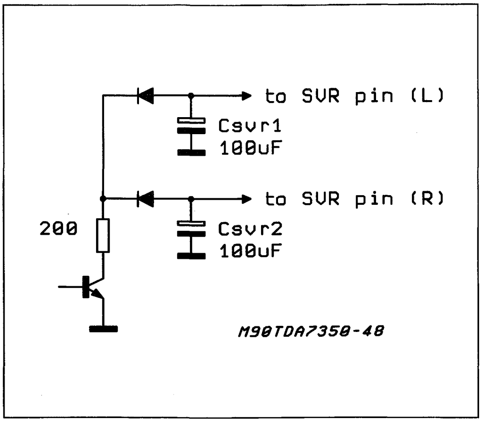


Figure 45



BALANCED INPUT IN BRIDGE CONFIGURATION

A helpful characteristic of the TDA7360 is that,in bridge configuration, a signal present on both the input capacitors is amplified by the same amount and it is present in phase at the outputs,so this signal does not produce effects on the load.The typical value of CMRR is 46 dB.

Looking at fig 46, we can see that a noise signal from the ground of the power amplifier to the ground of the hypothetical preamplifier is amplified of a factor equal to the gain of the amplifier (2 * Gv).

Using a configuration of fig. 47 the same ground noise is present at the output multiplied by the factor 2 * Gv/200.

This means less distortion,less noise (e.g. motor cassette noise) and/or a simplification of the layout of PC board.

The only limitation of this balanced input is the maximum amplitude of common mode signals (few tens of millivolt) to avoid a loss of output power due to the common mode signal on the output, but in a large number of cases this signal is within this range.

Figure 46

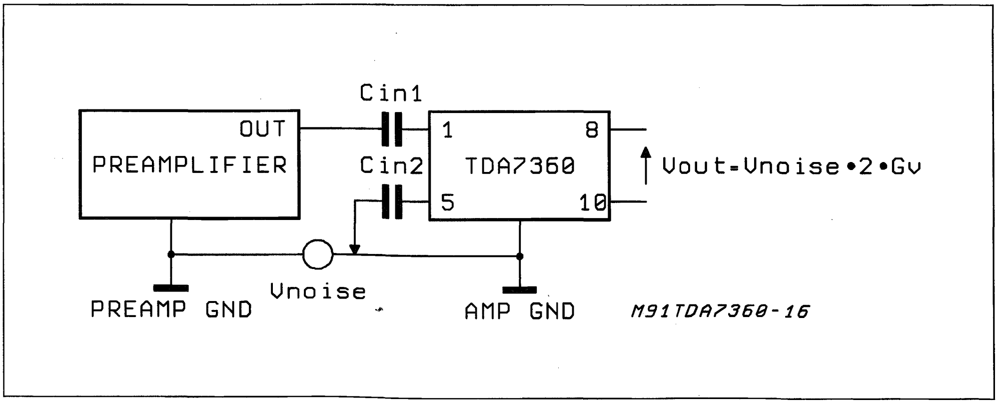
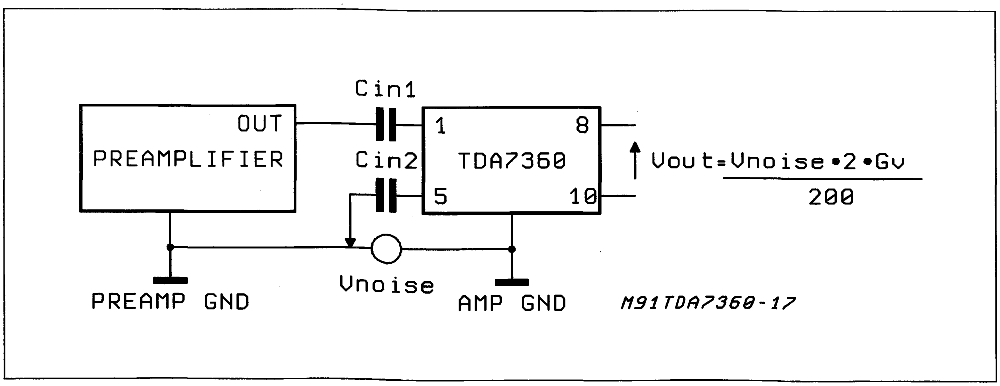


Figure 47



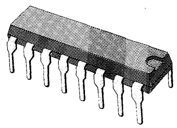
LOW VOLTAGE NBFM IF SYSTEM

- OPERATION FROM 1.8V TO 9V
- LOW DRAIN CURENT (4mA, V_s = 4V)
- HIGH SENSITIVITY (-3dB INPUT LIMITING AT 3μV)
- 8μV INPUT FOR 20dB S/N
- LOW EXTERNAL FAIR COUNT

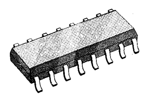
The TDA7361 is a low-power narrow band FM IF demodulation system operable to less than 2V supply voltage.

The device includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Op. Amp. Squelch, Scan Control and Mute Switch.

The TDA7361 is designed for use in **NBFM** dual conversion communication equipments using a 455KHz ceramic filter like cordless telephones, walkie-talkies, scan receivers, etc.



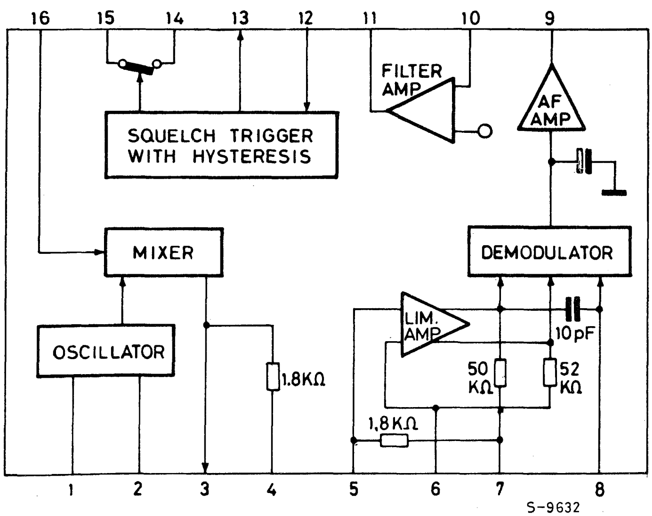
DIP-16 Plastic (0.25)



SO-16

ORDERING NUMBERS: TDA7361 (DIP-16)
TDA7361D (SO-16)

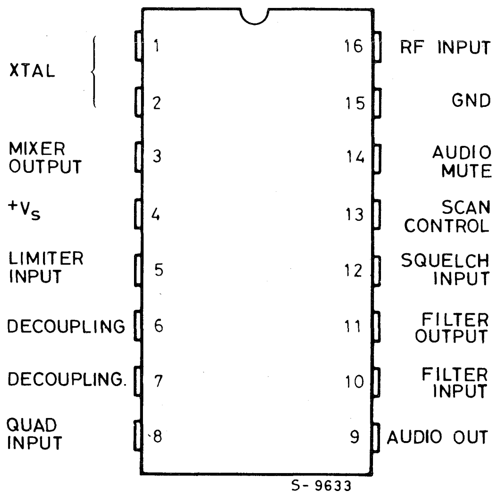
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	9	V
V_I	RF input voltage (pin 16)	1	V_{rms}
V_8	Detector input voltage	1	V_{pp}
V_{14}	Mute function voltage	-0.5 to 5	V
T_{op}	Operating ambient temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

			DIP-16	SO-16
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100°C/W	200°C/W

PIN FUNCTION

N°	NAME	FUNCTION
1-2	XTAL OSCILLATOR	Connections for the Colpitts XTAL oscillator. The XTAL may be replaced by an inductor (see fig. 5) if the application does not require high stability.
3	MIXER OUT	The Mixer is double balanced to reduce spurious products. The output impedance is 1.8KΩ to match the input impedance of a 455KHz ceramic filter.
4	SUPPLY VOLTAGE	Must be well decoupled with a 100nF ceramic capacitor.
5	IF LIMITER INPUT	Input pin of the six stages amplifier with about 50μV limiting sensitivity and 1.8KΩ input impedance. The if output is connected to the external quadrature coil (pin 8) via an internal 10pF capacitor.
6-7	DECOUPLING	Good quality 100nF ceramic capacitors and a suitable layout are important.
8	QUADRATURE COIL	A quadrature detector is used to demodulate the 455KHz FM signal. The Q of the quad coil has direct effect on output level and distortion (see fig. 6). For proper operation the voltage should be $100mV_{rms}$.
9	AUDIO OUTPUT SIGNAL	The audio Output signal is buffered by an internal emitter follower.
10	OP AMPLIFIER INPUT	Because of the Low DC bias, the swing on the operational amplifier output is limited to $500mV_{rms}$.
11	OP AMPLIFIER OUTPUT	This can be increased by adding a resistor from the operational amplifier input to ground.
12	SQUELCH INPUT	The squelch trigger circuit with a Low bias on the input (pin 12) will force pin 13 high; and pin 14 Low.
13	SCAN CONTROL	Pulling pin 12 above mute threshold (0.65V) will force pin 13 to an impedance of about 60KΩ to ground and pin 14 will be an open circuit.
14	MUTE	An hysteresis of about 50mV at pin 12 will effectively prevent jitter.
15	GND	Ground connection.
16	10.7MHz MIXER INPUT	Input of the wide-band mixer. Normally used as 10MHz/455KHz converter, it can be also used with input frequencies up to 60MHz.

ELECTRICAL CHARACTERISTICS ($V_s = 4V$; $f_o = 10.7MHz$; $\Delta f = \pm 3KHz$; $f_m = 1KHz$; T_{amb} = 25°C unless otherwise noted)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range		1.8	4	9	V
I_s	Supply current	Squelch OFF Squelch ON		3.8 4.7		mA
V_i	Input quieting voltage	S/N = 20dB		8		µV
V_i	Input limiting voltage	-3dB limiting		3		µV
V_o	Recovered audio output	V_i = 10mV		150		mV_{rms}
V_9	Detector output voltage			1.5		V_{DC}
R_9	Detector output impedance			400		Ω
	Detector center frequency slope			150		mV/KHz
G_v	Operational amplifier gain	f = 10KHz $G_v = V_{11}/V_{10}$	40	55		dB
V_{11}	Operational amplifier output voltage			1.5		V_{DC}
I_B	Operational amplifier input bias current	Pin 10		20		nA
V_T	Trigger hysteresis			50		mV
R_m	Mute switching impedance	LOW		50		Ω
		HIGH		10		MΩ
V_{13}	Scan voltage	Pin 12 HIGH (2V) Pin 12 LOW (0V)	 3.0	0 3.4	0.5	V_{DC}
G_c	Mixer converter gain			30		dB
R_i	Input resistance			3.3		KΩ
C_i	Input capacitance			2.2		pF

Fig. 2 - Test circuit

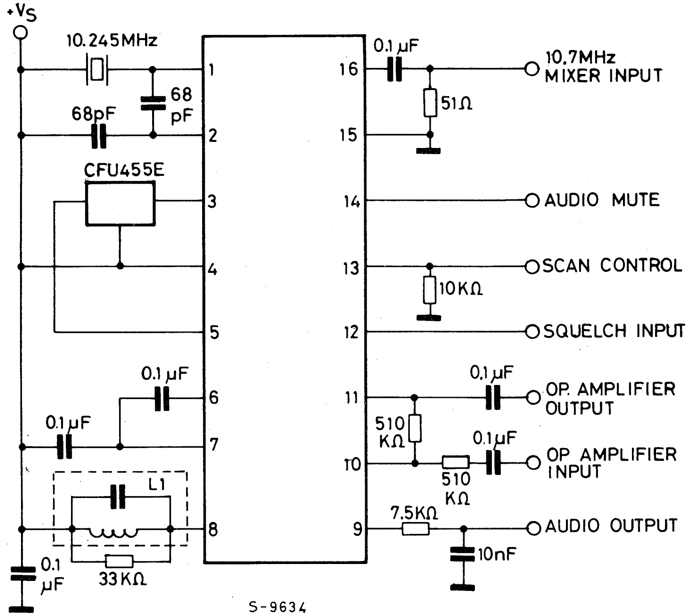


Fig. 3 - Supply current vs. supply voltage

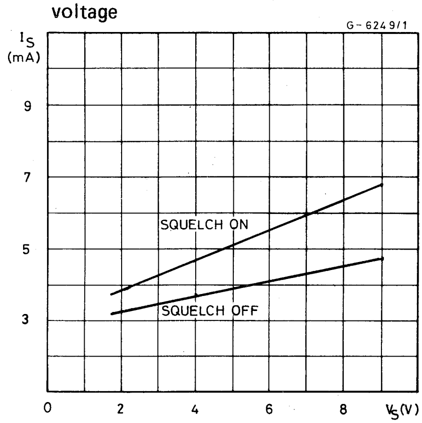


Fig. 4 - FM IF characteristics

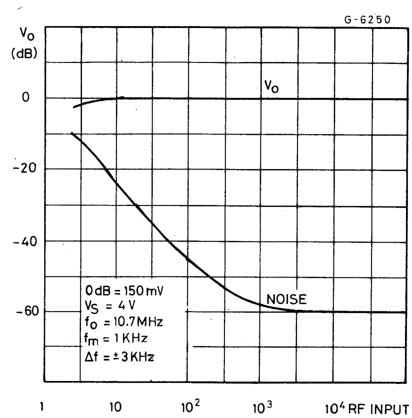


Fig. 5 - Colpitts XTAL oscillator

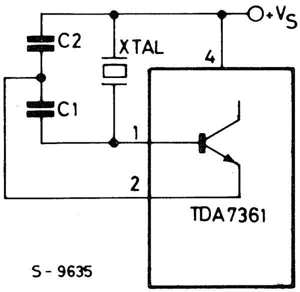
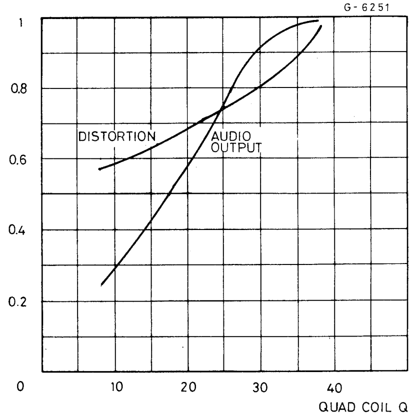


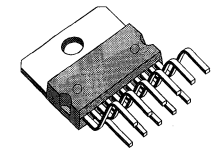
Fig. 6 - Effect of quadrature coil "Q" on audio level and distortion



2x8W CAR RADIO AMPLIFIER WITH CLIPPING DETECTOR

ADVANCE DATA

- VERY FEW EXTERNAL COMPONENTS
- NO BOUCHEROT CELLS
- NO BOOTSTRAP CAPACITORS
- FIXED GAIN (30dB)
- LOW OUTPUT VOLTAGE DROP
- NO SWITCH ON/OFF NOISE
- VERY LOW STAND-BY CURRENT
- PROGRAMMABLE TURN-ON DELAY
- CLIPPING DETECTION



Multiwatt-11
ORDERING NUMBER: TDA7362

PROTECTIONS:
- OUTPUT AC-DC SHORT CIRCUIT TO GROUND AND TO SUPPLY VOLTAGE
- VERY INDUCTIVE LOADS
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GROUND
- ESD

DESCRIPTION

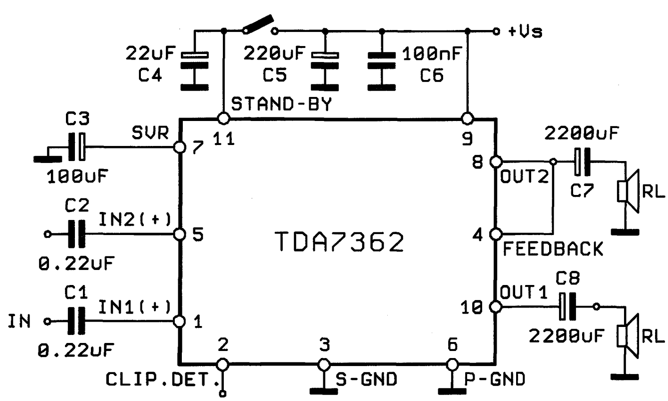
The TDA7362 is a new technology class AB Audio Power Amplifier in Multiwatt package designed for car radio applications.

Thanks to the fully complementary PNP/NPN output configuration the power performances of the TDA7362 are obtained without the boostrap capacitors.

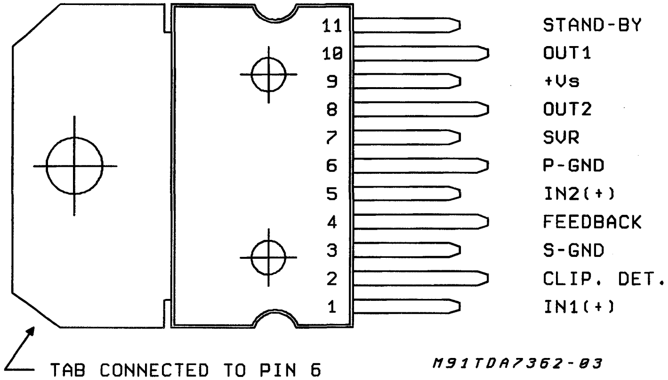
A delayed turn-on mute circuit eliminates audible on/off noise, and a novel short circuit protection system prevents spurious intervention with highly inductive loads.

The device provides a circuit for the detection of clipping in the output stages. The output, an open collector, is able to drive systems with automatic volume control.

APPLICATION CIRCUIT



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	28	V
V_{OP}	Operating Supply Voltage	18	V
V_{PEAK}	Peak Supply Voltage (t = 50ms)	40	V
I_O	Output Peak Current (non repetitive t = 100µs)	5	A
I_O	Output Peak Current (repetitive f > 10Hz)	4	A
P_{tot}	Power Dissipation T_{case} = 85°C	36	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_S = 14.4V; f = 1KHz, T_{amb} = 25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range		8		18	V
Id	Total Quiescent Drain Current				150	mA
A_{SB}	Stand-by attenuation		60	80		dB
I_{SB}	Stand-by Current				100	μA
I_{CO}	Clip Detector Average Current	d = 1% pin2 pull-up to 5V with 10KΩ R_L = 3.2Ω		70		μA
		d = 10% pin2 pull-up to 5V with 10KΩ R_L = 3.2Ω		120		μA
P_O	Output Power (each channel)	d = 10% R_L = 2Ω R_L = 3.2Ω R_L = 4Ω	 7 	 11 8 6.5		 W W W
		d = 10%; V_S = 13.2V R_L = 2Ω R_L = 3.2Ω R_L = 4Ω		 9 6.5 5.5		 W W W
d	Distortion	P_O = 0.1 to 4W; R_L = 3.2Ω			0.5	%
SVR	Supply Voltage Rejection	R_S = 10KΩ f = 100Hz C3 = 22μF C3 = 100μF	 40 	 57		 dB dB
CT	Crosstalk	f = 1KHz f = 10KHz	40 	 57		dB dB
R_i	Input Resistance		30	50		KΩ
G_V	Voltage Gain		27	29	31	dB
G_V	Voltage Gain Match				1	dB
E_{IN}	Input Noise Voltage	R_S = 50Ω (*) R_S = 10KΩ (*) R_S = 50Ω (**) R_S = 10KΩ (**)		1.5 2 2 	 7	μV μV μV μV
T_{sd}	Thermal Shutdown Junction Temperature			145		°C

(*) Curve A
(**) 22Hz to 22KHz

Figure 1: Test and Application Circuit

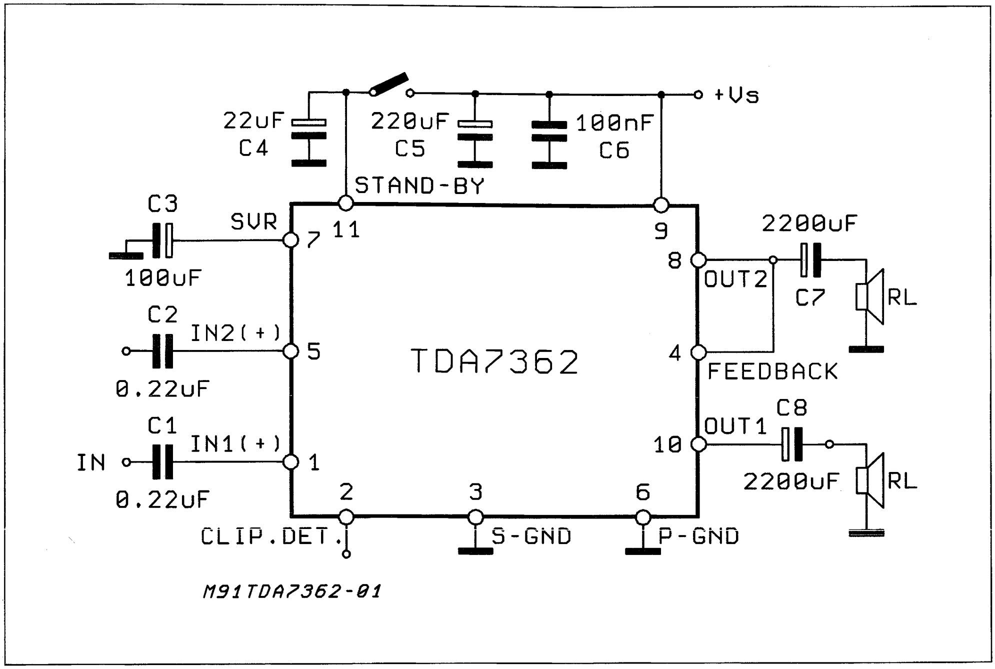
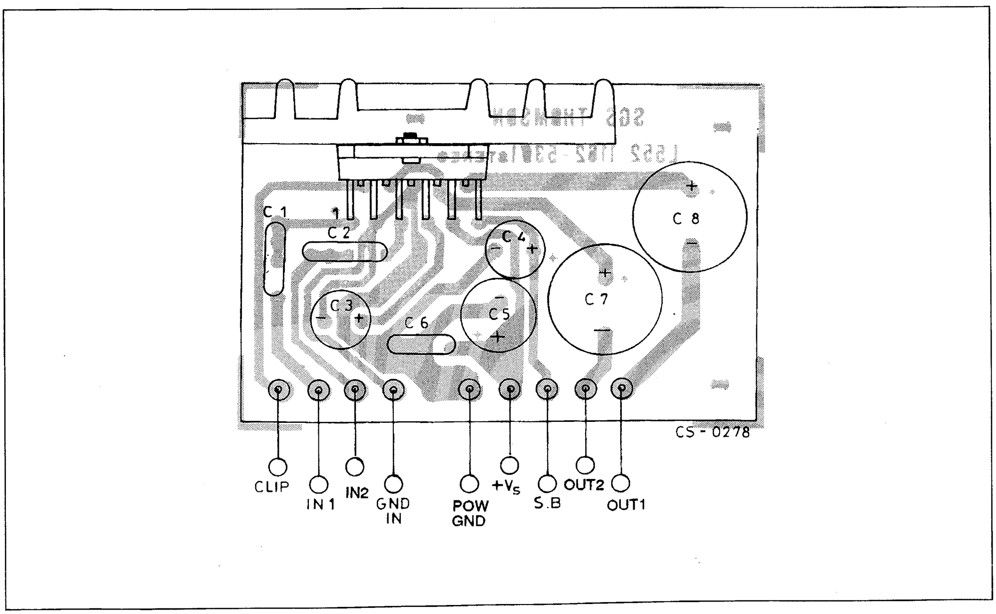


Figure 2: P.C. Board and Component Layout of the Circuit of Fig. 1 (1:1 scale)



RECOMMENDED VALUES OF THE EXTERNAL COMPONENTS (ref to the Test and Application Circuit)

Component	Recommended Value	Purpose	Larger than the Recomm. Value	Smaller than the Recomm. Value
C1	0.22µF	Input Decoupling (CH1)	—	—
C2	0.22µF	Input Decoupling (CH2)	—	—
C3	100µF	Supply Voltage Rejection Filtering Capacitor	Longer Turn-On Delay Time	Worse Supply Voltage Rejection. Shorter Turn-On Delay Time Danger of Noise (POP)
C4	22µF	Stand-By ON/OFF Delay	Delayed Turn-Off by Stand-By Switch	Danger of Noise (POP)
C5	220µF (min)	Supply By-Pass		Danger of Oscillations
C6	100nF (min)	Supply By-Pass		Danger of Oscillations
C7	2200µF	Output Decoupling CH2	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay
C8	2200µF	Output Decoupling CH1	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay

Figure 3: Output Power vs. Supply Voltage

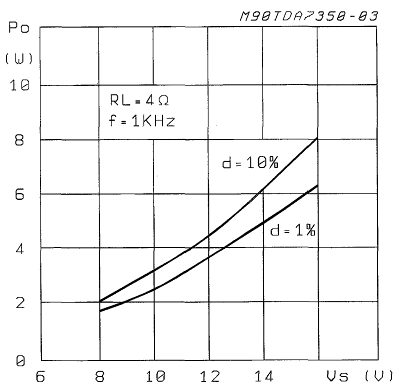


Figure 4: Output Power vs. Supply Voltage

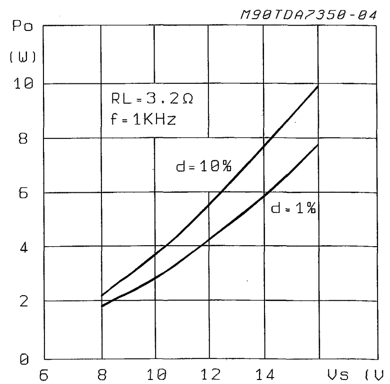


Figure 5: Output Power vs. Supply Voltage

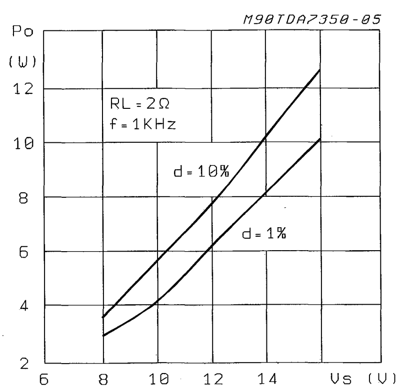


Figure 6: Drain Current vs. Supply Voltage

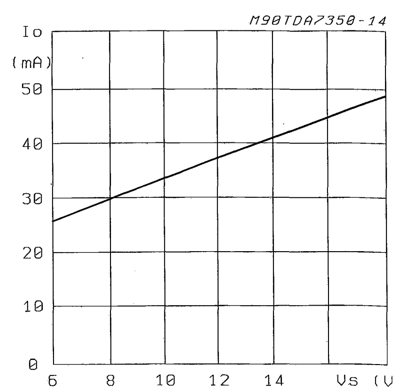


Figure 7: Distortion vs. Output Power

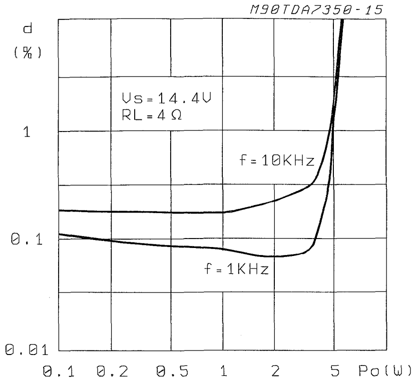


Figure 8: Distortion vs. Output Power

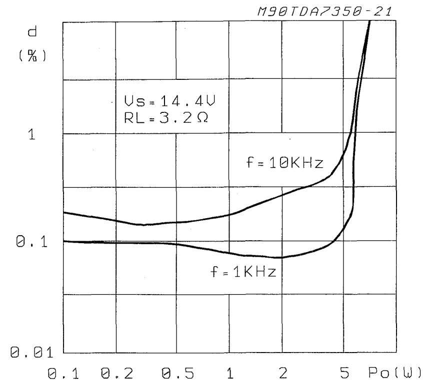


Figure 9: Distortion vs. Output Power

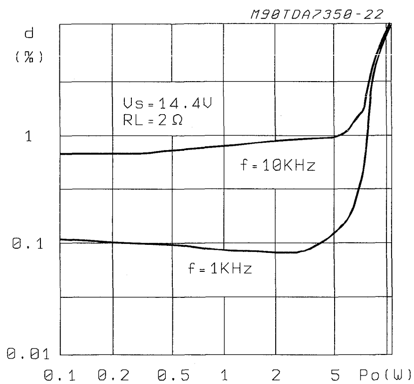


Figure 10: SVR vs. Frequency & C3

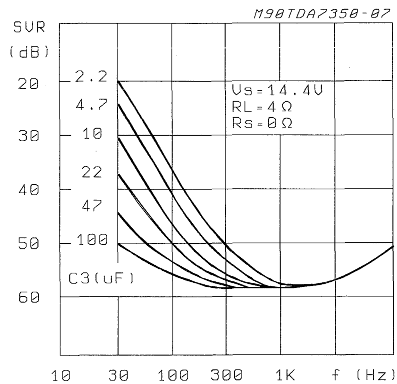


Figure 11: SVR vs. Frequency & C3

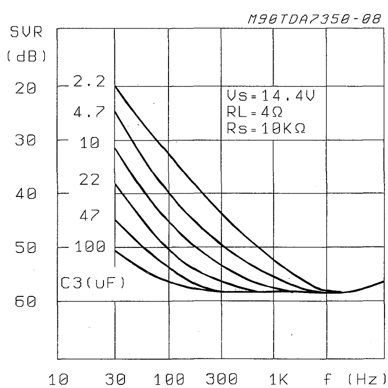


Figure 12: Crosstalk vs. Frequency

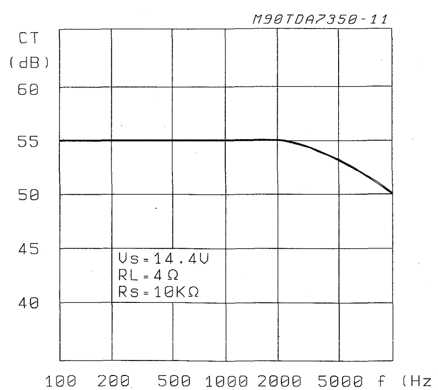


Figure 13: Power Dissipation & Efficiency vs. Output Power

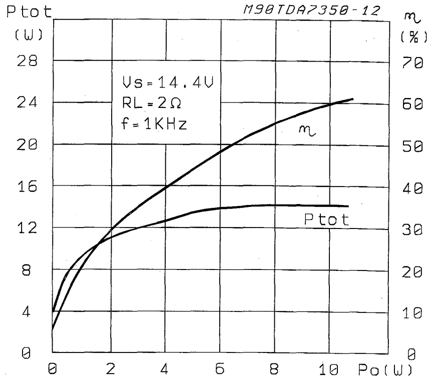
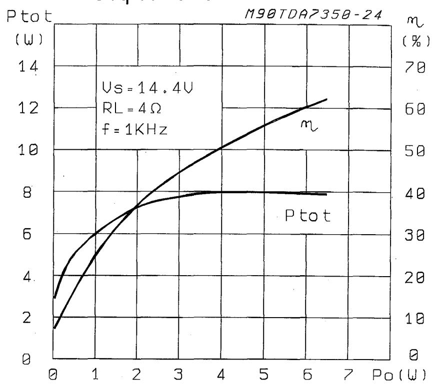


Figure 14: Power Dissipation & Efficiency vs. Output Power



AMPLIFIER ORGANIZATION

The TDA7362 has been developed taking care of the key concepts of the modern power audio amplifier for car radio such as: space and costs saving due to the minimized external count, excellent electrical performances, flexibility in use, superior reliability thanks to a built-in array of protections. As a result the following performances has been achieved:

- NO NEED OF BOOTSTRAP CAPACITORS
- ABSOLUTE STABILITY WITHOUT EXTERNAL COMPENSATION THANKS TO THE INNOVATIVE OUT STAGE CONFIGURATION, ALSO ALLOWING INTERNALLY FIXED CLOSED LOOP LOWER THAN COMPETITORS
- LOW GAIN (30dB FIXED WITHOUT ANY EXTERNAL COMPONENTS) IN ORDER TO MINIMIZE THE OUTPUT NOISE AND OPTIMIZE SVR
- SILENT MUTE/ST-BY FUNCTION FEATURING ABSENCE OF POP ON/OFF NOISE
- HIGH SVR
- AC/DC SHORT CIRCUIT PROTECTION (TO GND, TO V_S, ACROSS THE LOAD)
- LOUDSPEAKER PROTECTION
- DUMP PROTECTION
- ESD PROTECTION

BLOCK DESCRIPTION

Polarization

The device is organized with the gain resistors directly connected to the signal ground pin i.e. without gain capacitors (fig. 15).

The non inverting inputs of the amplifiers are connected to the SVR pin by means of resistor dividers, equal to the feedback networks. This allows the outputs to track the SVR pin which is sufficiently slow to avoid audible turn-on and turn-off transients.

SVR

The voltage ripple on the outputs is equal to the one on SVR pin: with appropriate selection of C_{SVR}, more than 55dB of ripple rejection can be obtained.

Delayed Turn-on (muting)

The C_{SVR} sets a signal turn-on delay too. A circuit is included which mutes the device until the voltage on SVR pin reaches ~2.5V (fig. 16). The mute function is obtained by duplicating the input differential pair (fig. 17): it can be switched to the signal source or to an internal mute input. This feature is necessary to prevent transients at the inputs reaching the loudspeaker(s) immediately after power-on).

Fig. 17 represents the detailed turn-on transient.
At the power-on the output decoupling capacitors are charged through an internal path but the device itself remains switched off (Phase 1 of the represented diagram).
When the outputs reach the voltage level of about 1V (this means that there is no presence of short circuits) the device switches on, the SVR capacitor starts charging itself and the output tracks exactly the SVR pin.
During this phase the device is muted until the SVR reaches the "Play" threshold (~2.5V), after that the music signal starts being played.

Stand-by
The device is also equipped with a stand-by function, so that a low current, and hence low cost switch, can be used for turn on/off.

Stability
The device is provided with an internal compensation wich allows to reach low values of closed loop gain.
In this way better performances on S/N ratio and SVR can be obtained.

Figure 15: Block Diagram; Stereo Configuration

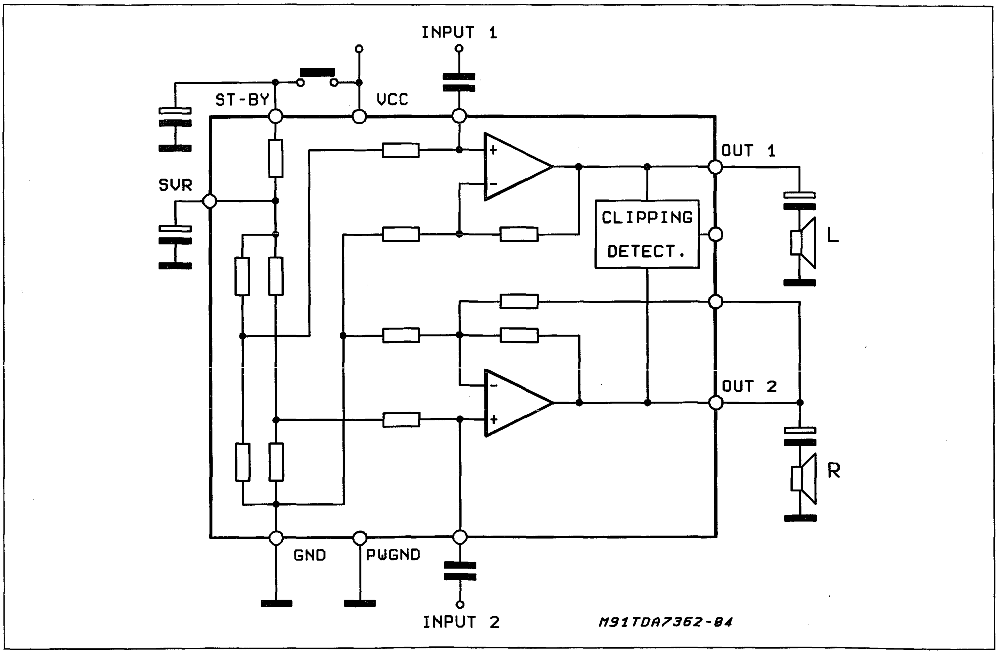


Figure 16: Mute Function Diagram

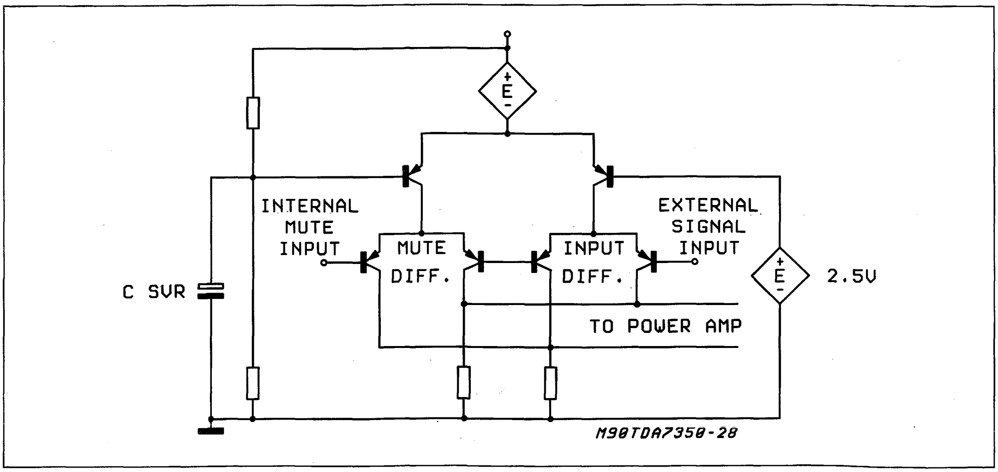
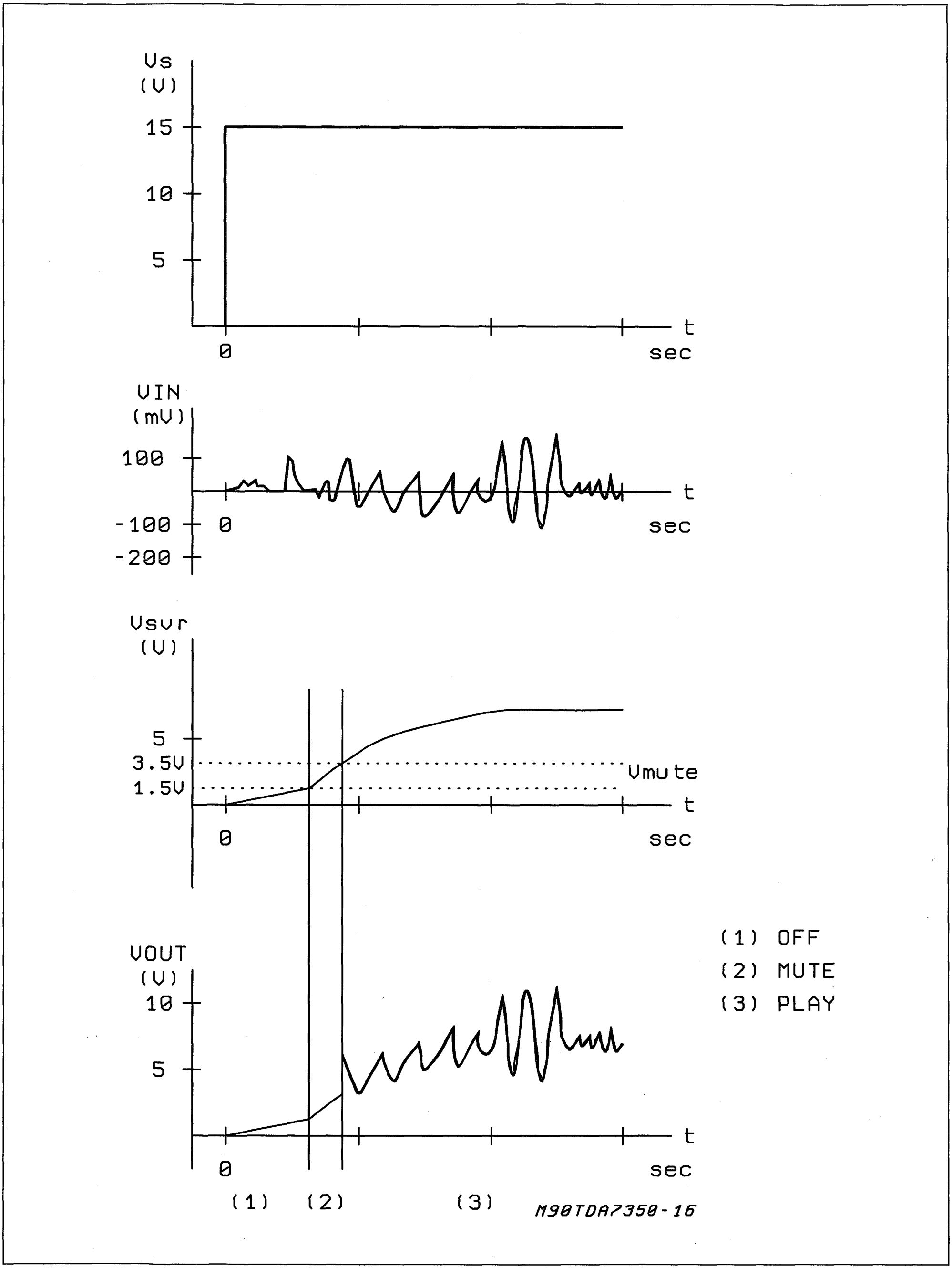


Figure 17: Turn-on Delay Circuit



CLIP DETECTOR

The TDA7362 is equipped with an internal circuit able to detect the output stage saturation providing a proper current sinking into a open collector out. (pin2) when a certain distortion level is reached at each output. This particular function allows compression facility whenever the amplifier is overdriven, so obtaining high quality sound at all listening levels.

Figure 18: Dual Channel Distortion Detector

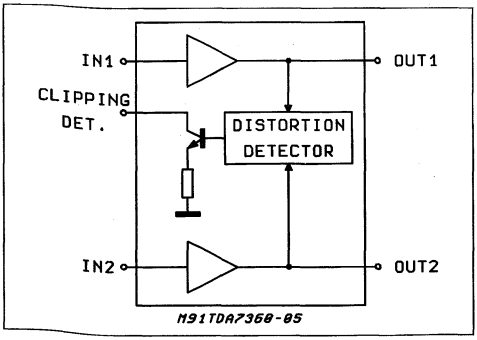


Figure 19: Output at Clipping Detector Pin vs. Signal Distortion

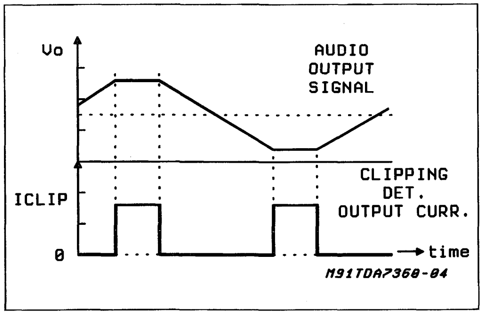


Figure 20: ICV - PNP Gain vs. Ic

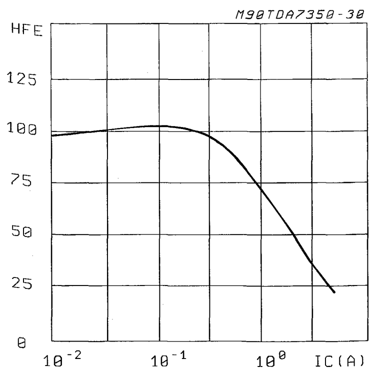


Figure 21: ICV - PNP $V_{CE(sat)}$ vs. Ic

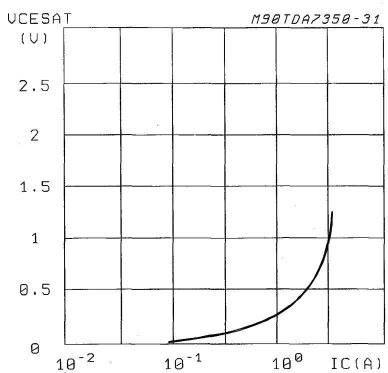
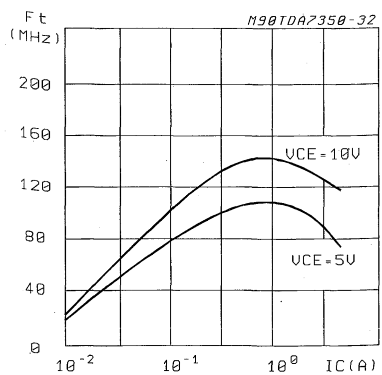


Figure 22: ICV - PNP cut-off Frequency vs. Ic



OUTPUT STAGE

Poor current capability and low cutoff frequency are well known limits of the standard lateral PNP. Composite PNP-NPN power output stages have been widely used, regardless their high saturation drop. This drop can be overcome only at the expense of external components, namely, the bootstrap capacitors. The availability of 4A isolated collector PNP (ICV PNP) adds versatility to the design. The performance of this component, in terms of gain, V_{CEsat} and cut-off frequency, is shown in fig. 20, 21, 22 respectively. It is realized in a new bipolar technology, characterized by top-bottom isolation techniques, allowing the implementation of low leakage diodes, too. It guarantees BV_{CEO} > 20V and BV_{CBO} > 50V both for

NPN and PNP transistors. Basically, the connection shown in fig. 23 has been chosen. First of all because its voltage swing is rail-to-rail, limited only by the VCEsat of the output transistors, which are in the range of 0.3Ω each. Then, the gain VOUT/VIN is greater than unity, approximately 1+R2/R1. (VCC/2 is fixed by an auxiliary amplifier common to both channel). It is possible, controlling the amount of this local feedback, to force the loop gain (A . β) to less than unity at frequencies for which the phase shift is 180°. This means that the output buffer is intrinsically stable and not prone to oscillation.

In contrast, with the circuit of fig. 24, the solution adopted to reduce the gain at high frequencies is the use of an external RC network.

AMPLIFIER BLOCK DIAGRAM

The block diagram of each voltage amplifier is shown in fig. 25. Regardless of production spread, the current in each final stage is kept low, with enough margin on the minimum, below which cross-over distortion would appear.

Figure 23: The New Output Stage

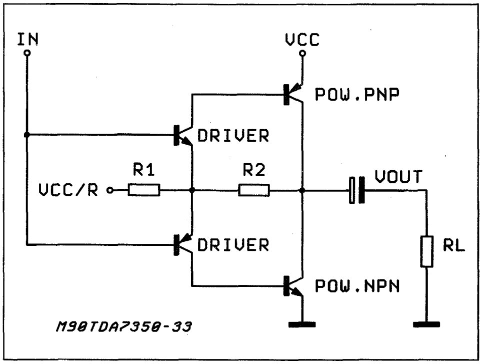


Figure 24: A Classic Output Stage

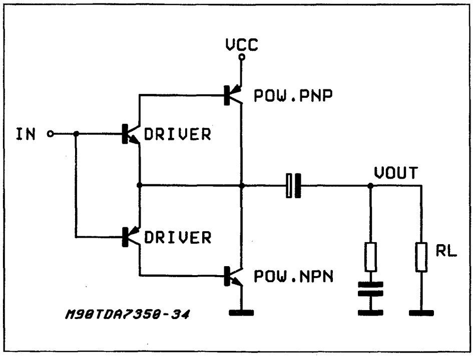
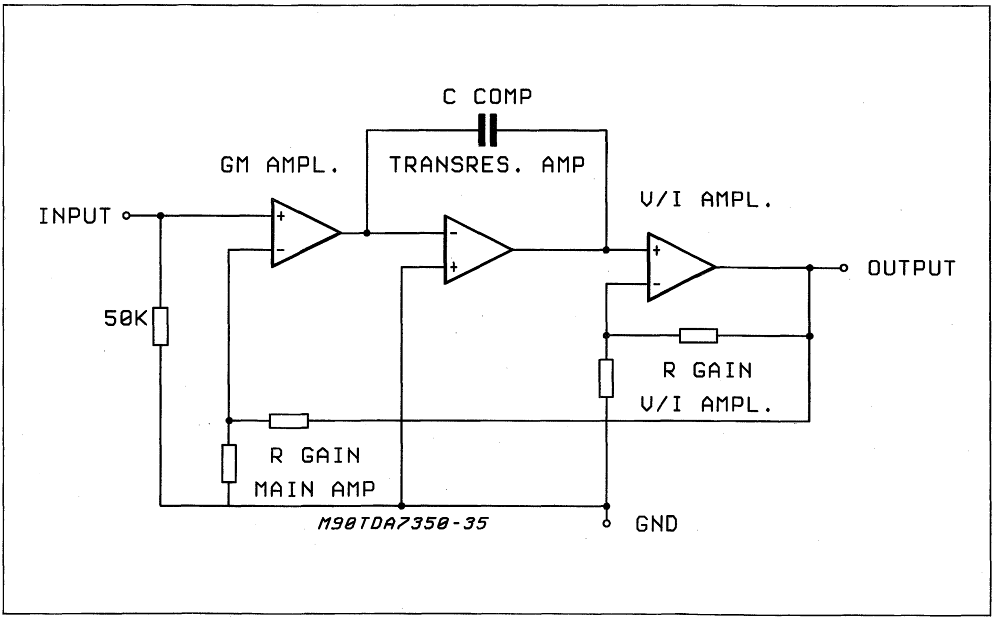


Figure 25: Amplifier Block Diagram



BUILT-IN PROTECTION SYSTEMS

Short Circuit Protection

The maximum current the device can deliver can be calculated by considering the voltage that may be present at the terminals of a car radio amplifier and the minimum load impedance.

Apart from consideration concerning the area of the power transistors it is not difficult to achieve peak currents of this magnitude (5A peak).
However it becomes more complicated if AC and DC short circuit protection is also required.In particular,with a protection circuit which limits the output current following the SOA curve of the output transistors it is possible that in some conditions (highly reactive loads, for example) the protection circuit may intervene during normal operation. For this reason each amplifier has been equipped with a protection circuit that intervenes when the output current exceeds 4A.

Fig 26 shows the protection circuit for an NPN power transistor (a symmetrical circuit applies to PNP).The VBE of the power is monitored and gives out a signal,available through a cascode.

This cascode is used to avoid the intervention of the short circuit protection when the saturation is below a given limit.

The signal sets a flip-flop which forces the amplifier outputs into a high impedance state.

In case of DC short circuit when the short circuit is removed the flip-flop is reset and restarts the circuit (fig. 30). In case of AC short circuit, the device is continuously switched in ON/OFF conditions and the current is limited.

Load Dump Voltage Surge

The TDA7362 has a circuit which enables it to withstand a voltage pulse train on pin 9, of the type shown in fig. 28.
If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.

A suggested LC network is shown in fig. 27
With this network, a train of pulses with amplitude up to 120V and width of 2ms can be applied at point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Figure 26: Circuitry for Short Circuit Detection

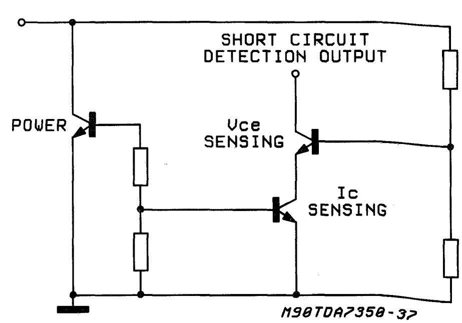


Figure 27.

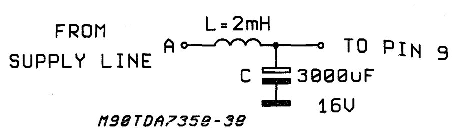


Figure 28.

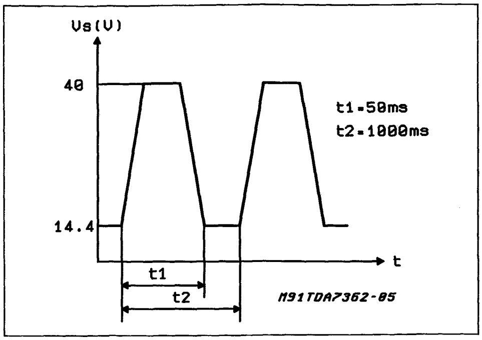
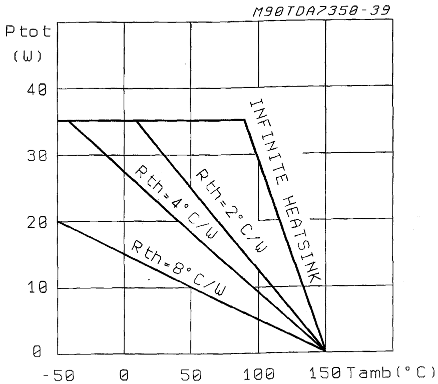


Figure 29: Maximum Allowable Power Dissipation vs. Ambient Temperature



Polarity Inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This features is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open Ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA7362 protection diodes are included to avoid any damage.

DC Voltage

The maximum operating DC voltage for the TDA7362 is 18V.

However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

Thermal Shut-down

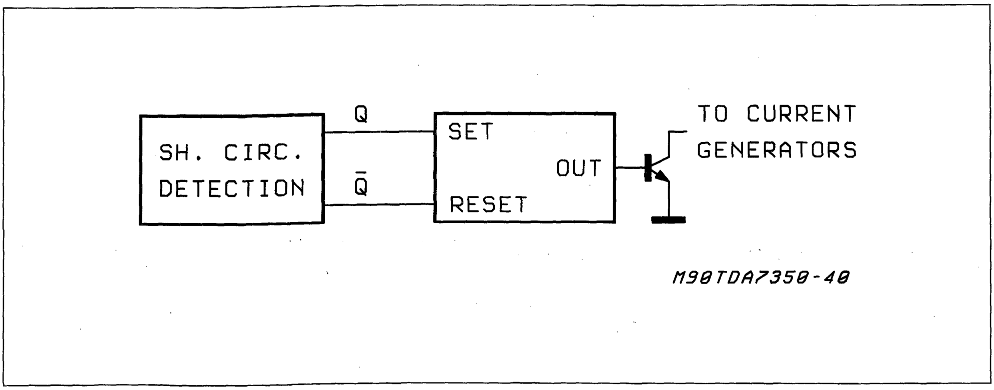
The presence of a thermal limiting circuit offers the following advantages:

1)an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2)the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 29 shows the dissipable power as a function of ambient temperature for different thermal resistance.

Figure 30: Restart Circuit



APPLICATION HINTS

This section explains briefly how to get the best from the TDA7362 and presents some application circuits with suggestions for the value of the components.These values can change depending on the characteristics that the designer of the car radio wants to obtain,or other parts of the car radio that are connected to the audio block.

To optimize the performance of the audio part it is useful (or indispensable) to analyze also the parts outside this block that can have an interconnection with the amplifier.

This method can provide components and system cost saving.

Reducing Turn On-Off Pop

The TDA7362 has been designed in a way that the turn on(off) transients are controlled through the charge(discharge) of the Csvr capacitor (C3).

As a result of it, the turn on(off) transient spectrum contents is limited only to the subsonic range.The following section gives some brief notes to get the best from this design feature.

TURN-ON

Fig 31 shows the output waveform (before and after the "A" weighting filter) compared to the value of Csvr.

Better pop-on performance is obtained with higher Csvr values (the recommended range is from 22uF to 220uF).

The turn-on delay (during which the amplifier is in mute condition) is a function essentially of : C_{out}, C_{svr}.

Being:

$$T1 \approx 120 \cdot C_{out}$$

$$T2 \approx 1200 \cdot C_{svr}$$

The turn-on delay is given by:

$$T1+T2$$

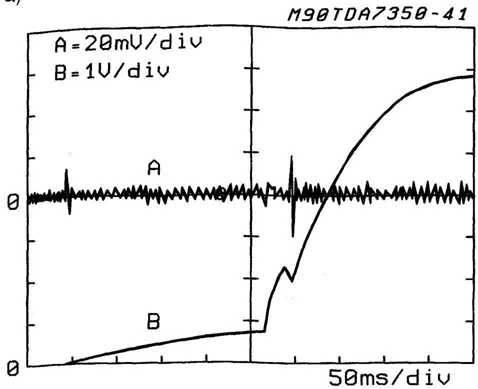
The best performance is obtained by driving the st-by pin with a ramp having a slope slower than 2V/ms.

TURN-OFF

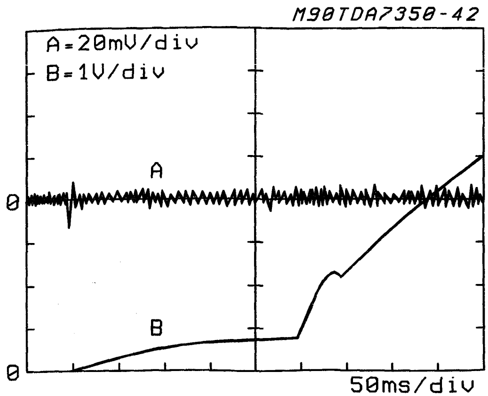
A turn-off pop can occur if the st-by pin goes low with a short time constant (this can occur if other

Figure 31:

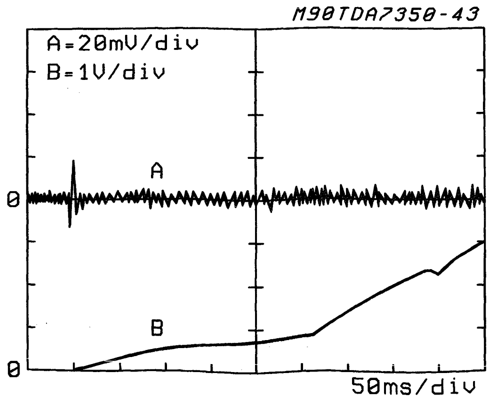
a) $C_{SVT} = 22\mu F$



b) $C_{SVT} = 47\mu F$



c) $C_{SVT} = 100\mu F$



car radio sections, preamplifiers,radio.. are supplied through the same st-by switch).
This pop is due to the fast switch-off of the internal current generator of the amplifier.
If the voltage present across the load becomes rapidly zero (due to the fast switch off) a small pop occurs, depending also on Cout,Rload.

The parameters that set the switch off time constant of the st-by pin are:

- the st-by capacitor Cst-by (C3)
- the SVR capacitor Csvr (C3)
- resistors connected from st-by pin to ground (Rext)

The time constant is given by :

$T \approx Csvr \cdot 2000\Omega // Rext + Cst\text{-}by \cdot 2500\Omega // Rext$

The suggested time constants are :

$T > 120ms$ with $C_{out}=1000\mu F, R_L = 4ohm$

$T > 170ms$ with $C_{out}=2200\mu F, R_L = 4ohm$

If Rext is too low the Csvr can become too high and a different approach may be useful (see next section).

Figg 32, 33 show some types of electronic switches (µP COMPATIBLE) suitable for supplying the st-by pin (it is important that Qsw is able to saturate with $V_{CE} \leq 150mV$).

GLOBAL APPROACH TO SOLVING POP PROBLEM BY USING THE MUTING/TURN ON DELAY FUNCTION

In the real case turn-on and turn-off pop problems are generated not only by the power amplifier,but also (very often) by preamplifiers,tone controls,radios etc. and transmitted by the power amplifier to the loudspeaker.

A simple approach to solving these problems is to use the mute characteristics of the TDA7362.

If the SVR pin is at a voltage below 1.5 V, the mute attenuation (typ)is 30dB .The amplifier is in play mode when Vsvr overcomes 3.5 V.

With the circuit of fig 34 we can mute the amplifier for a time Ton after switch-on and for a time Toff after switch-off.During this period the circuitry that precedes the power amplifier can produce spurious spikes that are not transmitted to the loudspeaker. This can give back a very simple design of this circuitry from the pop point of view.

A timing diagram of this circuit is illustrated in fig 35. Other advantages of this circuit are:

- A reduced time constant allowance of stand-by pin turn off.Consequently it is possible to drive all the car-radio with the signal that drives this pin.

-A better turn-off noise with signal on the output.

To drive two stereo amplifiers with this circuit it is possible to use the circuit of fig 36.

Figure 32

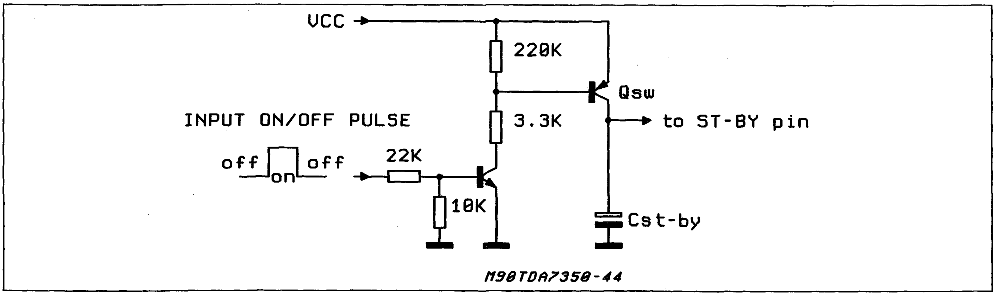


Figure 33

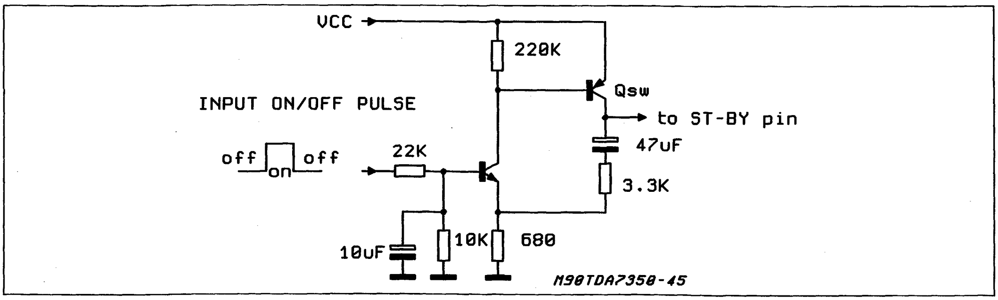


Figure 34

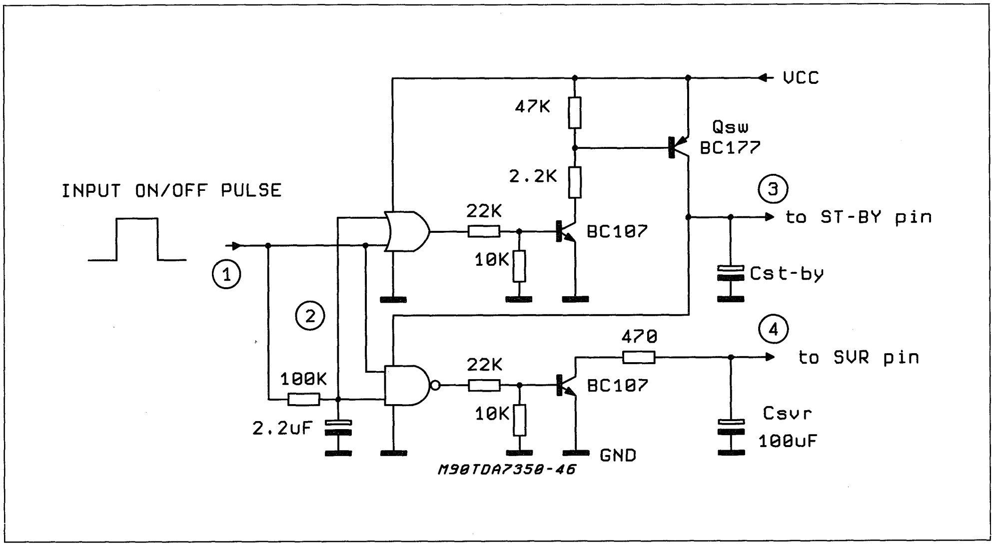


Figure 35

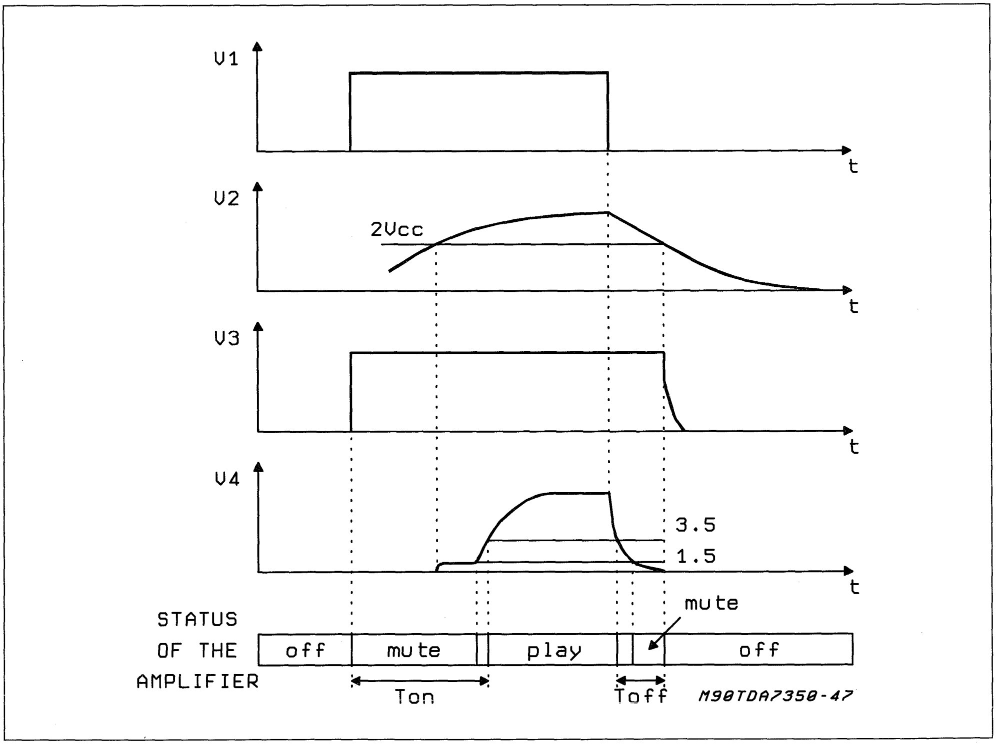
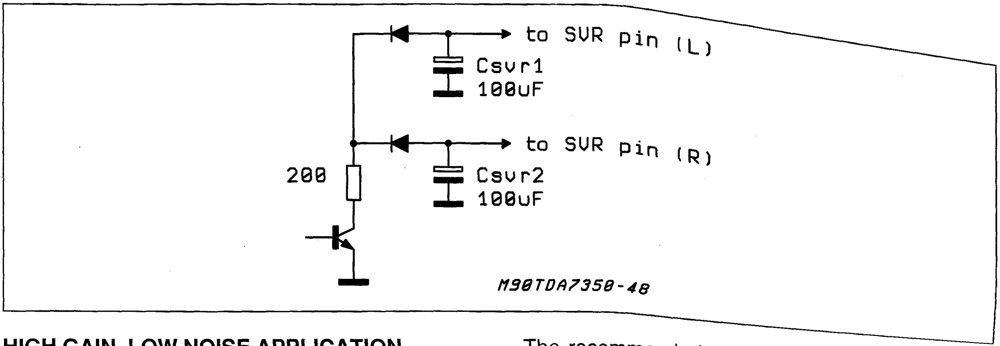


Figure 36



HIGH GAIN ,LOW NOISE APPLICATION

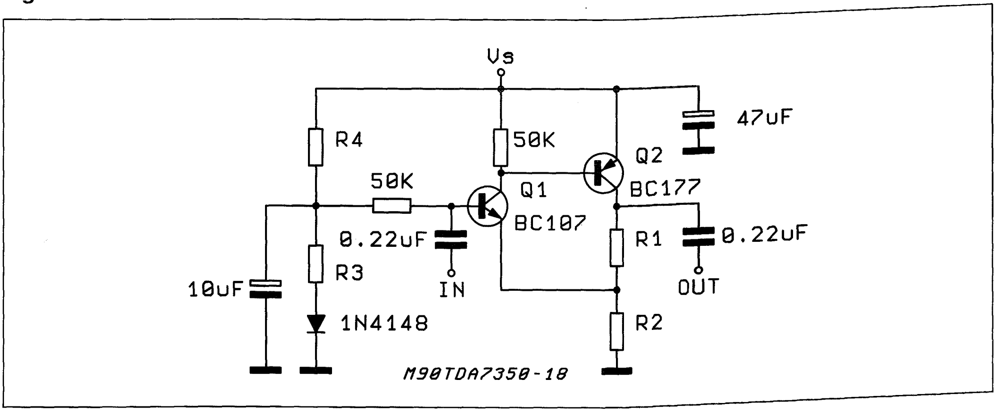
The following section describes a flexible preamplifier having the purpose to increase the gain of the TDA7362.

A two transistor network (fig. 37) has been adopted whose components can be changed in order to achieve the desired gain without affecting the good performances of the audio amplifier itself.

The recommended values for 40 dB overall gain are :

Resistance	Value
R1	10KΩ
R2	4.3KΩ
R3	10KΩ
R4	50KΩ

Figure 37



SGS-THOMSON MICROELECTRONICS

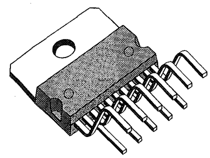
TDA7363

24W BRIDGE / STEREO AUDIO AMPLIFIER WITH CLIPPING DETECTOR

ADVANCE DATA

- VERY FEW EXTERNAL COMPONENTS
- NO BOUCHEROT CELLS
- NO BOOSTRAP CAPACITORS
- HIGH OUTPUT POWER
- NO SWITCH ON/OFF NOISE
- VERY LOW STAND-BY CURRENT
- FIXED GAIN (20dB STEREO)
- PROGRAMMABLE TURN-ON DELAY
- CLIPPING DETECTOR

Protections:
- OUTPUT AC-DC SHORT CIRCUIT TO GROUND AND TO SUPPLY VOLTAGE
- VERY INDUCTIVE LOADS
- LOUDSPEAKER PROTECTION
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GROUND
- ESD

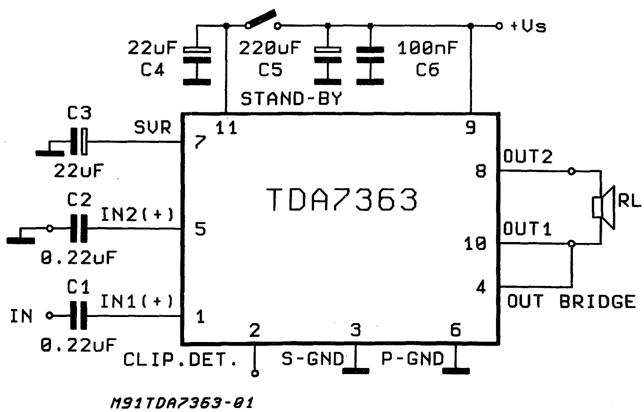


Multiwatt - 11

ORDERING NUMBER: TDA7363

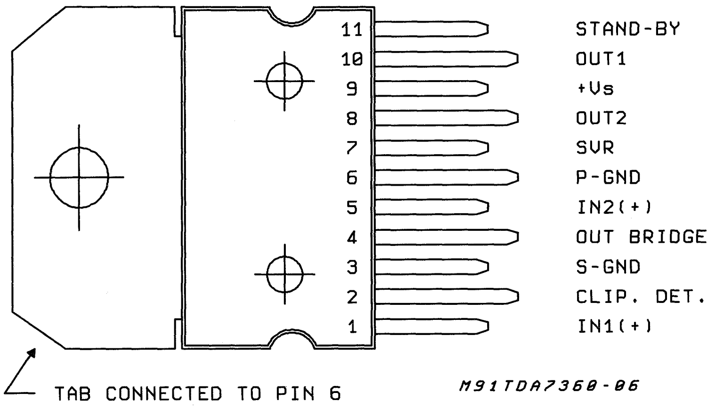
DESCRIPTION
The TDA7363 is a new technology class AB Audio Power Amplifier in the Multiwatt® package designed for car radio applications.
Thanks to the fully complementary PNP/NPN output configuration the high power performances of the TDA7363 is obtained without bootstrap capacitors.
A delayed turn-on mute circuit eliminates audible on/off noise, and a novel short circuit protection system prevents spurious intervention with highly inductive loads.
The device provides a circuit for the detection of clipping in the output stages. The output, an open collector, is able to drive systems with automatic volume control.

APPLICATION CIRCUIT (BRIDGE)



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Operating Supply Voltage	18	V
V_S	DC Supply Voltage	28	V
V_S	Peak Supply Voltage (for t = 50ms)	50	V
I_o	Output Peak Current (non rep. for t = 100µs)	5	A
I_o	Output Peak Current (rep. freq. > 10Hz)	4	A
P_{tot}	Power Dissipation at T_{case} = 85°C	36	W
T_{stg}, T_J	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description	Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case Max.	1.8	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, T_{amb} = 25°C, V_S = 14.4V, f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range		8		18	V
I_d	Total Quiescent Drain Current	stereo configuration			120	mA
A_{SB}	Stand-by attenuation		60	80		dB
I_{SB}	Stand-by Current				100	µA
I_{CO}	Clip Detector Average Current	pin2 pull-up to 5V with 10KΩ d = 1% d = 5%		70 130		µA µA

STEREO

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
P_o	Output Power (each channel)	d = 10% R_L = 1.6Ω R_L = 2Ω R_L = 3.2Ω R_L = 4Ω	 7 	 13 11 8 6.5		 W W W W
d	Distortion	P_O = 0.1 to 4W R_L = 3.2Ω		0.03	0.5	%
SVR	Supply Voltage Rejection	R_S = 10KΩ f = 100Hz; C3 = 22µF C3 = 100µF	45 	 62		dB dB
CT	Crosstalk	f = 1KHz f = 10KHz	45 	 55		dB dB
R_I	Input Resistance			50		KΩ
G_V	Voltage Gain			20		dB
G_V	Voltage Gain Match				1	dB
E_{IN}	Input Noise Voltage	22 Hz to 22KHz R_S = 50Ω R_S = 10KΩ		2.5 3	 7	µV µV

BRIDGE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OS}	Output Offset Voltage				250	mV
P_o	Output Power	d = 10%; R_L = 4Ω d = 10%; R_L = 3.2Ω	20 	24 28		W W
d	Distortion	P_o = 0.1 to 10W; R_L = 4Ω		0.04	1	%
SVR	Supply Voltage Rejection	R_S = 10KΩ f = 100Hz; C3 = 22µF C3 = 100µF	45 	 62		dB dB
R_I	Input Resistance			50		KΩ
G_V	Voltage Gain			26		dB
E_{IN}	Input Noise Voltage	22Hz to 22KHz R_S = 50Ω R_S = 10KΩ		3.5 4	 10	µV µV

Figure 1: STEREO Test and Appication Circuit

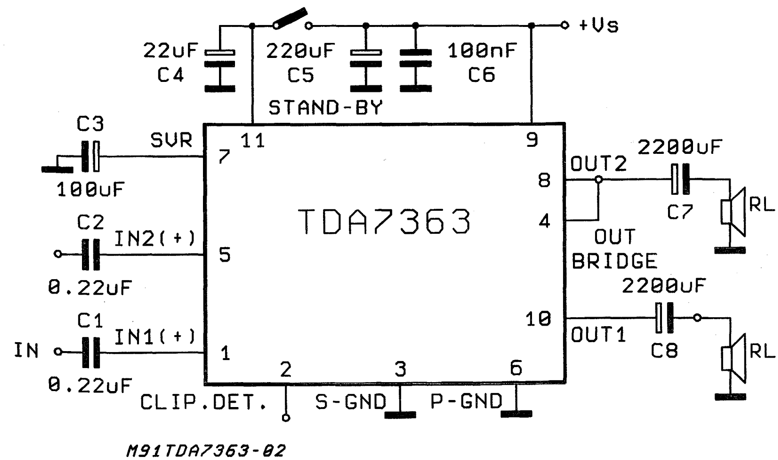
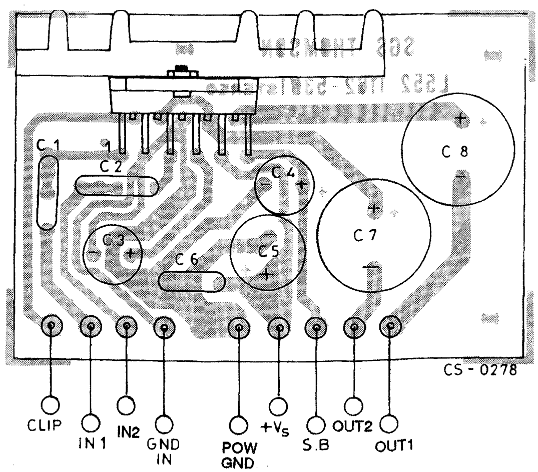


Figure 2: P.C. Board and Component Layout (STEREO) of the circuit of fig. 1 (1:1 scale)



RECOMMENDED VALUES OF THE EXTERNAL COMPONENTS (ref to the Stereo Test and Application Circuit)

Component	Recommended Value	Purpose	Larger than the Recomm. Value	Smaller than the Recomm. Value
C1	0.22µF	Input Decoupling (CH1)	—	—
C2	0.22µF	Input Decoupling (CH2)	—	—
C3	100µF	Supply Voltage Rejection Filtering Capacitor	Longer Turn-On Delay Time	- Worse Supply Voltage Rejection. - Shorter Turn-On Delay Time - Danger of Noise (POP)
C4	22µF	Stand-By ON/OFF Delay	Delayed Turn-Off by Stand-By Switch	Danger of Noise (POP)
C5	220µF (min)	Supply By-Pass		Danger of Oscillations
C6	100nF (min)	Supply By-Pass		Danger of Oscillations
C7	2200µF	Output Decoupling CH2	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay
C8	2200µF	Output Decoupling CH1	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay

Figure 3: BRIDGE Test and Appication Circuit

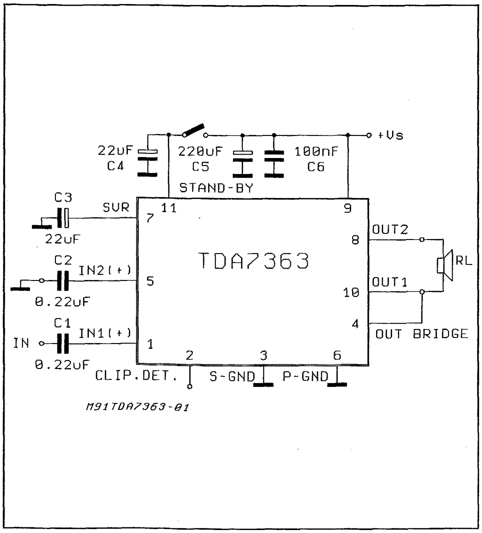


Figure 4: P.C. Board and Layout (BRIDGE) of the circuit of fig. 3 (1:1 scale)

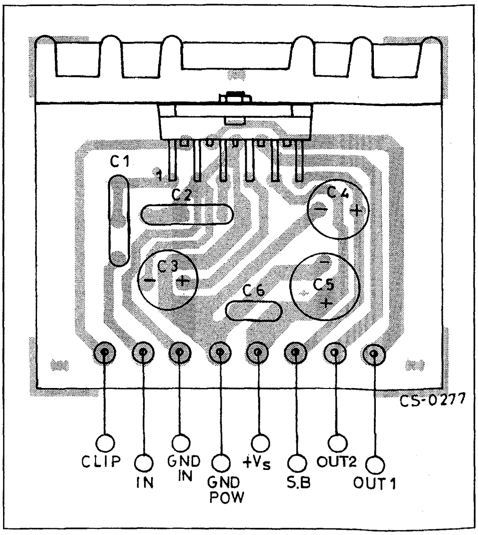


Figure 5: Output Power vs. Supply Voltage (STEREO

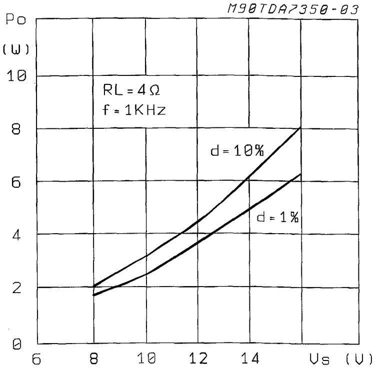


Figure 6: Output Power vs. Supply Voltage (STEREO)

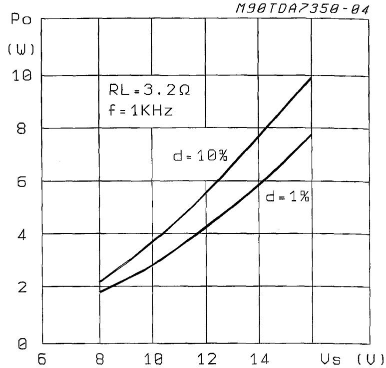


Figure 7: Output Power vs. Supply Voltage (Stereo)

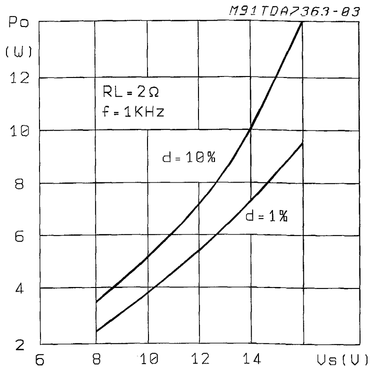


Figure 8: Output Power vs. Supply Voltage (Stereo)

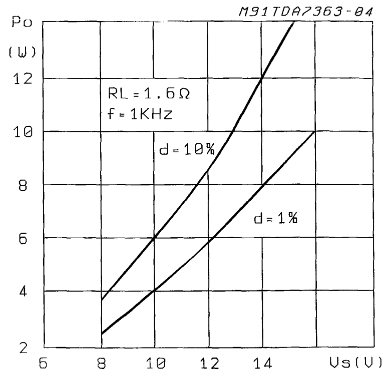


Figure 9: Output Power vs. Supply Voltage (BRIDGE)

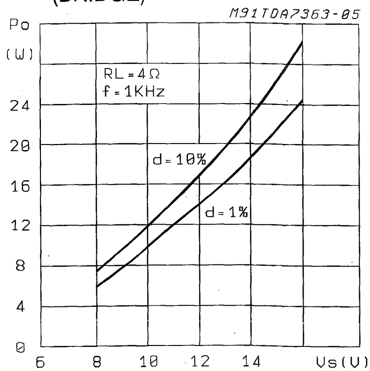


Figure 10: Output Power vs. Supply Voltage (BRIDGE)

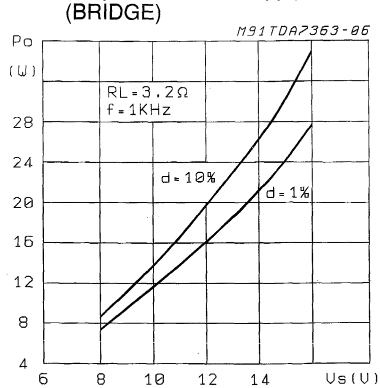


Figure 11: Distortion vs. Output Power (STEREO)

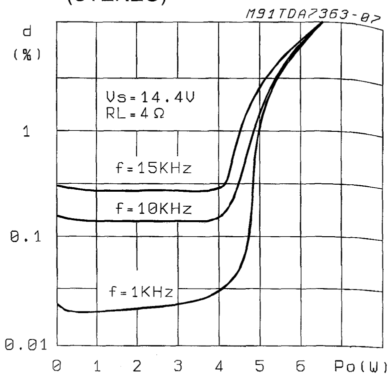


Figure 12: Distortion vs. Output Power (STEREO)

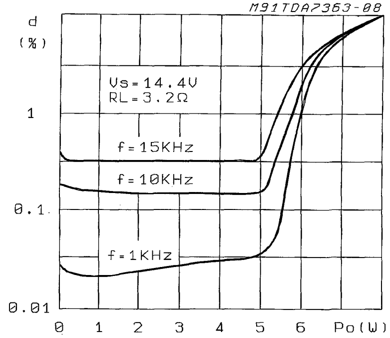


Figure 13: Distortion vs Output Power (BRIDGE)

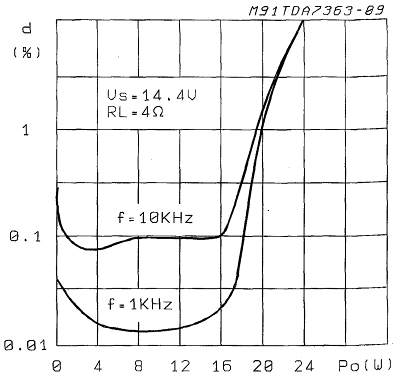


Figure 14: SVR vs. Frequency (STEREO) for Different Values of C3 Capacitor

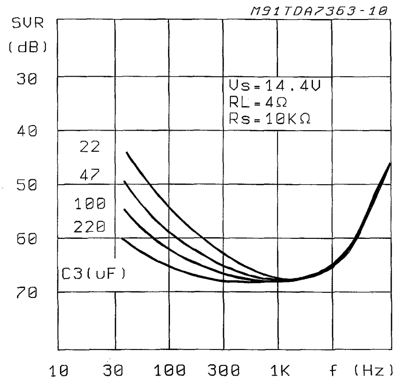


Figure 15: SVR vs. Frequency (BRIDGE) for Different Values of C3 Capacitor

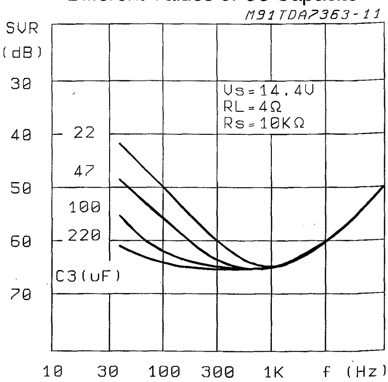


Figure 16: Power Dissipation & Efficiency vs. Output Power (STEREO)

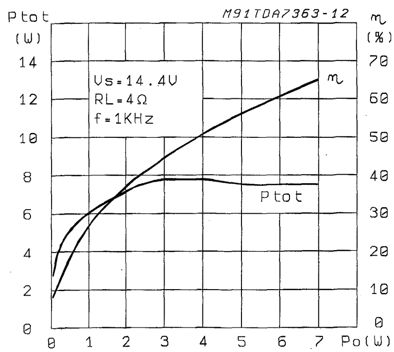


Figure 17: Power Dissipation & Efficiency vs. Output Power (STEREO)

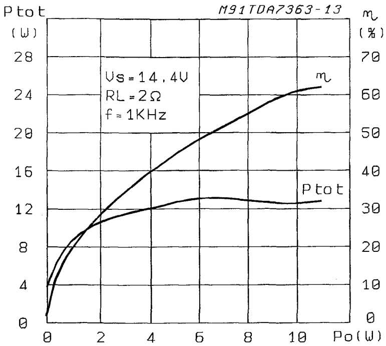


Figure 18: Power Dissipation & Efficiency vs. Output Power (BRIDGE)

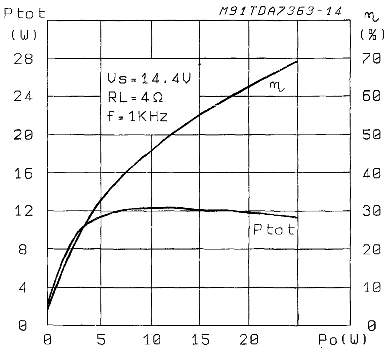
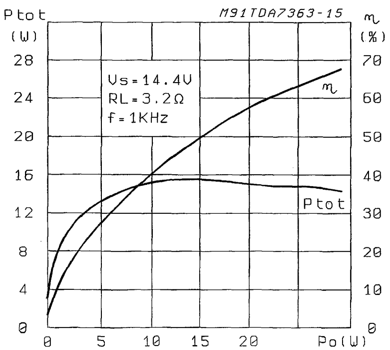


Figure 19: Power Dissipation & Efficiency vs. Output Power (BRIDGE)



AMPLIFIER ORGANIZATION

The TDA7363 has been developed taking care of the key concepts of the modern power audio amplifier for car radio such as: space and costs saving due to the minimized external count, excellent electrical performances, flexibility in use, superior reliability thanks to a built-in array of protections. As a result the following performances has been achieved:

- NO NEED OF BOOTSTRAP CAPACITORS EVEN AT THE HIGHEST OUTPUT POWER LEVELS
- ABSOLUTE STABILITY WITHOUT EXTERNAL COMPENSATION THANKS TO THE INNOVATIVE OUT STAGE CONFIGURATION, ALSO ALLOWING INTERNALLY FIXED CLOSED LOOP LOWER THAN COMPETITORS
- LOW GAIN (20dB STEREO FIXED WITHOUT ANY EXTERNAL COMPONENTS) IN ORDER TO MINIMIZE THE OUTPUT NOISE AND OPTIMIZE SVR
- SILENT MUTE/ST-BY FUNCTION FEATURING ABSENCE OF POP ON/OFF NOISE
- HIGH SVR
- STEREO/BRIDGE OPERATION WITHOUT ADDITION OF EXTERNAL COMPONENT
- AC/DC SHORT CIRCUIT PROTECTION (TO GND, TO V_S, ACROSS THE LOAD)
- LOUDSPEAKER PROTECTION
- DUMP PROTECTION
- ESD PROTECTION

BLOCK DESCRIPTION

Polarization

The device is organized with the gain resistors directly connected to the signal ground pin i.e. without gain capacitors (fig. 20).

The non inverting inputs of the amplifiers are connected to the SVR pin by means of resistor dividers, equal to the feedback networks. This allows the outputs to track the SVR pin which is sufficiently slow to avoid audible turn-on and turn-off transients.

SVR

The voltage ripple on the outputs is equal to the one on SVR pin: with appropriate selection of C_{SVR}, more than 60dB of ripple rejection can be obtained.

Delayed Turn-on (muting)

The C_{SVR} sets a signal turn-on delay too. A circuit is included which mutes the device until the voltage on SVR pin reaches ~2V typ. (fig. 21). The mute function is obtained by duplicating the input differential pair (fig. 22): it can be switched to the signal source or to an internal mute input. This feature is necessary to prevent transients at the inputs reaching the loudspeaker(s) immediately after power-on).

Fig. 21 represents the detailed turn-on transient with reference to the stereo configuration.
At the power-on the output decoupling capacitors are charged through an internal path but the device itself remains switched off (phase 1 of the represented diagram).
When the outputs reach the voltage level of about 1V (this means that there is no presence of short circuits) the device switches on, the SVR capacitor starts charging itself and the output tracks exactly the SVR pin.
During this phase the device is muted until the SVR reaches the "Play" threshold (~2V typ.), after that the music signal starts being played.

Stereo/Bridge Switching
There is also no need for external components for changing from stereo to bridge configuration (figg. 20-23). A simple short circuit between two pins allows phase reversal at one output, yet maintaining the quiescent output voltage.

Stand-by
The device is also equipped with a stand-by function, so that a low current, and hence low cost switch, can be used for turn on/off.

Stability
The device is provided with an internal compensation wich allows to reach low values of closed loop gain.
In this way better performances on S/N ratio and SVR can be obtained.

Figure 20: Block Diagram; Stereo Configuration

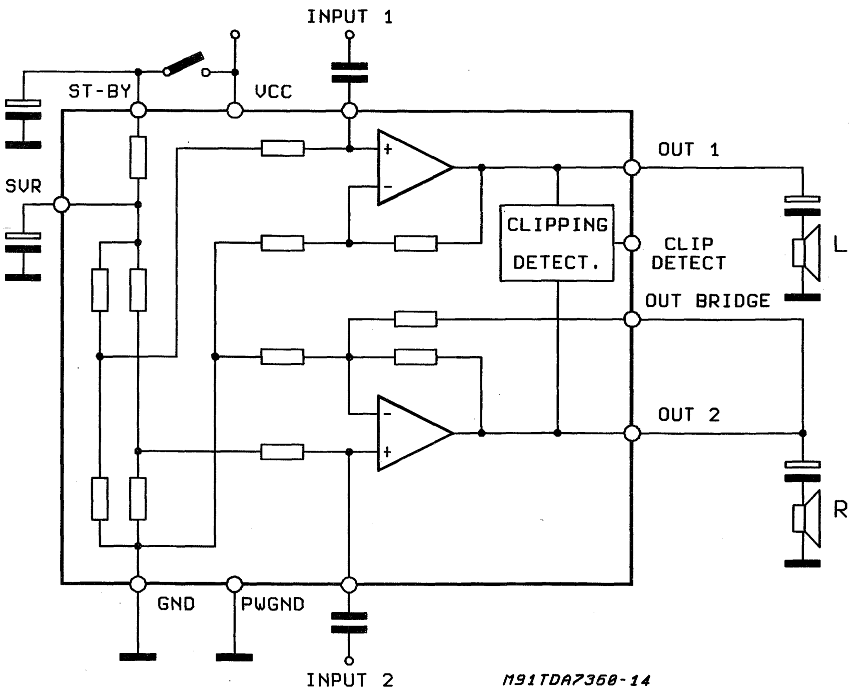


Figure 21: Turn-on Delay Circuit

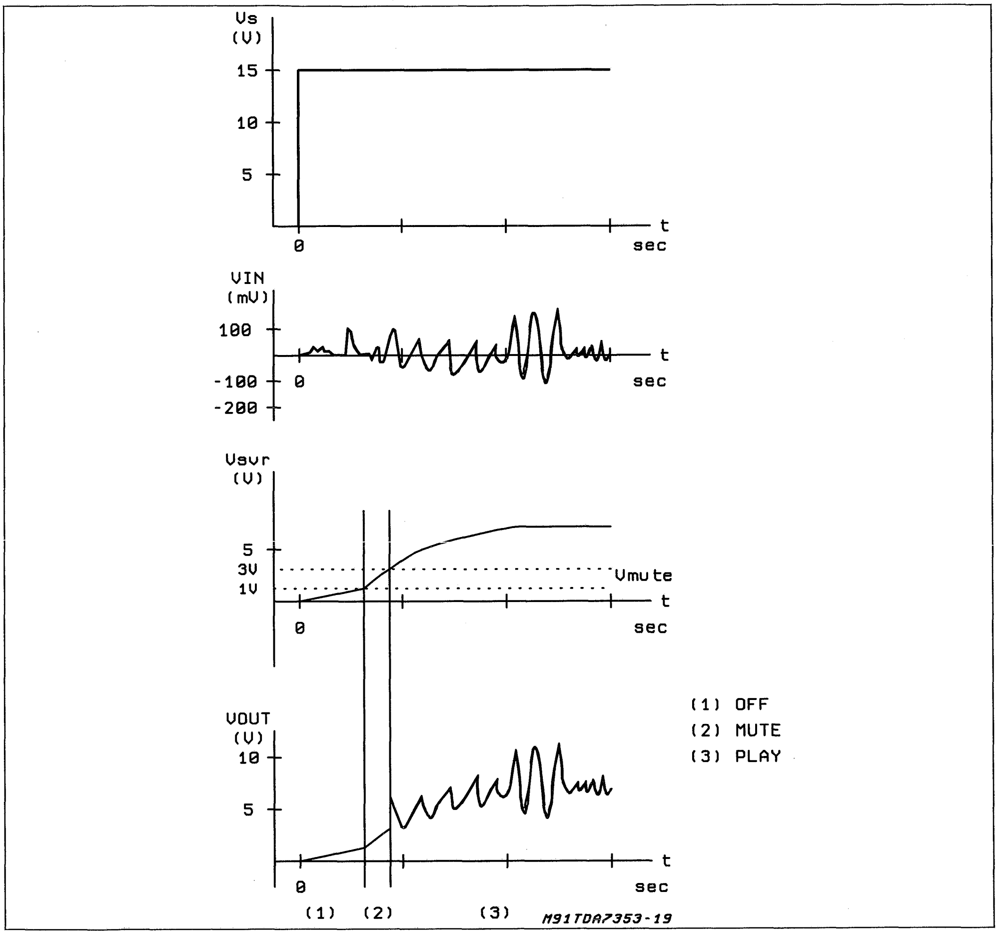


Figure 22: Mute Function Diagram

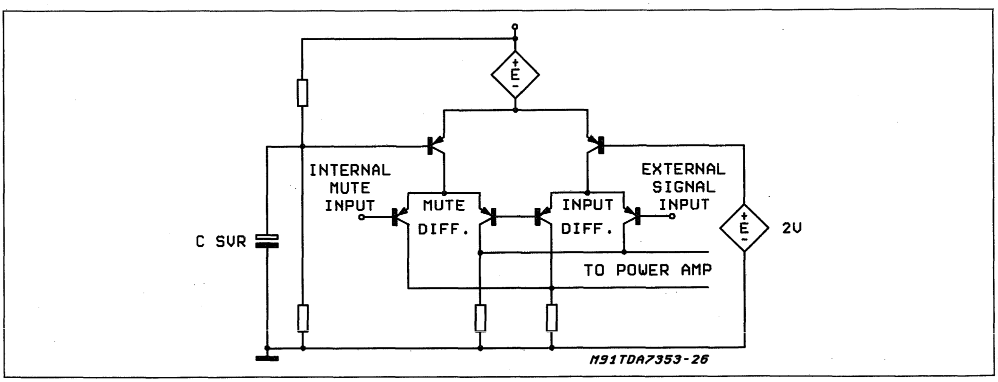
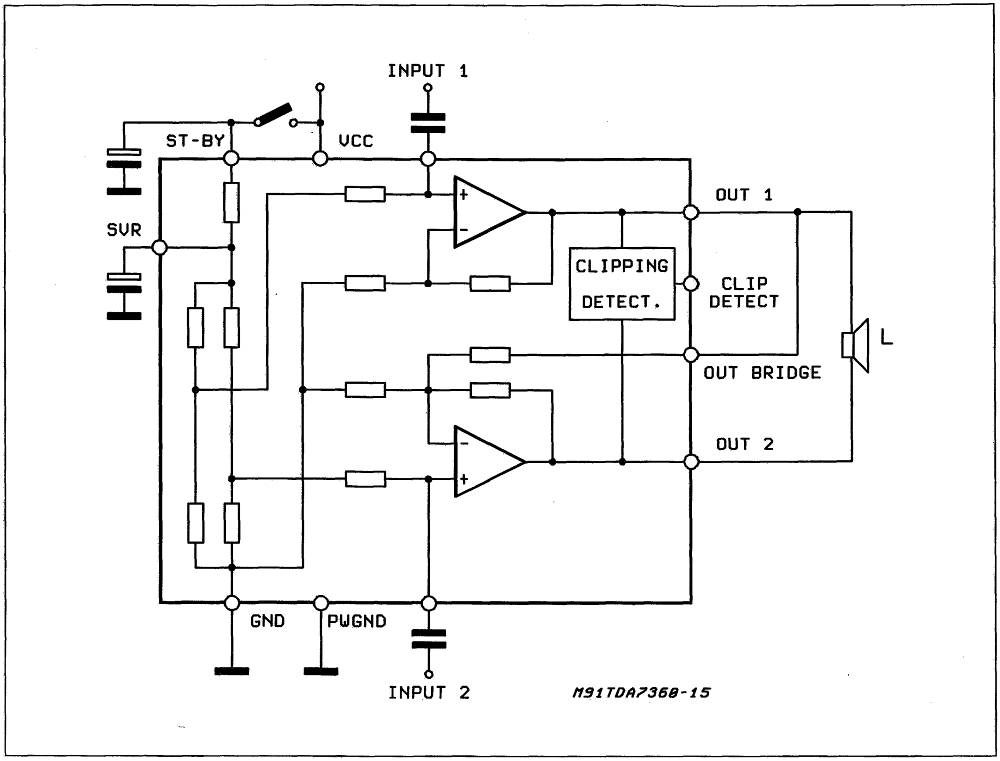


Figure 23: Block Diagram; Bridge Configuration



CLIP DETECTOR

The TDA7363 is equipped with an internal circuit able to detect the output stage saturation providing a proper current sinking into an open collector out. (pin2) when a certain distortion level is reached at each output. This particular function allows compression facility whenever the amplifier is overdriven, so obtaining high quality sound at all listening levels.

Figure 24: Dual Channel Distortion Detector

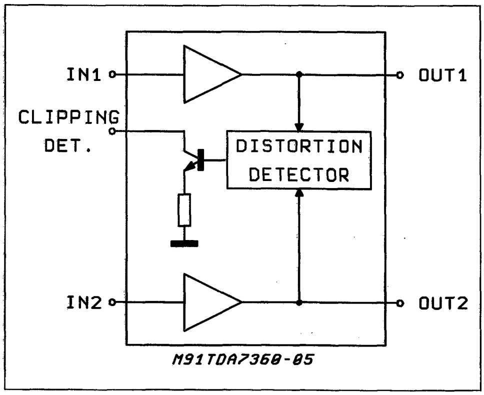


Figure 25: Output at Clipping Detector Pin vs. Signal Distortion

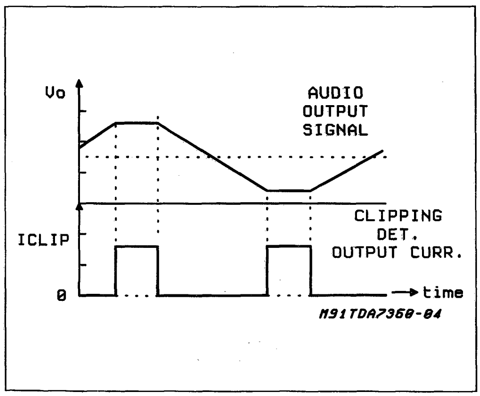


Figure 26: ICV - PNP Gain vs. I_C

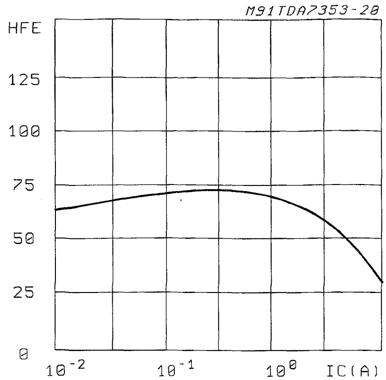


Figure 27: ICV - PNP $V_{CE(sat)}$ vs. I_C

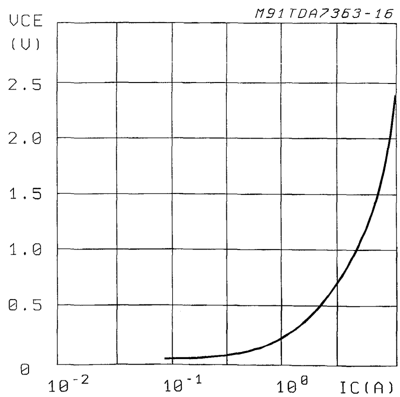
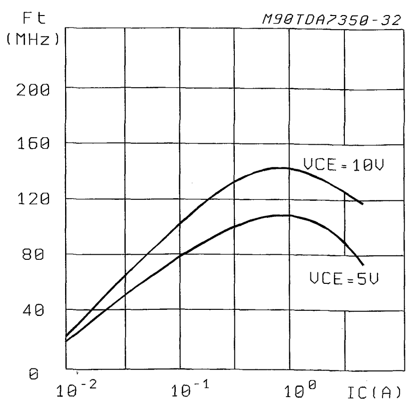


Figure 28: ICV - PNP cut-off frequency vs. I_C

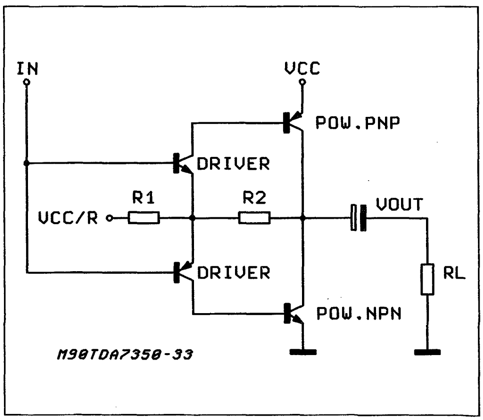


OUTPUT STAGE

Poor current capability and low cutoff frequency are well known limits of the standard lateral PNP. Composite PNP-NPN power output stages have been widely used, regardless their high saturation drop. This drop can be overcome only at the expense of external components, namely, the bootstrap capacitors. The availability of a new 4A isolated collector PNP (ICV PNP) adds versatility to the design. The performance of this component, in terms of gain, V_{CEsat} and cut-off frequency, is shown in fig. 26, 27, 28 respectively. It is realized in a new bipolar technology, characterized by top-bottom isolation techniques, allowing the implementation of low leakage diodes, too. It guarantees BV_{CEO} > 20V and BV_{CBO} > 50V both for NPN and PNP transistors. Basically, the connection shown in fig. 29 has been chosen. First of all because its voltage swing is rail-to-rail, limited only by the VCEsat of the output transistors, which are in the range of 0.3Ω each. Then, the gain VOUT/VIN is greater than unity, approximately 1+R2/R1. (VCC/2 is fixed by an auxiliary amplifier common to both channel). It is possible, controlling the amount of this local feedback, to force the loop gain (A * β) to less than unity at frequencies for which the phase shift is 180°. This means that the output buffer is intrinsically stable and not prone to oscillation.

In contrast, with the circuit of fig. 30, the solution adopted to reduce the gain at high frequencies is the use of an external RC network.

Figure 29: The New Output Stage



AMPLIFIER BLOCK DIAGRAM

The block diagram of each voltage amplifier is shown in fig. 31. Regardless of production spread, the current in each final stage is kept low, with enough margin on the minimum, below which cross-over distortion would appear.

Figure 30: A Classical Output Stage

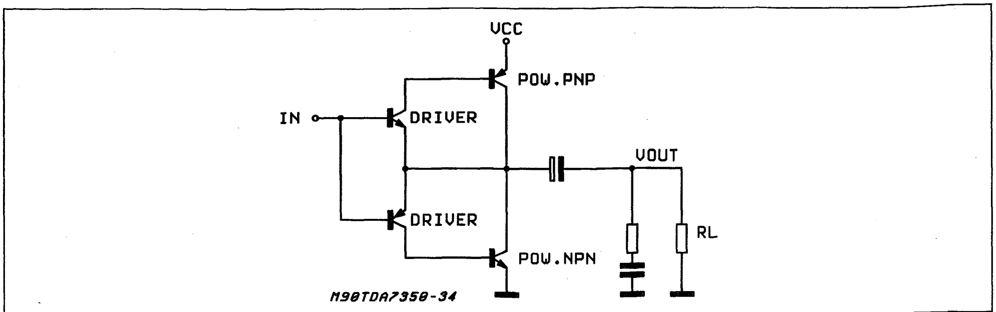
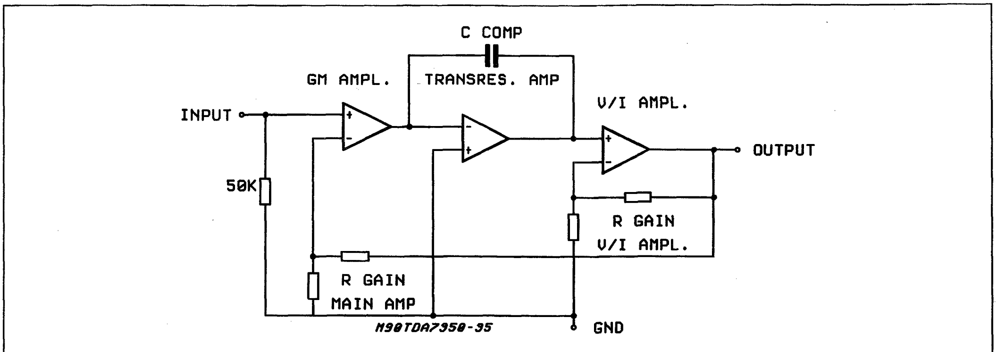


Figure 31: Amplifier Block Diagram



BUILT-IN PROTECTION SYSTEMS

Short Circuit Protection

The maximum current the device can deliver can be calculated by considering the voltage that may be present at the terminals of a car radio amplifier and the minimum load impedance.

Apart from consideration concerning the area of the power transistors it is not difficult to achieve peak currents of this magnitude (5A peak).
However, it becomes more complicated if AC and DC short circuit protection is also required.In particular, with a protection circuit which limits the output current following the SOA curve of the output transistors it is possible that in some conditions (highly reactive loads, for example) the protection circuit may intervene during normal operation. For this reason each amplifier has been equipped with a protection circuit that intervenes when the output current exceeds 4A.

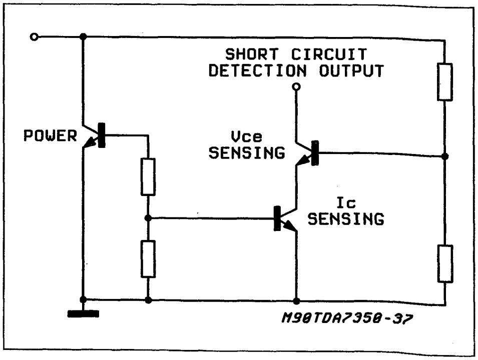
Fig 32 shows the protection circuit for an NPN power transistor (a symmetrical circuit applies to PNP).The VBE of the power is monitored and gives out a signal,available through a cascode.

This cascode is used to avoid the intervention of the short circuit protection when the saturation is below a given limit.

The signal sets a flip-flop which forces the amplifier outputs into a high impedance state.

In case of DC short circuit when the short circuit is removed the flip-flop is reset and restarts the circuit (fig. 36). In case of AC short circuit or load shorted in Bridge configuration, the device is continuously switched in ON/OFF conditions and the current is limited.

Figure 32: Circuitry for Short Circuit Detection



Load Dump Voltage Surge

The TDA 7363 has a circuit which enables it to withstand a voltage pulse train on pin 9, of the type shown in fig. 34.
If the supply voltage peaks to more than 50V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.

A suggested LC network is shown in fig. 33.
With this network, a train of pulses with amplitude up to 120V and width of 2ms can be applied at point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Figure 33

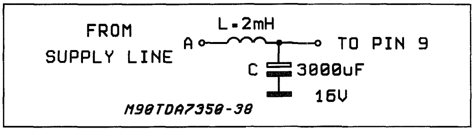
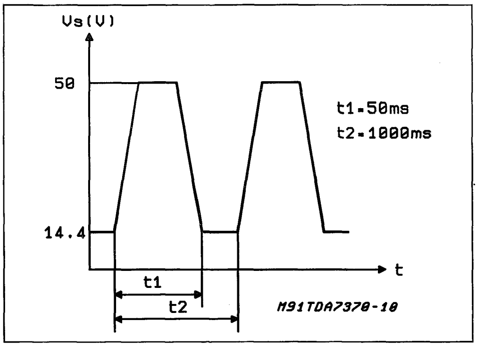


Figure 34



Polarity Inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This features is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open Ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA7363 protection diodes are included to avoid any damage.

DC Voltage

The maximum operating DC voltage for the TDA7363 is 18V.

However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

Thermal Shut-down

The presence of a thermal limiting circuit offers the following advantages:

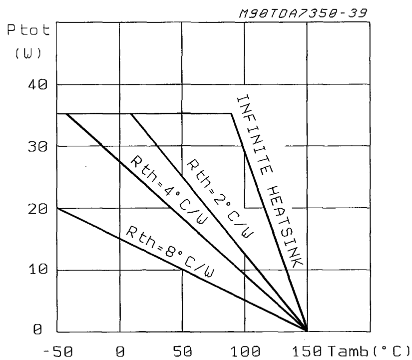
1)an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2)the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 35 shows the dissipable power as a function of ambient temperature for different thermal resistance.

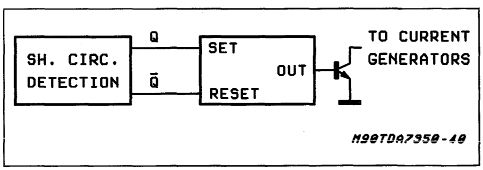
Loudspeaker Protection

Figure 35: Maximum Allowable Power Dissipation vs. Ambient Temperature



The TDA7363 guarantees safe operations even for the loudspeaker in case of accidental shortcircuit. Whenever a single OUT to GND, OUT to V_S short circuit occurs both the outputs are switched OFF so limiting dangerous DC current flowing through the loudspeaker.

Figure 36: Restart Circuit



APPLICATION HINTS

This section explains briefly how to get the best from the TDA7363 and presents some application circuits with suggestions for the value of the components.These values can change depending on the characteristics that the designer of the car radio wants to obtain,or other parts of the car radio that are connected to the audio block.

To optimize the performance of the audio part it is useful (or indispensable) to analyze also the parts outside this block that can have an interconnection with the amplifier.

This method can provide components and system cost saving.

Reducing Turn On-Off Pop

The TDA7363 has been designed in a way that the turn on(off) transients are controlled through the charge(discharge) of the Csvr capacitor.

As a result of it, the turn on(off) transient spectrum contents is limited only to the subsonic range.The following section gives some brief notes to get the best from this design feature(it will refer mainly to the stereo application which appears to be in most cases the more critical from the pop viewpoint.The bridge connection in fact,due to the common mode waveform at the outputs,does not give pop effect).

TURN-ON

Fig 37 shows the output waveform (before and after the "A" weighting filter) compared to the value of Csvr.

Better pop-on performance is obtained with higher Csvr values (the recommended range is from 22uF to 220uF).

The turn-on delay (during which the amplifier is in mute condition) is a function essentially of : C_{out} , C_{svr} .

Being:

$$T1 \approx 120 \cdot C_{out}$$
$$T2 \approx 1200 \cdot C_{svr}$$

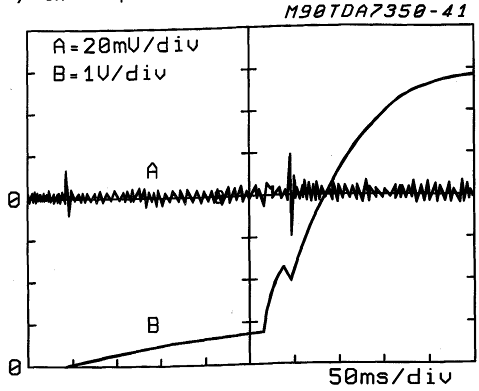
The turn-on delay is given by:

T1+T2 STEREO
T2 BRIDGE

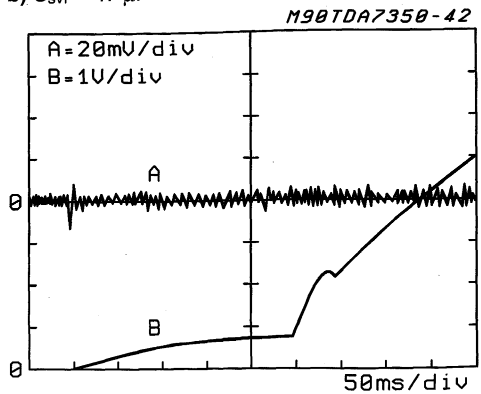
The best performance is obtained by driving the st-by pin with a ramp having a slope slower than 2V/ms

Figure 37:

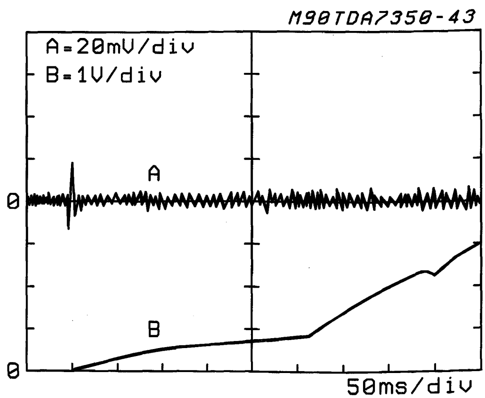
a) C_{svr} = 22 µF



b) C_{svr} = 47 µF



c) C_{svr} = 100 µF



TURN-OFF

A turn-off pop can occur if the st-by pin goes low with a short time constant (this can occur if other car radio sections, preamplifiers,radio.. are supplied through the same st-by switch).
This pop is due to the fast switch-off of the internal current generator of the amplifier.
If the voltage present across the load becomes rapidly zero (due to the fast switch off) a small pop occurs, depending also on Cout,Rload.

The parameters that set the switch off time constant of the st-by pin are:

- the st-by capacitor (Cst-by)
- the SVR capacitor (Csvr)
- resistors connected from st-by pin to ground (Rext)

The time constants is given by :

$T \approx Csvr \bullet 2000\Omega // Rext + Cst\text{-}by \bullet 2500\Omega // Rext$

The suggested time constants are :

$T > 120ms$ with $C_{out}=1000\mu F, R_L = 4ohm$,stereo

$T > 170ms$ with $C_{out}=2200\mu F, R_L = 4ohm$,stereo

If Rext is too low the Csvr can become too high and a different approach may be useful (see next section).

Figg 38, 39 show some types of electronic switches (µP compatible) suitable for supplying the st-by pin (it is important that Qsw is able to saturate with $V_{CE} \leq 150mV$).

Also for turn off pop the bridge configuration is superior, in particular the st-by pin can go low faster.

GLOBAL APPROACH TO SOLVING POP PROBLEM BY USING THE MUTING/TURN ON DELAY FUNCTION

In the real case turn-on and turn-off pop problems are generated not only by the power amplifier,but also (very often) by preamplifiers,tone controls,radios etc. and transmitted by the power amplifier to the loudspeaker.

A simple approach to solving these problems is to use the mute characteristics of the TDA7363.

If the SVR pin is at a voltage below 1V, the mute attenuation (typ)is 30dB .The amplifier is in play mode when Vsvr overcomes 3V.

With the circuit of fig 40 we can mute the amplifier for a time Ton after switch-on and for a time Toff after switch-off.During this period the circuitry that precedes the power amplifier can produce spurious spikes that are not transmitted to the loudspeaker. This can give back a very simple design of this circuitry from the pop point of view.

A timing diagram of this circuit is illustrated in fig 41. Other advantages of this circuit are:

- A reduced time constant allowance of stand-by pin turn off.Consequently it is possible to drive all the car-radio with the signal that drives this pin.

-A better turn-off noise with signal on the output.

To drive two stereo amplifiers with this circuit it is possible to use the circuit of fig 42.

Figure 38

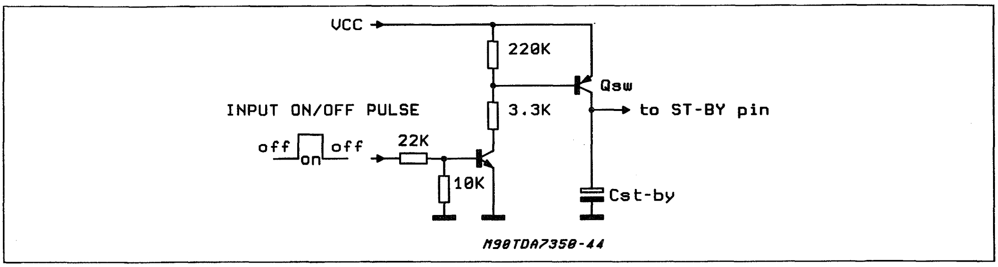


Figure 39

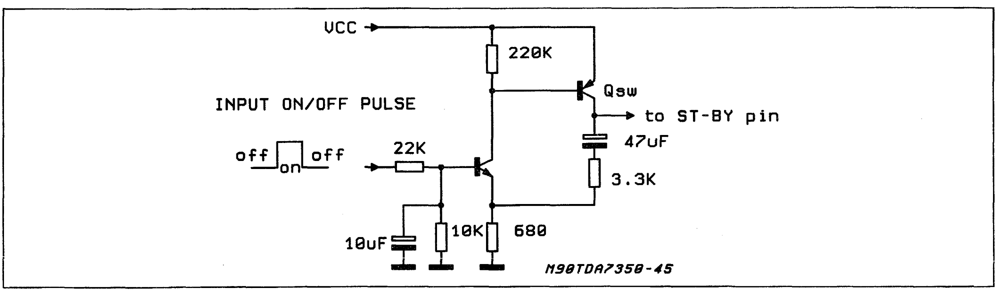


Figure 40

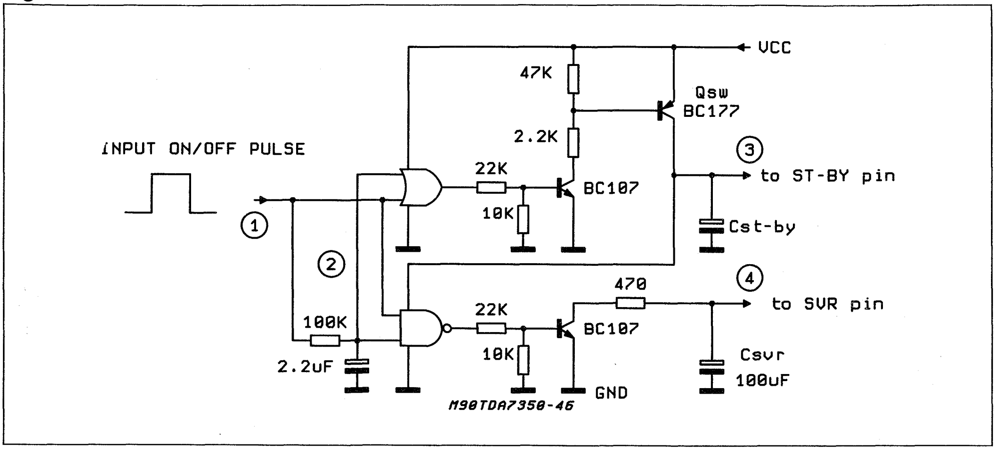


Figure 41

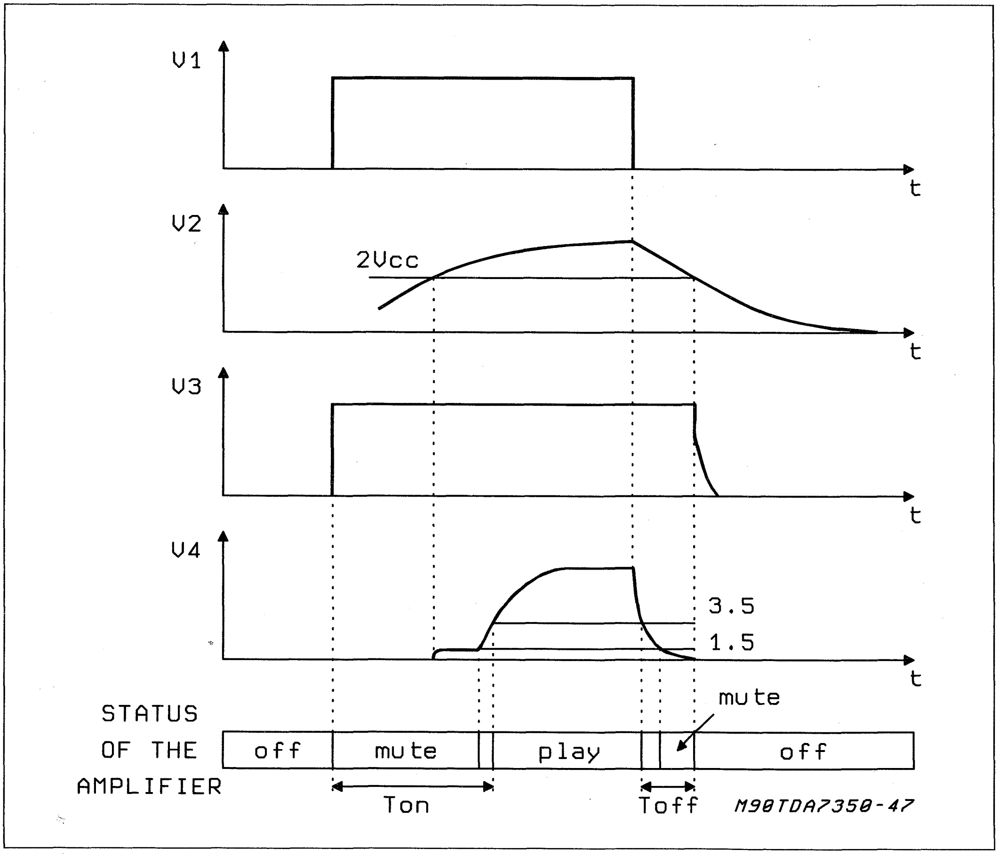
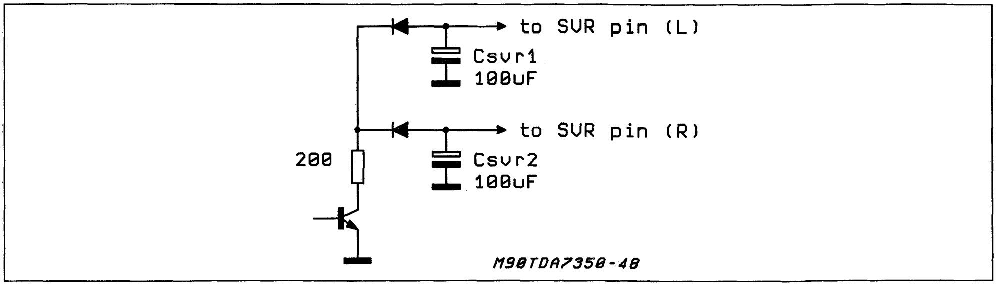


Figure 42



BALANCED INPUT IN BRIDGE CONFIGURATION

A helpful characteristic of the TDA7363 is that,in bridge configuration, a signal present on both the input capacitors is amplified by the same amount and it is present in phase at the outputs,so this signal does not produce effects on the load.The typical value of CMRR is 46 dB.

Looking at fig 43, we can see that a noise signal from the ground of the power amplifier to the ground of the hypothetical preamplifier is amplified of a factor equal to the gain of the amplifier (2 * Gv).

Using a configuration of fig. 44 the same ground noise is present at the output multiplied by the factor 2 * Gv/200.

This means less distortion,less noise (e.g. motor cassette noise) and/or a simplification of the layout of PC board.

The only limitation of this balanced input is the maximum amplitude of common mode signals (few tens of millivolt) to avoid a loss of output power due to the common mode signal on the output, but in a large number of cases this signal is within this range.

Figure 43

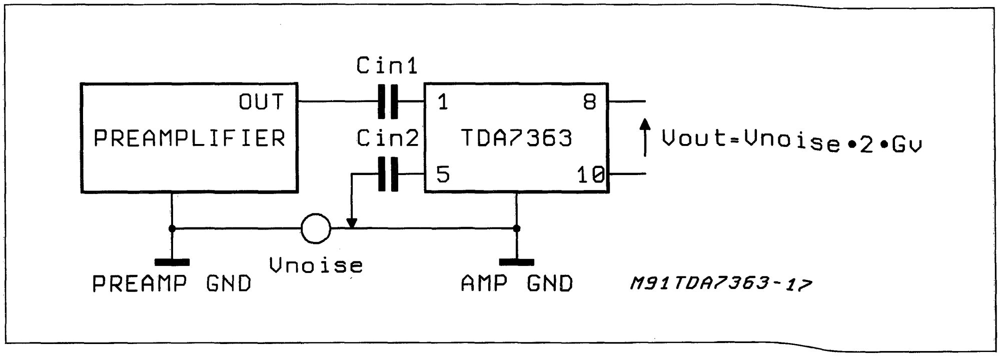
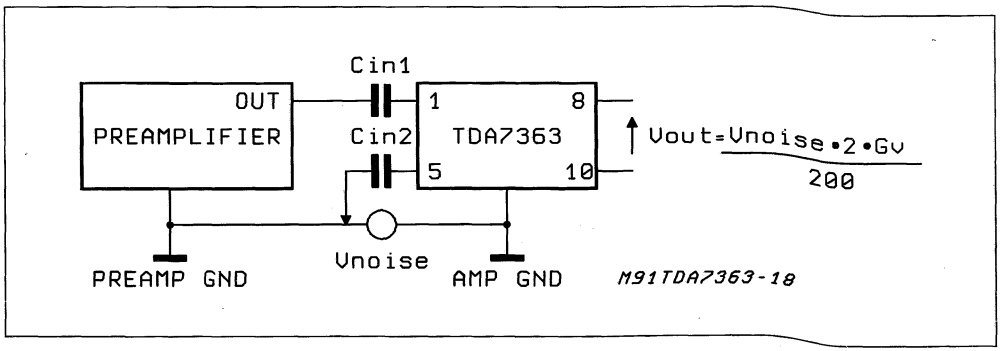


Figure 44



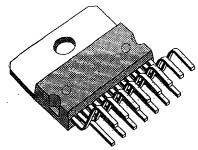
QUAD POWER AMPLIFIER FOR CAR RADIO

ADVANCE DATA

- MINIMUM EXTERNAL COMPONENT COUNT
- HIGH CURRENT CAPABILITY
- NO BOOTSTRAP
- NO BOUCHEROT CELLS
- CLIP DETECTOR OUTPUT
- HIGH OUTPUT POWER
- HIGH APPLICATION FLEXIBILITY
- FIXED GAIN
- VERY LOW STAND-BY CURRENT (1μA typ)
- NO SWITCH ON/OFF NOISE

PROTECTIONS:

- OUTPUT AC/DC SHORT CIRCUIT TO GND AND TO Vs
- VERY INDUCTIVE LOADS
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GND
- REVERSE BATTERY
- ESD



Multiwatt-15

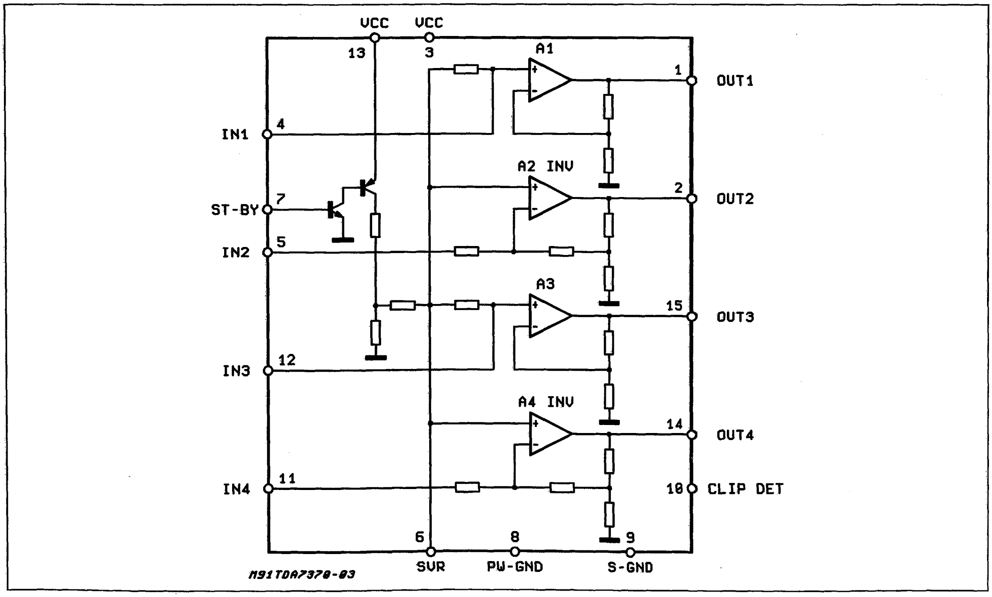
ORDERING NUMBER: TDA7370

DESCRIPTION

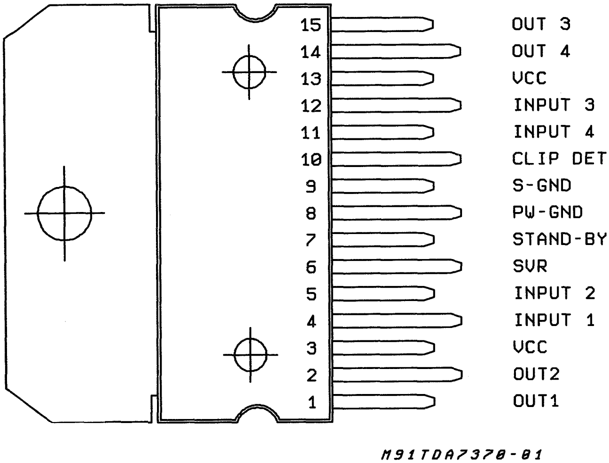
The TDA7370 is a new technology class AB quad channels Audio Power Amplifier in Multiwatt package designed for car radio applications.

Thanks to the fully complementary PNP/NPN output configuration the high power performances of the TDA7370 are obtained without the bootstrap capacitors.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	28	V
V_{OP}	Operating Supply Voltage	18	V
V_{PEAK}	Peak Supply Voltage (t = 50ms)	50	V
I_O	Output Peak Current (not rep. t = 100µs)	4.5	A
I_O	Output Peak Current (rep. f > 10Hz)	3.5	A
P_{tot}	Power Dissipation T_{CASE} = 85°C	36	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

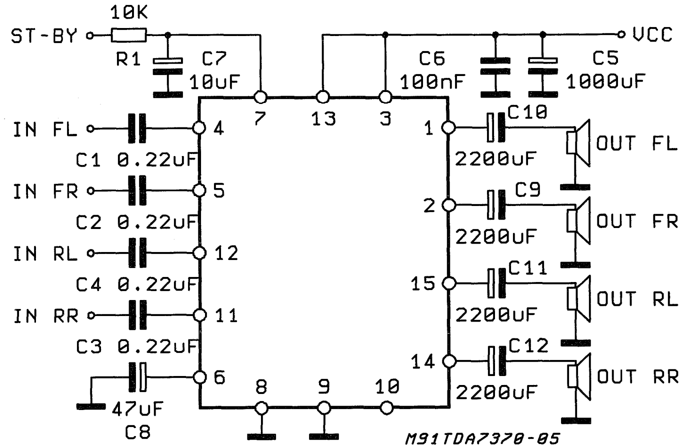
Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; V_S = 14.4V; R_L = 4Ω, T_{amb} = 25°C, f = 1kHz, unless otherwise specified)

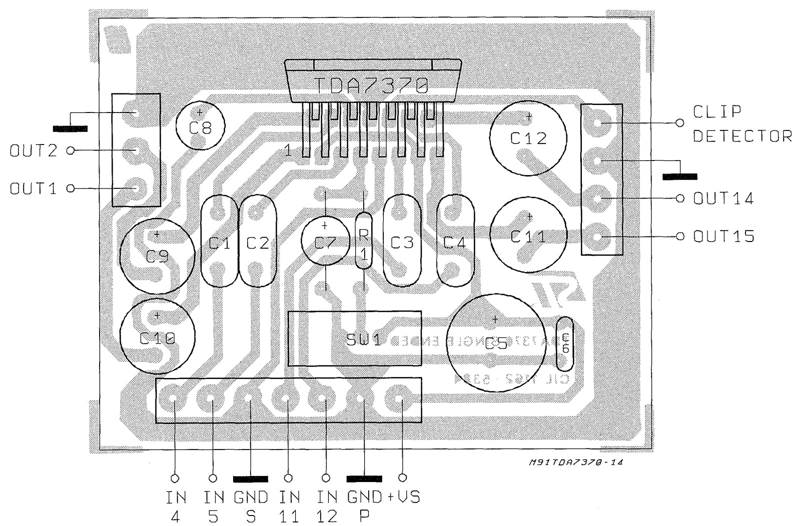
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Range		8		18	V
I_d	Total Quiescent Drain Current	$R_L = \infty$			150	mA
P_O	Output Power	R_L = 4Ω; THD = 10% Single Ended Bridge	 5.5	 6.5 20		 W W
d	Distortion	R_L = 4Ω; Single Ended, P_O = 0.1 to 4W Bridge, P_O = 0.1 to 10W		 0.03	 0.5	 % %
CT	Cross Talk	f = 1kHz Bridge f = 10kHz Bridge f = 1kHz Single Ended f = 10kHz Single Ended		65 55 60 50		dB dB dB dB
R_{IN}	Input Impedance	Single Ended Bridge	20	 15		KΩ KΩ
G_V	Voltage Gain	Single Ended Bridge		20 26		dB dB
G_V	Voltage Gain Match.				1	dB
E_{IN}	Input Noise Voltage (*)	SINGLE ENDED Non Inv. Ch., R_S = 10kΩ Inv. Ch., R_S = 10kΩ BRIDGE (R_S = 0 to 10kΩ)		 3.0 5 3.5		 μV μV μV
SVR	Supply Voltage Rejection	R_S = 0; f = 100Hz to 10kHz		50		dB
ASB	Stand-by Attenuation		60			dB
I_{SB}	ST-BY Current			1		μA
$V_{SB\ ON}$	ST-BY On Threshold Voltage				1.5	V
$V_{SB\ OFF}$	ST-BY Off Threshold Voltage		3.5			V
V_{OS}	Output Offset Voltage				200	mV
$I_{CD\ OFF}$	Clipping Detector "OFF" Output Average Current	THD = 1% (**)		 100		 μA
$I_{CD\ ON}$	Clipping Detector "ON" Output Average Current	THD = 10% (**)		 190		 μA

(*) Weighted A
(**) Pin 10 Pulled-up to 5V with 10kΩ;

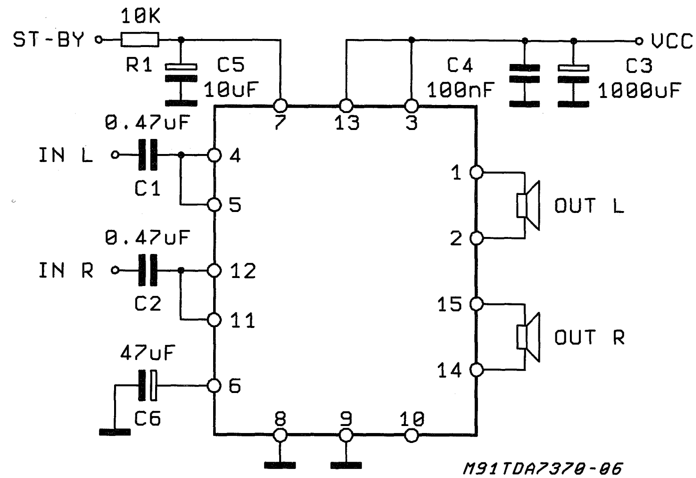
APPLICATION CIRCUIT (QUAD STEREO)



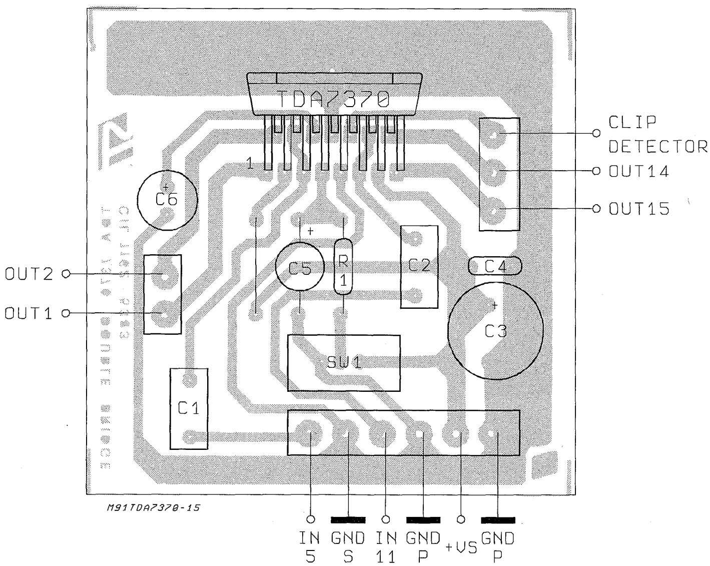
QUAD STEREO P.C. BOARD AND COMPONENT LAYOUT (1:1 SCALE)



APPLICATION CIRCUIT (DOUBLE BRIDGE)



DOUBLE BRIDGE P.C. BOARD AND COMPONENT LAYOUT (1:1 SCALE)



APPLICATION CIRCUIT (STEREO/BRIDGE)

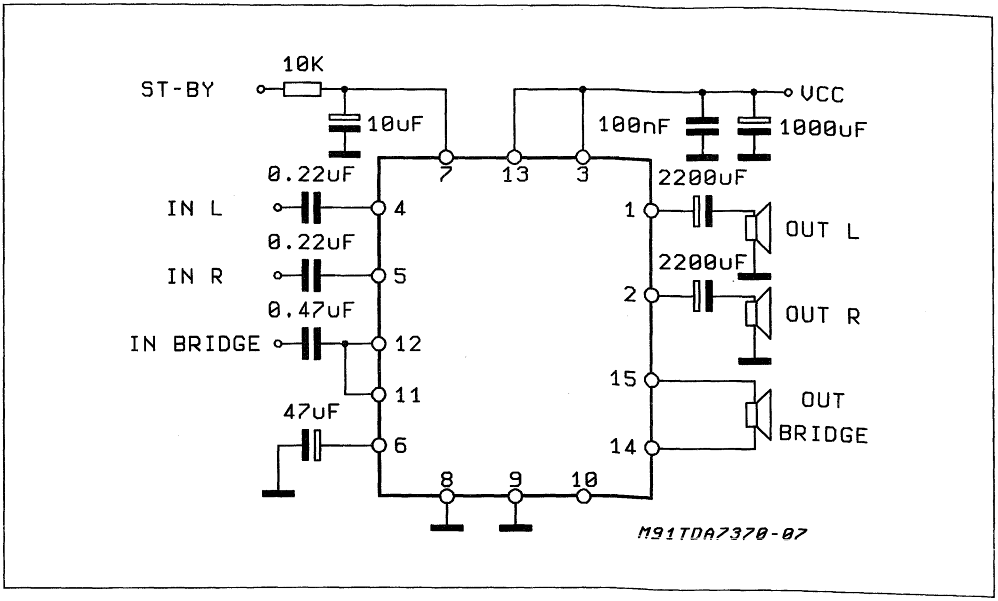


Figure 1: Quiescent Drain Current vs. Supply Voltage (Bridge/Single Ended)

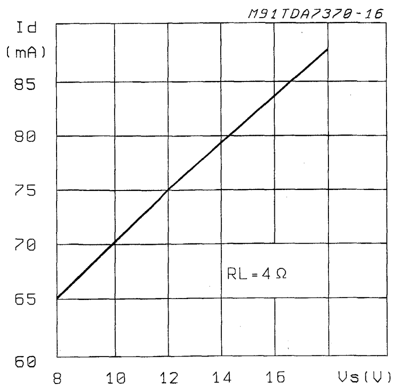


Figure 2: Quiescent Output Voltage vs. Supply Voltage (Bridge/Single Ended)

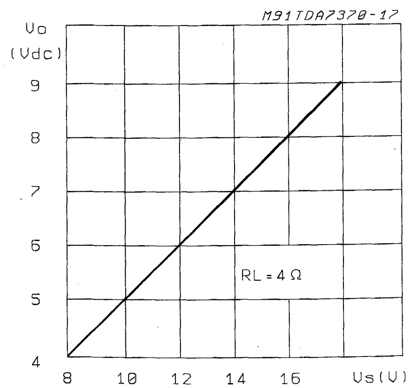


Figure 3: Output Power vs. Supply Voltage (Single Ended)

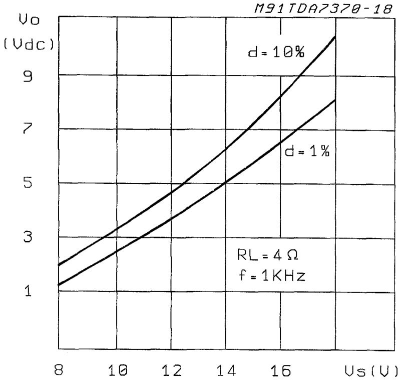


Figure 4: Output Power vs. Supply Voltage (Bridge)

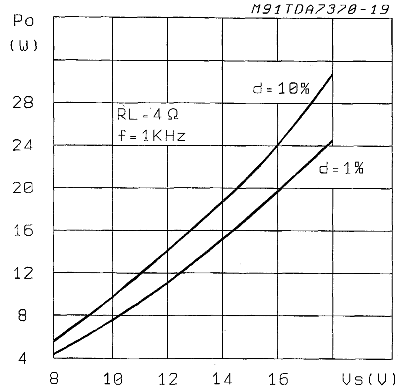


Figure 5: Distortion vs. Output Power (Single Ended)

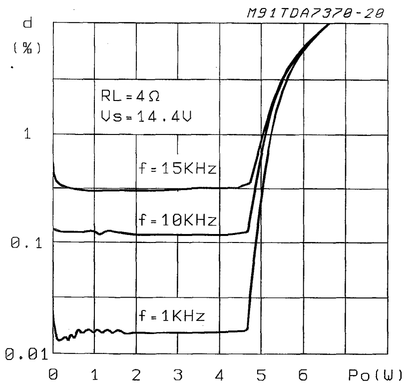


Figure 6: Distortion vs. Output Power (Bridge)

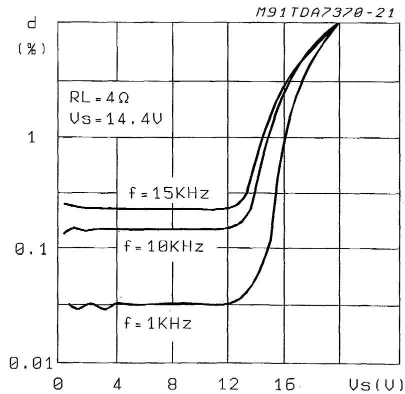


Figure 7: Output Power vs. Frequency (Single Ended)

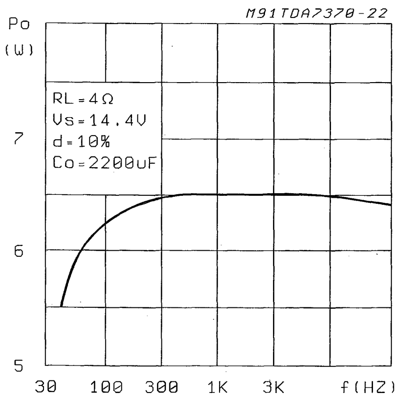


Figure 8: Output Power vs. Frequency (Bridge)

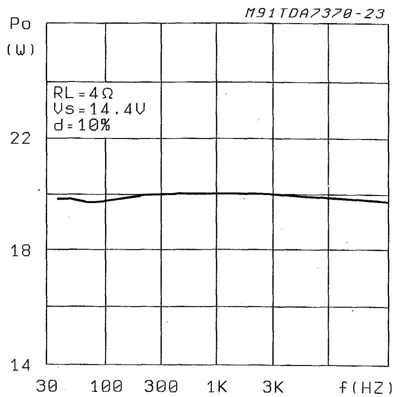


Figure 9: Supply Voltage Rejection vs. Frequency (Single Ended) for different values of pin 6 capacitor.

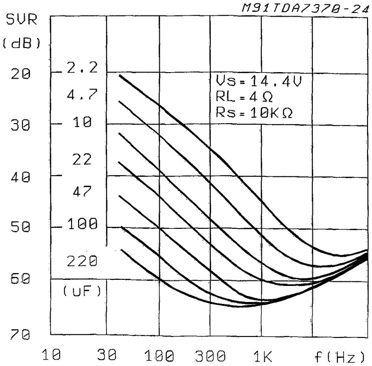


Figure 10: Supply Voltage Rejection vs. Frequency (Bridge) for different values of pin 6 capacitor.

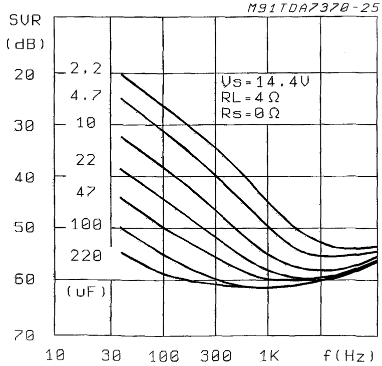


Figure 11: Cross-Talk vs. Frequency (Bridge)

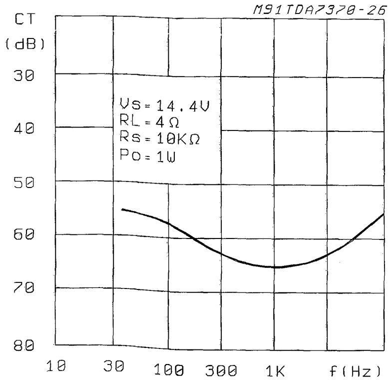


Figure 12: Stand-By Attenuation vs. Threshold Voltage (Single Ended/Bridge)

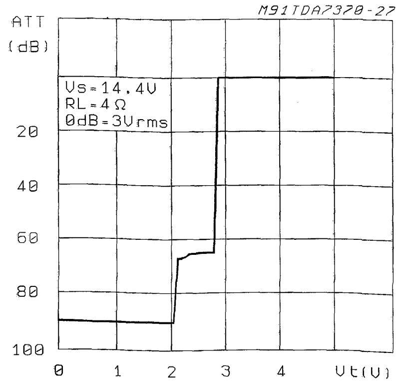


Figure 13: Clipping Detector Average Current (pin 10) vs.Distortion (Single Ended)

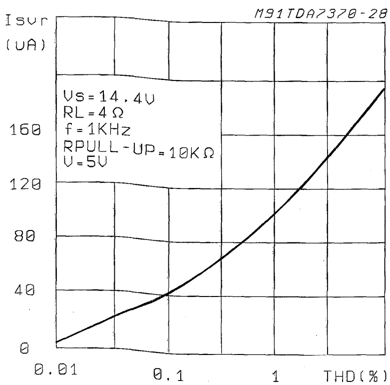


Figure 14: En input vs. Rs (Single Ended)

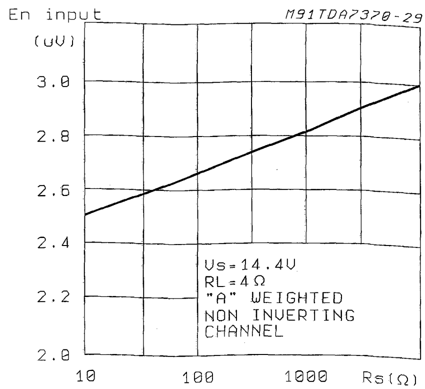


Figure 15: En input vs. Rs (Single Ended)

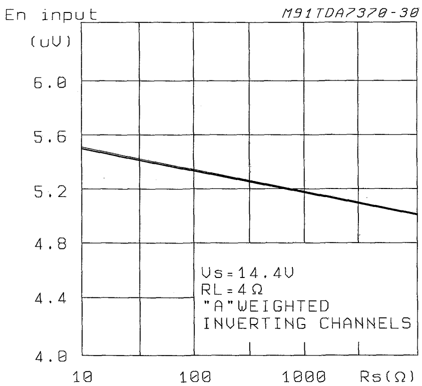


Figure 16: En input vs. Rs (Bridge)

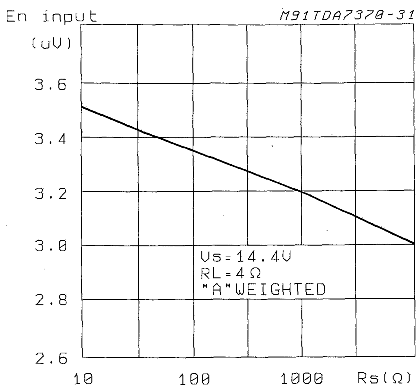


Figure 17: Total Power Dissipation and Efficiency vs. Ouput Power (Single Ended)

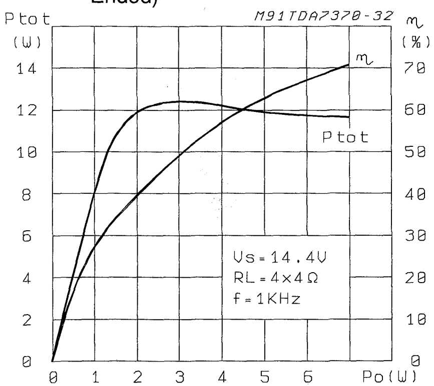
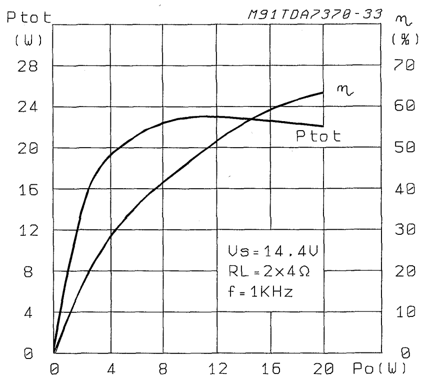


Figure 18: Total Power Dissipation and Efficiency vs. Ouput Power (Bridge)

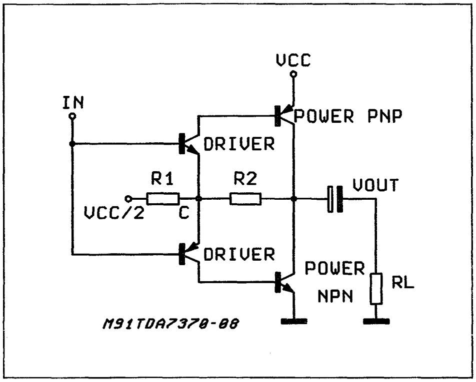


OUTPUT STAGE

The fully complementary output stage was made possible by the development of a new component: the ST exclusive power ICV PNP.

A novel design based upon the connection shown in fig. 19 has then allowed the full exploitation of its possibilities.

Figure 19: The new Output Stage



The clear advantages this new approach has over classical output stages are as follows:

1 - Rail-to-Rail Output Voltage Swing With No Need Of Bootstrap Capacitors.

The output swing is limited only by the Vcesat of the output transistors, which are in the range of 0.6 Ohm (R_{sat}) each.

Classical solutions adopting composite PNP-NPN for the upper output stage have higher saturation loss on the top side of the waveform. This unbalanced saturation causes a significant power reduction. The only way to recover power consists of the addition of expensive bootstrap capacitors.

2 - Absolute Stability Without Any External Compensation.

Referring to the circuit of Fig. 19 the gain V_{OUT}/V_{IN} is greater than unity, approximately 1 + R2/R1. The DC output ($V_{CC}/2$) is fixed by an auxiliary amplifier common to all the channels).

By controlling the amount of this local feedback it is possible to force the loop gain (A * β) to less than unity at frequency for which the phase shift is 180 Deg. This means that the output buffer is intrinsically stable and not prone to oscillation.

Most remarkably, the above feature has been achieved in spite of the very low closed loop gain of the amplifier (20 dB).

In contrast, with the classical PNP-NPN stage, the solution adopted for reducing the gain at high frequencies makes use of external RC networks, namely the Boucherot cells.

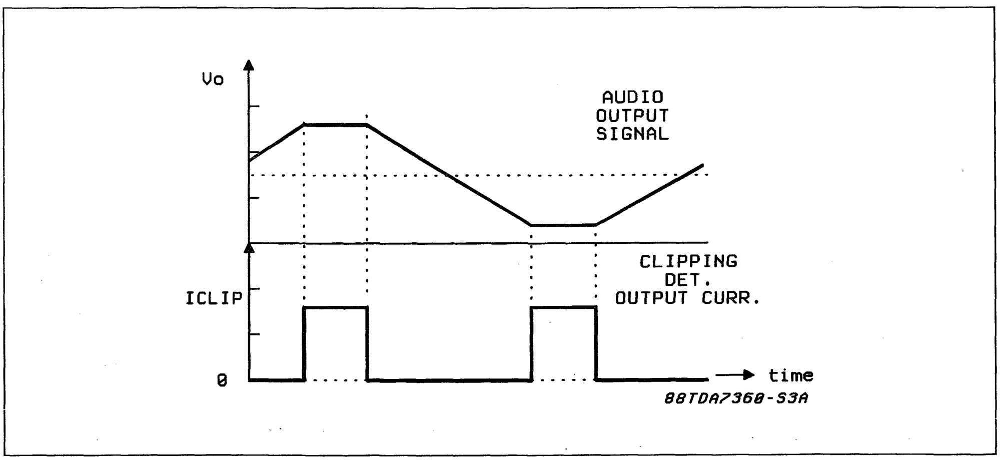
OTHER OUTSTANDING CHARACTERISTICS:

Clipping Detector Output

The TDA7370 is equipped with an internal circuit able to detect the output stage saturation providing a current sinking into a open collector output (pin 10) when a certain distortion level is reached at each output.

This particular function allows gain compression facility whenever the amplifier is overdriven, thus obtaining high quality sound at all listening levels.

Figure 20: Clipping Detection Waveforms



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The quiescent output voltage must be as close as possible to its nominal value, so that less undistorted power would be available.

For this reason an input bias current compensation is implemented to reduce the voltage drop across the input resistors, which appears amplified at the outputs.

Gain Internally Fixed to 20dB in Single Ended, 26dB in Bridge

Advantages of this design choice are in terms of:

- components and space saving
- output noise, supply voltage rejection and distortion optimization.

Silent Turn On/Off and Muting/Stand-by Function

The stand-by can be easily activated by means of a CMOS level applied to pin 7 through a RC filter. Under stand-by condition the device is turned off completely (supply current= 1 µA TYP ; output attenuation= 90 dB TYP).

Every ON/OFF operation is virtually pop free.

Furthermore, at turn-on the device stays in muting condition for a time determined by the value assigned to the SVR capacitor (T= Csvr * 7,000). While in muting the device outputs becomes insensitive to any kinds of signal that may be present at the input terminals. In other words every transient coming from previous stages produces no unpleasant acoustic effect to the speakers.

Another situation under which the device is totally muted is whenever the supply voltage drops lower than 7V. This is helpful to pop suppression during the turn-off by battery switch.

Easy Single Ended to Bridge Transition.

The change from single ended to bridge configurations is made simply by means of a short circuit across the inputs, that is no need of further external components.

High Application Flexibility

The availability of 4 independent channels makes it possible to accomplish several kinds of applications ranging from 4 speakers stereo (F/R) to 2 speakers bridge solutions.
In case of working in single ended conditions the polarity of the speakers driven by the inverting amplifier must be reversed respect to those driven by non inverting channels.
This is to avoid phase inconveniences causing sound alterations especially during the reproduction of low frequencies.

BUILT-IN PROTECTION SYSTEMS

Full Protection of Device and Loudspeakers Against AC/DC Short Circuits (to Gnd, to Vs, across the Speakers).

Reliable and safe operation in presence of all kinds of short circuit involving the outputs is assured by a built-in protection system that operates in the following way:

In case of overload, a SCR is activated as soon as the current flowing through the output transistors overcomes a preset threshold value depending on the chip temperature. The SCR causes an interruption of the supply current of the power transistor. The normal working is restored by a restart circuit going into action as soon as the short circuit is removed.

Load Dump Voltage Surge

The TDA 7370 has a circuit which enables it to withstand a voltage pulse train on pins 3 and 13, of the type shown in fig. 22.
If the supply voltage peaks to more than 50V, then an LC filter must be inserted between the supply and pins 3 and 13, in order to assure that the pulses at pins 3 and 13 will be held within the limits shown.

A suggested LC network is shown in fig. 21.
With this network, a train of pulses with amplitude up to 120V and width of 2ms can be applied at point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Figure 21

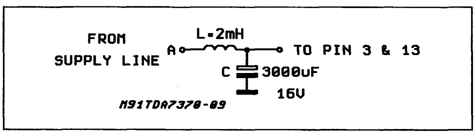
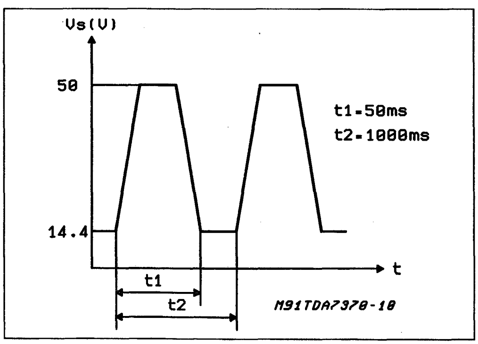


Figure 22



Polarity Inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This features is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open Ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA7370 protection diodes are included to avoid any damage.

Inductive Load

A protection diode is provided to allow use of the TDA7370 with inductive loads.

DC Voltage

The maximum operating DC voltage for the TDA7370 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

Thermal Shut-down

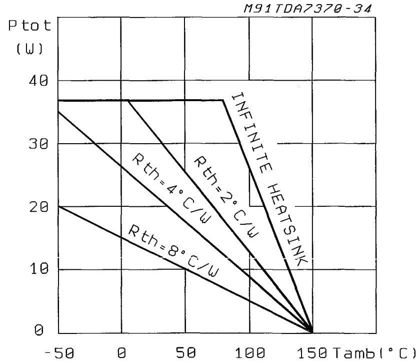
The presence of a thermal limiting circuit offers the following advantages:

1)an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2)the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in case of excessive junction temperature: all happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 23 shows the dissipable power as a function of ambient temperature for different thermal resistance.

Figure 23: Maximum Allowable Power Dissipation vs. Ambient Temperature



Loudspeaker Protection

The TDA7370 guarantees safe operations even for the loudspeaker in case of accidental shortcircuit. Whenever a single OUT to GND, OUT to V_S short circuit occurs both the outputs are switched OFF so limiting dangerous DC current flowing through the loudspeaker.

CLIPPING DETECTOR

Figures 25 and 26 show an application using the TDA7370 in combination with the SGS-THOMSON audioprocessor TDA7302.

The output clipping is recognized by the microprocessor (in this application it is simulated by a PC).

The detailed way to operate of the system is represented by the flow-chart of fig.24

The controller detects when the clipping is active (minimun detection width fixed by a C29 = 12 nF external capacitor), and reduces the volume (or bass) by steps of 2 dB (with a programmable waiting time), until no more clipping is detected.

Then the controller waits for a programmable time before increasing the volume again by step of 2 dB until clipping is again detected or the panel selected volume is reached.

Practical advantages of this application is a better sound quality deriving from operation under no clipping conditions, which also means the availability of higher undistorted power.

WHAT IS NEEDED FOR A DEMONSTRATION

- a XT or AT IBM compatible PC, supplied with EGA card
- a SGS-THOMSON audioprocessor application disk
- a TDA 7302 + TDA7370 board
- a connector from audioprocessor board to PC parallel port

GENERAL INFORMATION

In the application shown in figures 25 and 26 the TDA7302 audioprocessor works on PC XT or AT IBM compatible.

Control is accomplished by serial bus (S-bus or I^2C-bus or SPI bus) sent to the test board through the PC parallel port.

The PC simulates the behaviour of the microprocessor in a real application (for example in a car radio) and the buffer is necessary only in this application for protecting the PC.

Figure 24: Clipping Detector Control Routine

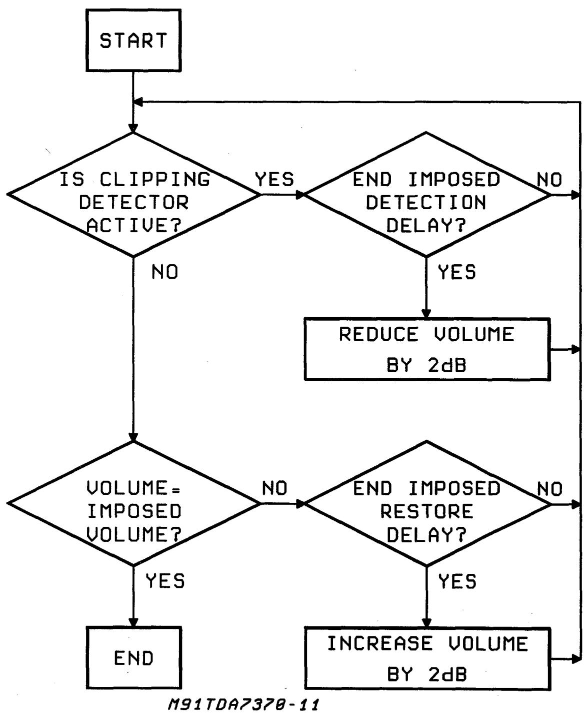


Figure 25: Application with TDA7302 + TDA7370 (QUAD STEREO)

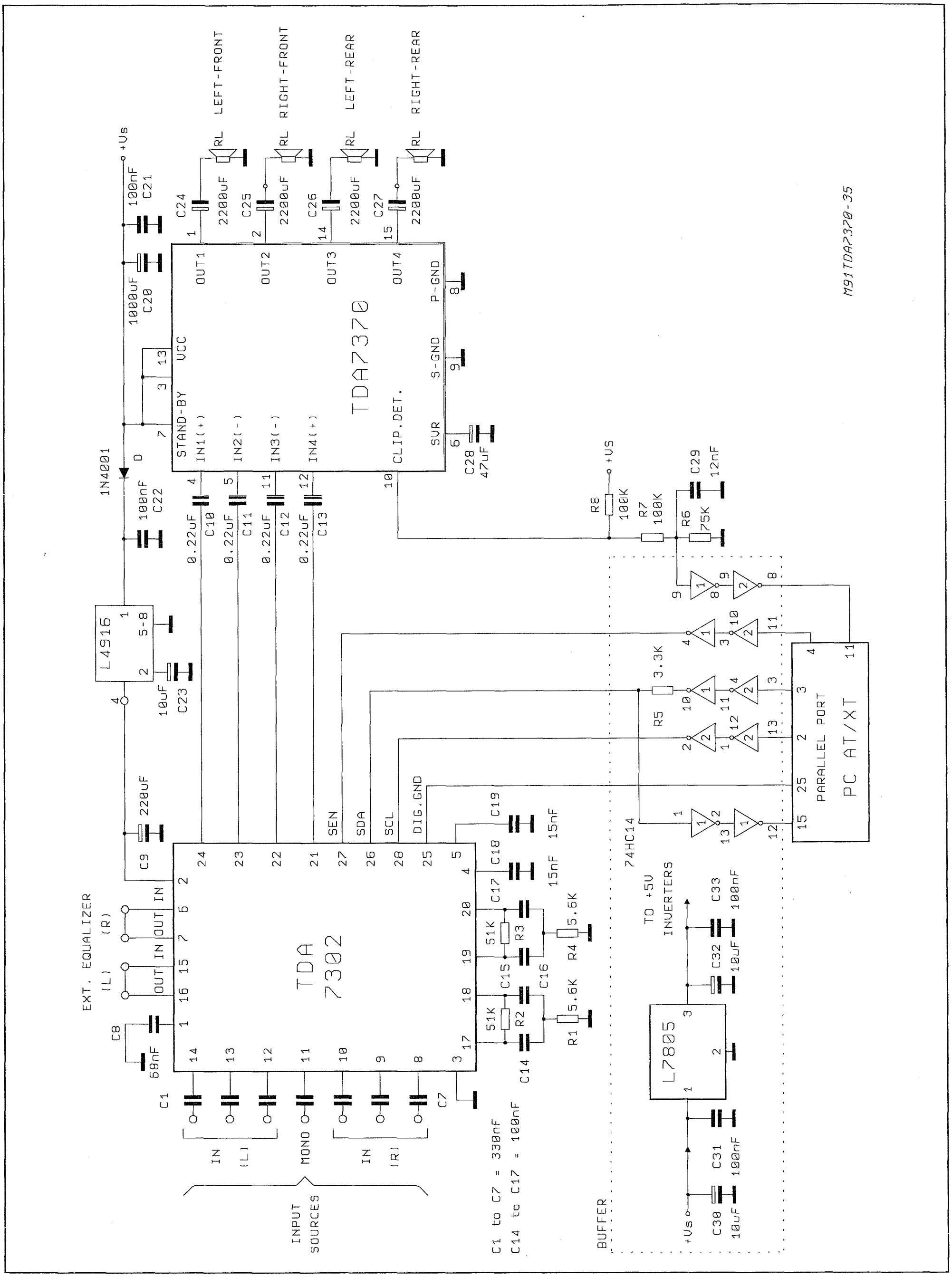
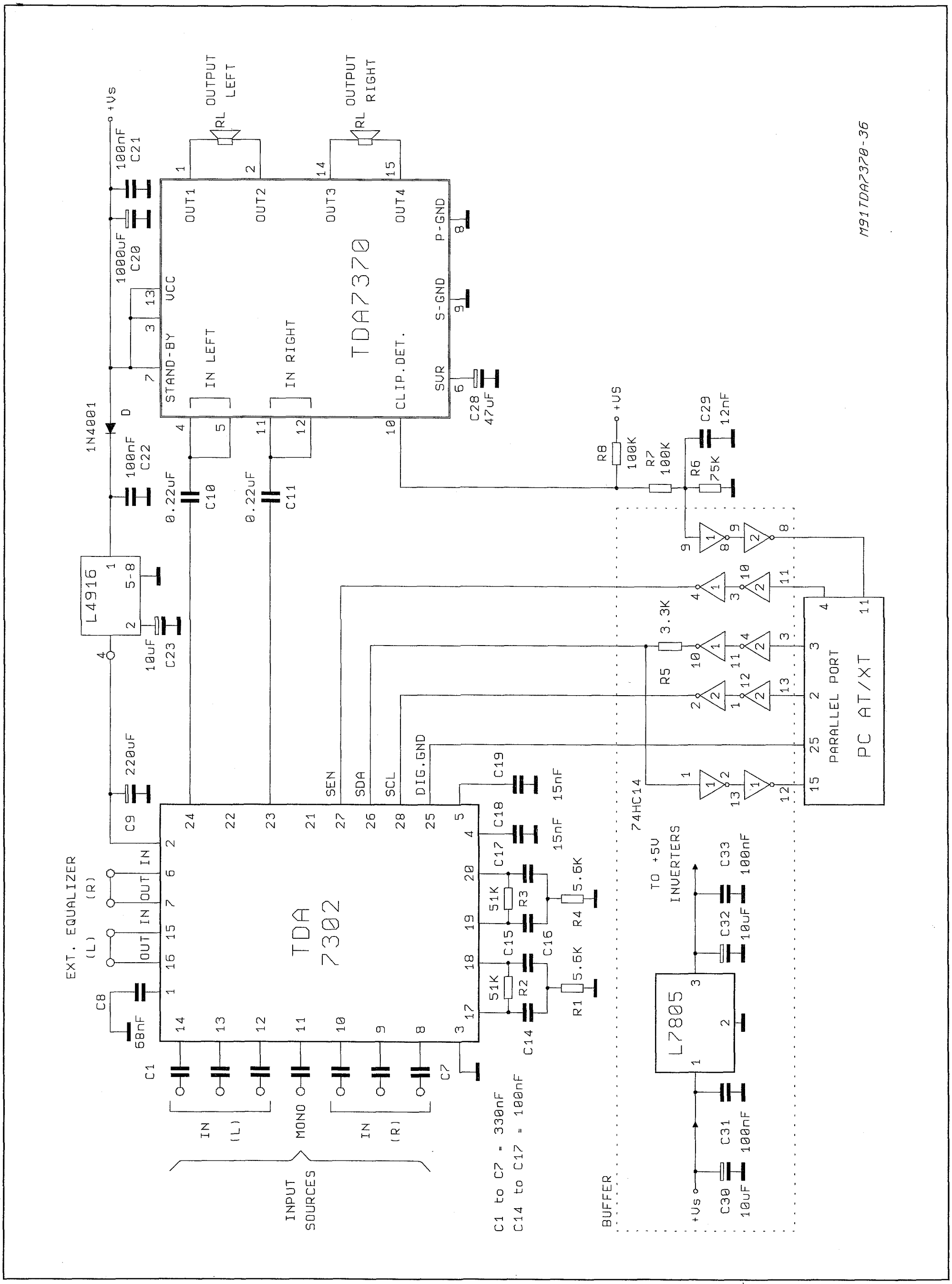


Figure 26: Application wiyh TDA7302 + TDA7370 (DOUBLE BRIDGE)



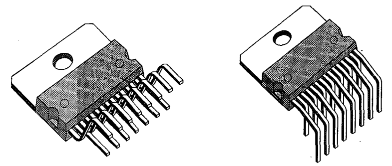
DUAL BRIDGE AUDIO AMPLIFIER FOR CAR RADIO

ADVANCE DATA

- MINIMUM EXTERNAL COMPONENT COUNT
- NO BOOTSTRAP CAPACITORS
- NO BOUCHEROT CELLS
- CLIP DETECTOR OUTPUT
- HIGH OUTPUT POWER
- FIXED GAIN
- VERY LOW STAND-BY CURRENT (1μA typ)
- NO SWITCH ON/OFF NOISE

PROTECTIONS:

- OUTPUT AC/DC SHORT CIRCUIT TO GND AND TO V_S
- VERY INDUCTIVE LOADS
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GND
- REVERSE BATTERY
- ESD



Multiwatt15 V **Multiwatt15 H**

ORDERING NUMBERS:

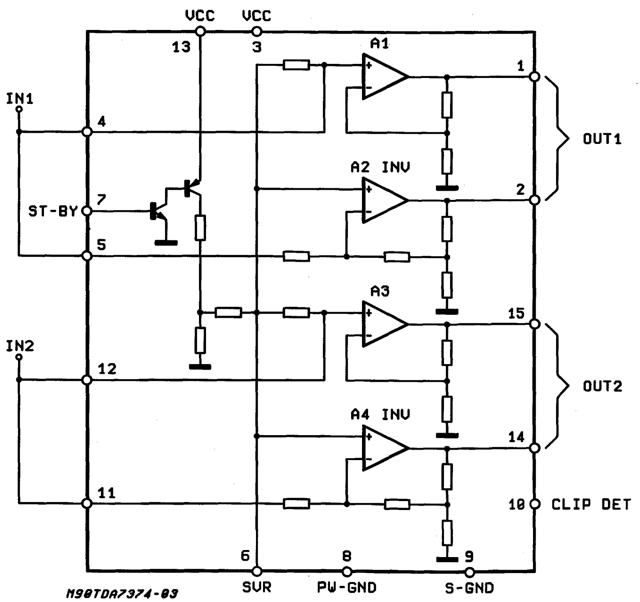
TDA7374V TDA7374H

DESCRIPTION

The TDA7374 is a new technology class AB Audio Dual Bridge Power Amplifier in Multiwatt package designed for car radio applications.

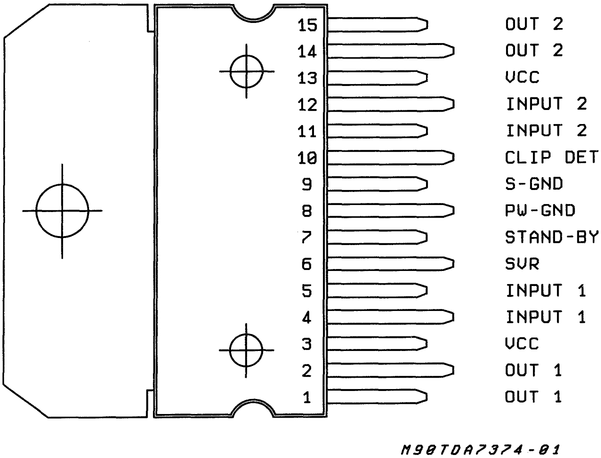
Thanks to the fully complementary PNP/NPN output configuration the high power performances of the TDA7374 are obtained without the bootstrap capacitors.

TEST AND APPLICATION CIRCUIT



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice. notice.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	28	V
V_{OP}	Operating Supply Voltage	18	V
V_{PEAK}	Peak Supply Voltage (t = 50ms)	50	V
I_O	Output Peak Current (not rep. t = 100µs)	4.5	A
I_O	Output Peak Current (rep. f > 10Hz)	3.5	A
P_{tot}	Power Dissipation T_{CASE} = 85°C	36	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

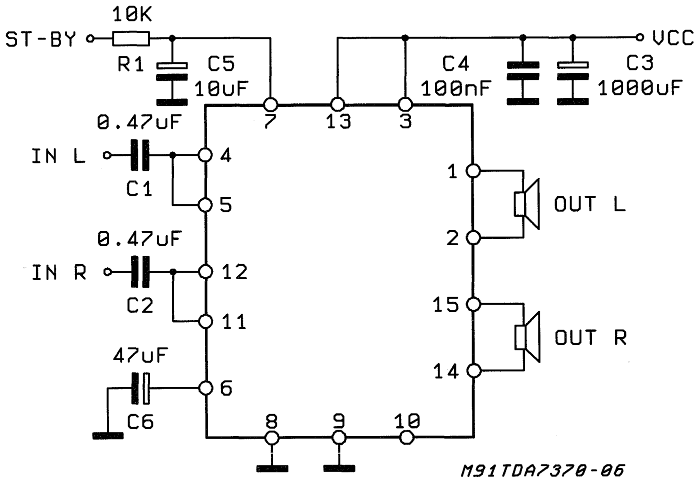
Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; V_S = 14.4V; R_L = 4Ω, T_{amb} = 25°C, f = 1kHz, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Range		8		18	V
I_d	Total Quiescent Drain Current	$R_L = \infty$			150	mA
P_O	Output Power	R_L = 4Ω; THD = 10%	17	21		W
d	Distortion	R_L = 4Ω P_O = 0.1 to 10W			0.5	%
CT	Cross-Talk	f = 1kHz f = 10kHz		65 55		dB dB
R_{IN}	Input Impedance		10			KΩ
G_V	Voltage Gain			26		dB
G_V	Voltage Gain Match.				1	dB
E_{IN}	Input Noise Voltage	R_S = 0 to 10kΩ Weight A 22Hz to 22KHz		3.5	 10	μV μV
SVR	Supply Voltage Rejection	R_S = 0; f = 100Hz f = 10kHz	48	 55		dB
ASB	Stand-by Attenuation		60			dB
I_{SB}	ST-BY Current			1		μA
$V_{SB\ ON}$	ST-BY On Threshold Voltage				1.5	V
$V_{SB\ OFF}$	ST-BY Off Threshold Voltage		3.5			V
V_{OS}	Output Offset Voltage				200	mV
$I_{CD\ OFF}$	Clipping Detector "OFF" Output Average Current	THD = 1% (*)		100		μA
$I_{CD\ ON}$	Clipping Detector "ON" Output Average Current	THD = 10% (*)		190		μA

(*) Pin 10 Pulled-up to 5V with 10kΩ; R_L = 4Ω

TEST AND APPLICATION CIRCUIT



P.C. BOARD AND COMPONENT LAYOUT (1:1 scale)

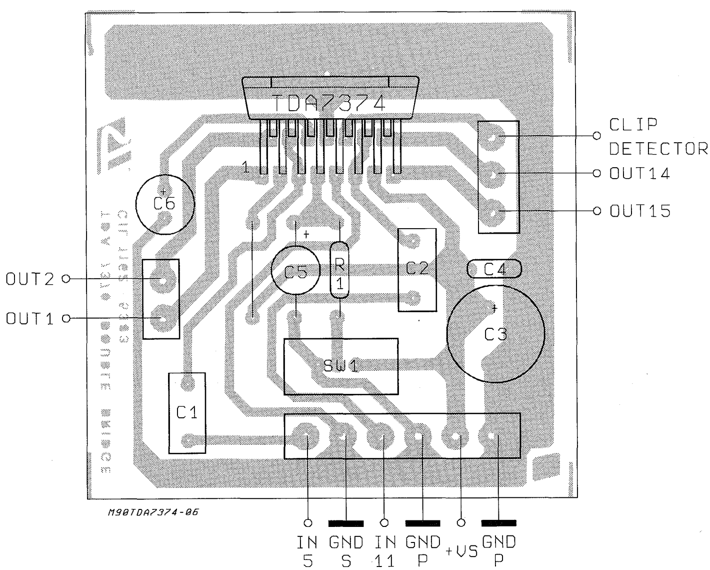


Figure 1: Quiescent Drain Current vs. Supply Voltage

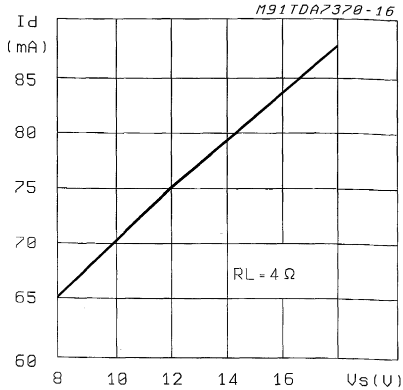


Figure 2: Quiescent Output Voltage vs. Supply Voltage

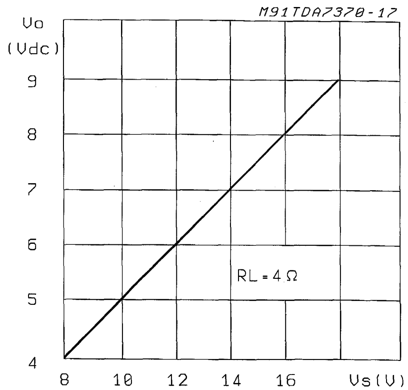


Figure 3: Output Power vs. Supply Voltage

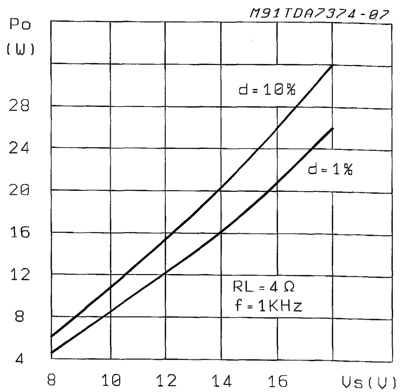


Figure 4: Distortion vs. Output Power

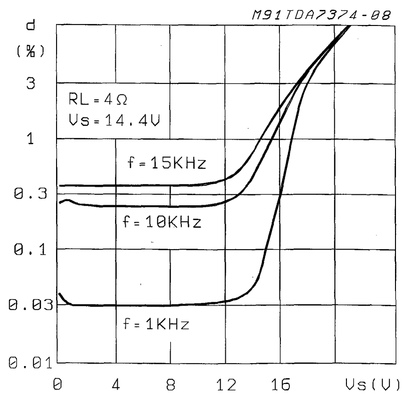


Figure 5: Output Power vs. Frequency

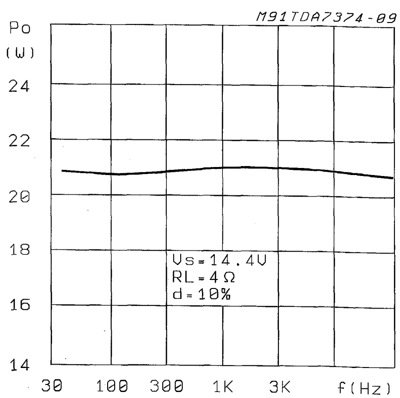


Figure 6: Supply Voltage Rejection vs. Frequency for a Different values of C6 Capacitor

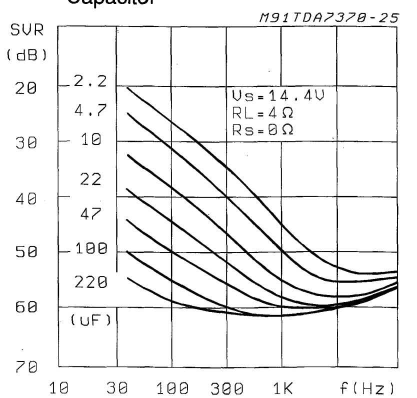


Figure 7: Cross-Talk vs. Frequency

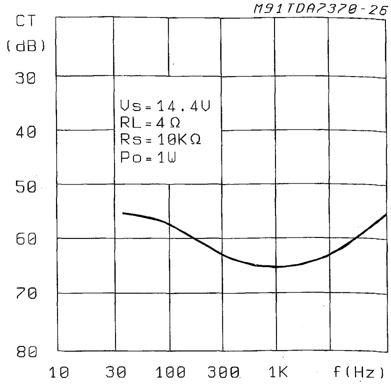


Figure 8: En Input vs. Rg

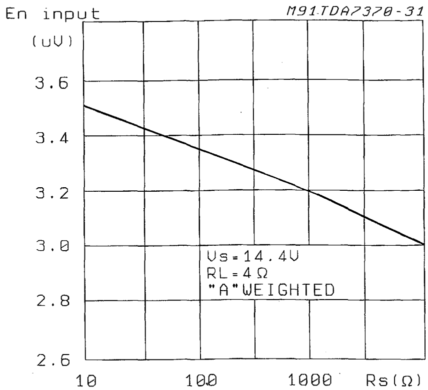


Figure 9: Stand-by Attenuation vs. Threshold Voltage

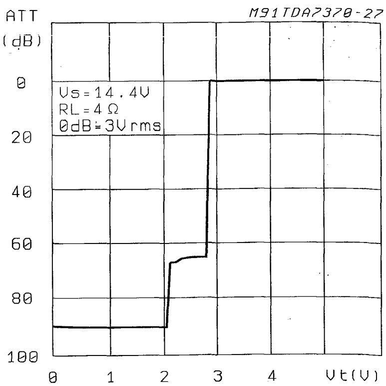


Figure 10: Stand-by Attenuation vs. Input Voltage

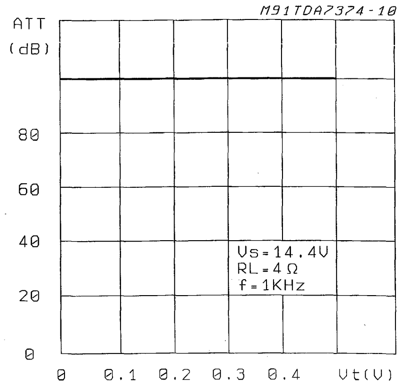


Figure 11: Clipping Detector Average Current (Pin 10) vs. Distortion

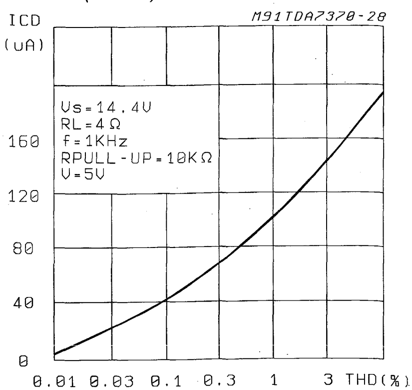
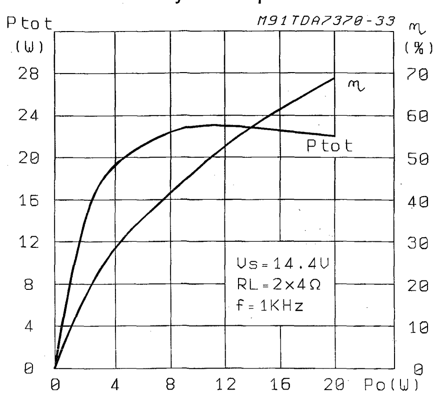


Figure 12: Total Power Dissipation and Efficiency vs. Output Power



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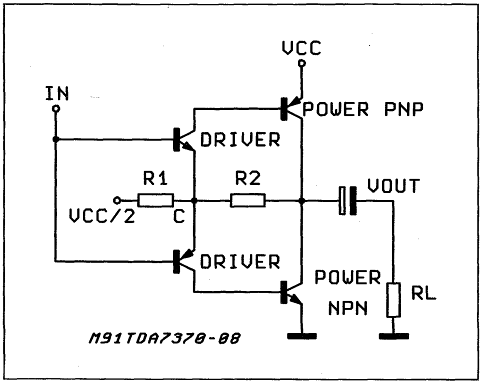

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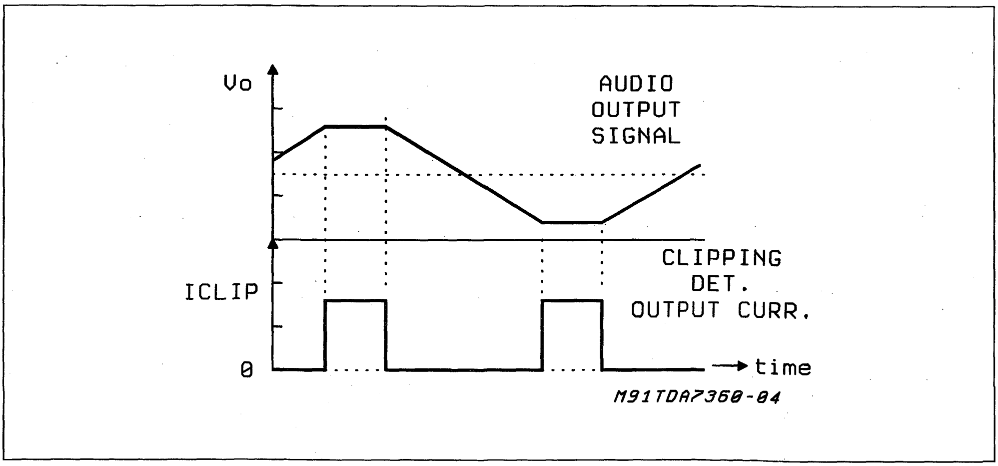

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Figure 15

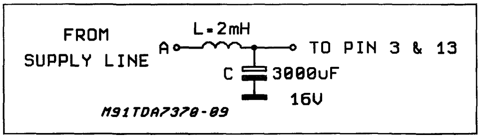
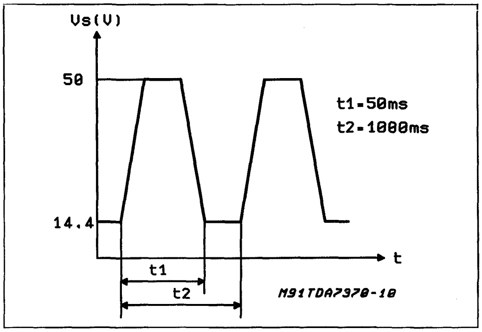


Figure 16



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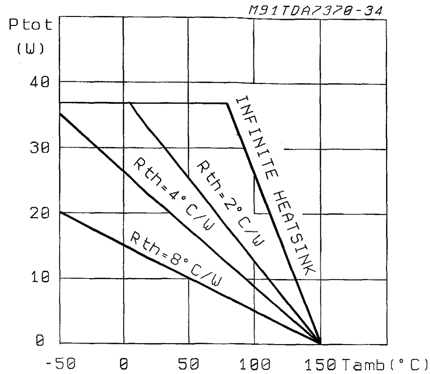
The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 17 shows the dissipable power as a function of ambient temperature for different thermal resistance.

Figure 17: Maximum Allowable Power Dissipation vs. Ambient Temperature



Loudspeaker Protection

The TDA7374 guarantees safe operations even for the loudspeaker in case of accidental shortcircuit.
Whenever a single OUT to GND, OUT to V_S short circuit occurs both the outputs are switched OFF so limiting dangerous DC current flowing through the loudspeaker.

CLIPPING DETECTOR

Fig 19 shows an application using the TDA7374 in combination with the SGS-THOMSON audioprocessor TDA7302.

The output clipping is recognized by the microprocessor (in this application it is simulated by a PC).

The detailed way to operate of the system is represented by the flow-chart of fig.18.

The controller detects when the clipping is active (minimun detection width fixed by a C29 = 12 nF external capacitor), and reduces the volume (or bass) by step of 2 dB (with a programmable waiting time), until no more clipping is detected.

Then the controller waits for a programmable time before increasing the volume again by step of 2 dB until clipping is again detected or the panel selected volume is reached.

Practical advantages of this application is a better sound quality deriving from operation under no clipping conditions, which also means the availability of higher undistorted power.

WHAT IS NEEDED FOR A DEMONSTRATION

- a XT or AT IBM compatible PC, supplied with EGA card
- a SGS-THOMSON audioprocessor application disk
- a TDA 7302 + TDA7374 board
- a connector from audioprocessor board to PC parallel port

GENERAL INFORMATION

In the application shown in fig 18 the TDA7302 audioprocessor works on PC XT or AT IBM compatible.

Control is accomplished by serial bus (S-bus or I^2C-bus or SPI bus) sent to the test board through the PC parallel port.

The PC simulates the behaviour of the microprocessor in a real application (for example in a car radio) and the buffer is necessary only in this application for protecting the PC.

Figure: 18: Clipping Detector Control Routine

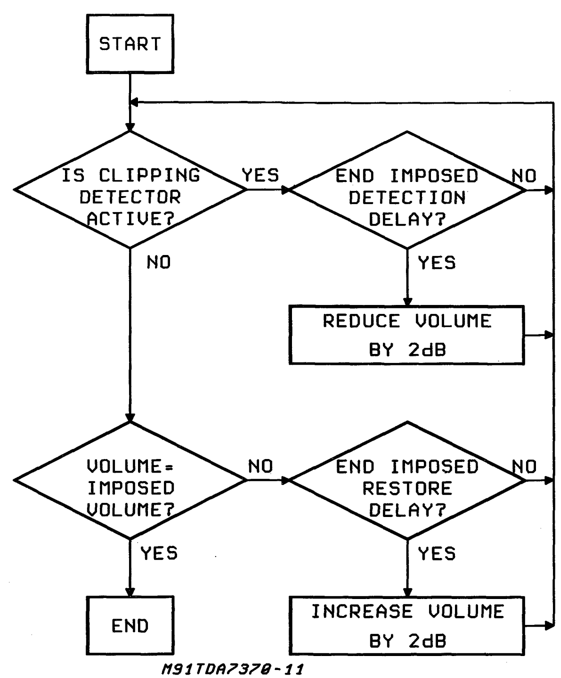
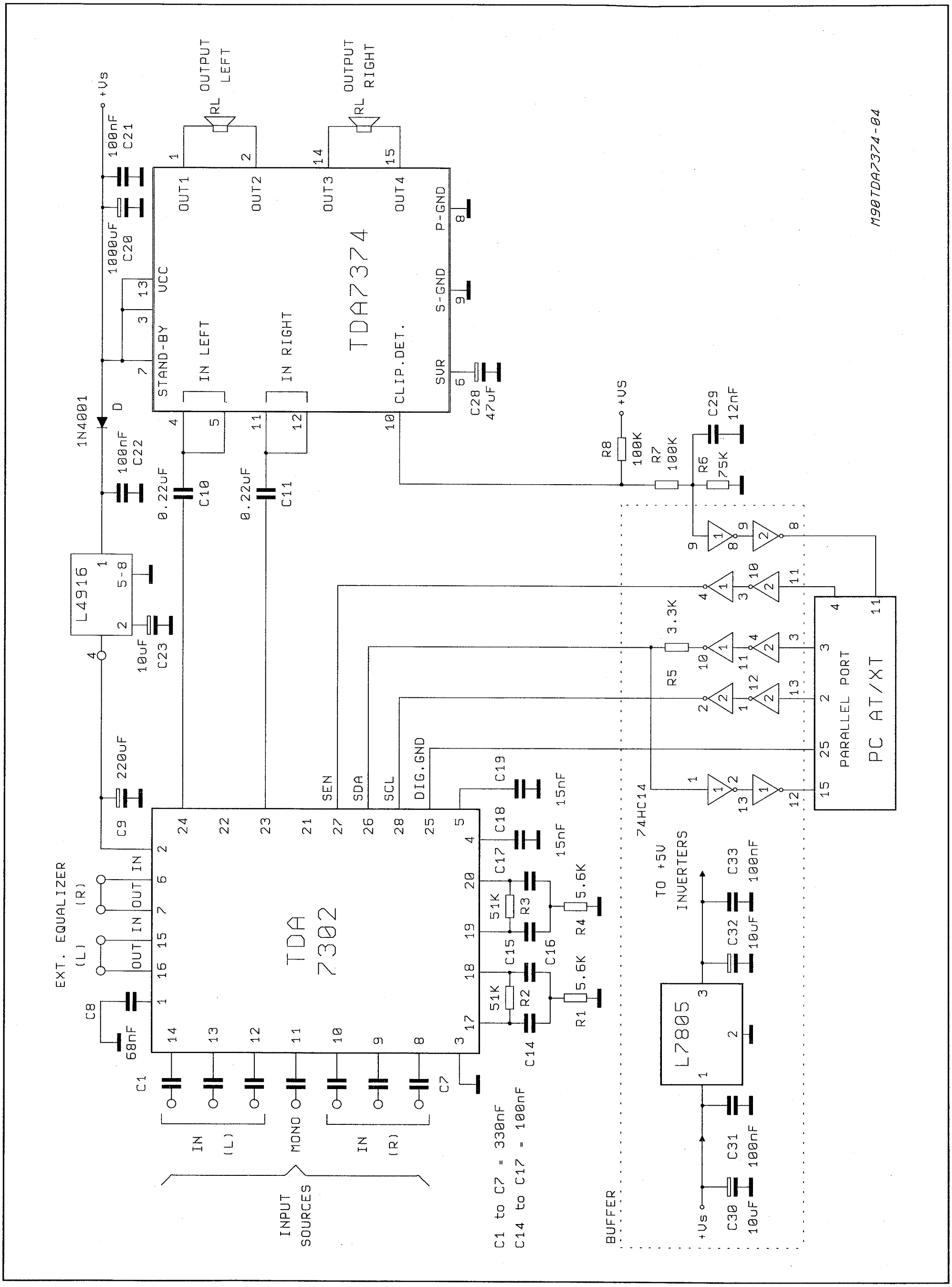


Figure 19: Application with TDA7302 + TDA7374

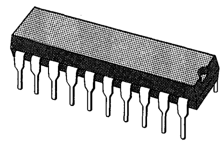


SGS-THOMSON
MICROELECTRONICS

TDA8190

TV SOUND CHANNEL WITH DC CONTROLS

- SEPARATE VCR INPUT AND OUTPUT PINS
- 4W OUTPUT POWER INTO 16Ω
- NO SCREENING REQUIRED
- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- LOW DISTORTION
- DC TONE/VOLUME CONTROLS
- THERMAL PROTECTION



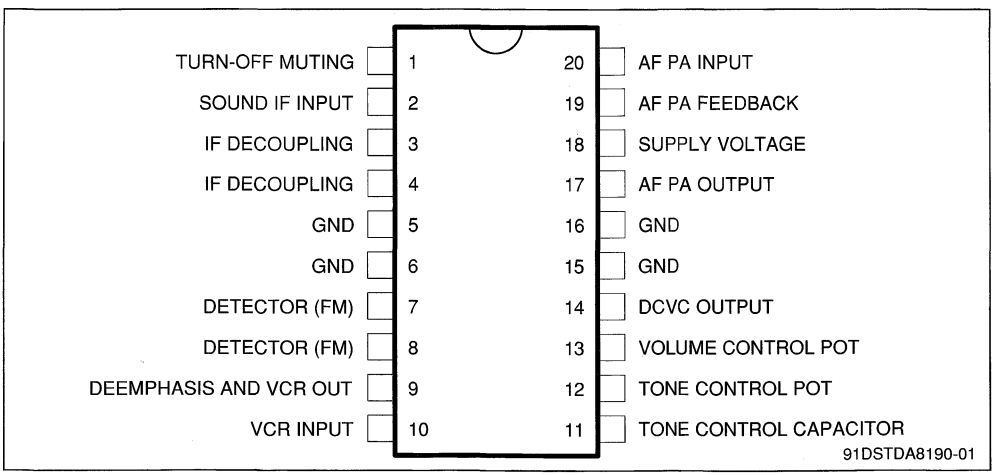
DIP20
(Plastic Package)

ORDER CODE : TDA8190

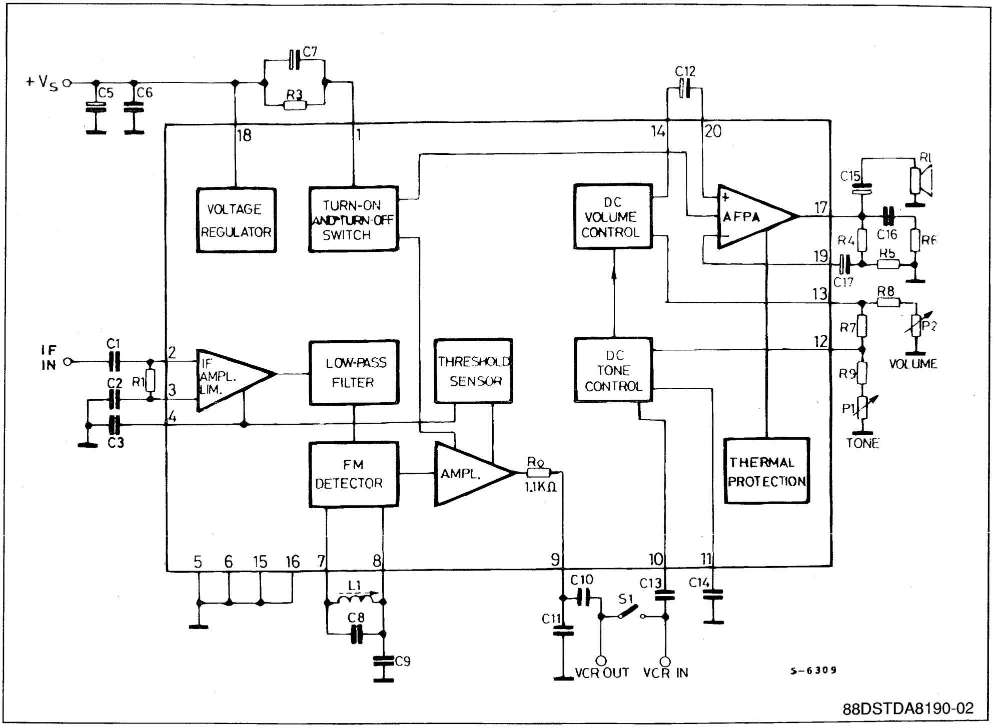
DESCRIPTION

The TDA8190 is a complete TV sound channel with DC tone and volume controls plus separate VCR input and output connections. Mounted in a Powerdip 16 + 2 + 2 package, the device delivers an output power of 4W into 16Ω (d = 10%, V_S = 24V) or 1.5W into 8Ω (d = 10%, V_S = 12V). Included in the TDA8190 are : IF amplifier limiter, active low-pass filter, AF pre-amplifier and power amplifier, turn-off muting, mute circuit and thermal protection. High output, high sensitivity, excellent AM rejection and low distortion make the device suitable for use in TVs of almost every type. Further, no screening is necessary because the device is free of radiation problems.

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 18)	28	V
V_l	Voltage at Pin 1	$\pm V_s$	
V_i	Input Voltage (pin 2)	1	V_{pp}
I_o	Output Peak Current (repetitive)	1.5	A
I_o	Output Peak Current (non repetitive)	2	A
I_4	Current (pin 4)	10	mA
P_{tot}	Power Dissipation : at T_{pins} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{stg} - T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W*

(*) Obtained with GND pins soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_S = 24V, S1 : on, Δf = ± 25kHz, V_I = 1mV, P_1 = 12kΩ, f_o = 4.5MHz, f_m = 400Hz, T_{amb} = 25°C, unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
V_s	Supply Voltage (pin 18)	P_2 = 12kΩ	10.8		27	V
V_o	Quiescent Output Voltage (pin 17)	P_2 = 12kΩ	11	12	13	V
V_1	Pin 1 DC Voltage	P_2 = 12kΩ, R_1 = 270kΩ		5.3		V
V_4	Pin 4 DC Voltage	P_2 = 12kΩ		3.2		V
I_d	Quiescent Drain Current	P_2 = 12kΩ		32		mA
IF AMPLIFIER AND DETECTOR						
$V_{i\ (threshold)}$	Input Limiting Voltage at Pin 2 (–3dB)	V_o = 4 V_{rms}		50	100	μV
V_9	Recovered Audio Voltage (pin 9)	Δf = ± 7.5kHz, P_2 = 12kΩ	140	200	280	mV
AMR	Amplitude Modulation Rejection (*)	m = 0.3, V_i = 1mV, V_o = 4V_{RMS}		60		dB
R_i	Input Resistance (pin 2)	Δf = 0, P_2 = 12 kΩ		30		kΩ
C_i	Input Capacitance (pin 2)	Δf = 0, P_2 = 12 kΩ		6		pF
R_9	Deemphasis Resistance	C_1 = 68 to 888 nF	0.75	1.1	1.5	kΩ
DC VOLUME CONTROL						
K_v	Volume Attenuation (resistance control)	P_2 = 0 Ω P_2 = 4.3 kΩ P_2 = 12 kΩ	20	0 26 88	32	dB dB dB
V_c	Control Voltage	K = 0 dB K = 26 dB K = 88 dB		0 1.3 2.6		V V V
$\frac{\Delta K_V}{\Delta T_{pins}}$	Volume Attenuation Thermal Drift (resistance control)	T_{pins} = 25 to 85 °C P_2 = 4.3 kΩ		– 0.05		dB/°C
DC TONE CONTROL						
K_T	Tone Cut	S1 : Off V_{10} = 200 mV P_1 = 12 kΩ to 100 Ω f_{AF} = 10 kHz		14		dB
AUDIO FREQUENCY AMPLIFIER						
P_o	Output Power (d = 10 %)	V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω	3.5	4.1 1.5		W W
B	Frequency Response of Audio Amplifier (– 3 dB)	P_o = 1 W R_L = 16 Ω S1 : Off V_{10} = 200 mV V_o = 4 V_{RMS} @400 Hz	15	50		kHz
SVR	Supply Voltage Rejection	P_2 = 12kΩ Δf = 0 f_{ripple} = 120Hz		26		dB

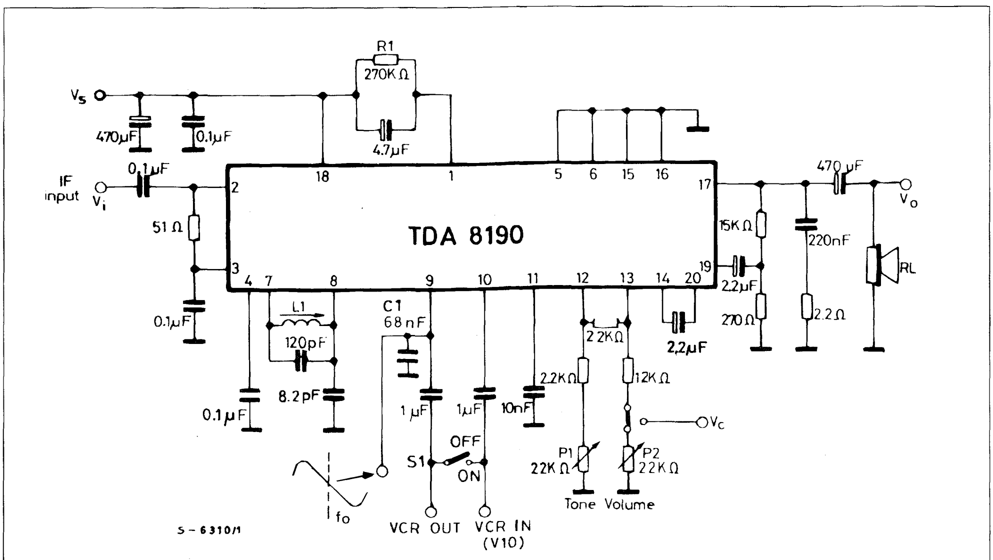
ELECTRICAL CHARACTERISTICS (continued)

(refer to the test circuit, V_S = 24V, S1 : on, $\Delta f = \pm$ 25kHz, V_I = 1mV, P_1 = 12kΩ, f_o = 4.5MHz, f_m = 400Hz, T_{amb} = 25°C, unless otherwise specified).

Symbol	Parameter	Test Conditions	Typ.	Max.	Unit	
V. C. R.						
d	Total Harmonic Distortion of pin 9 Output Signal	$\Delta f = \pm$ 7.5 kHz V_i = 1 mV		0.5		%
SVR	Supply Voltage Rejection at Output Pin 9	Δf = 0 f_{ripple} = 120 Hz P_2 = 12 kΩ		66		dB
$\frac{S+N}{N}$	Signal to Noise Ratio at Output Pin 9	Δf = 25 kHz $V_i \geq$ 1 mV		70		dB
V_{10}	Input Voltage (playback)	V_o = 4 V_{rms} P_2 = 0 S1 : Off	50	70	100	mV
R_{10}	Input Resistance (playback)	S1 : Off	10			kΩ
	Total Harmonic Distortion for 20 dB Overload of V_{10}	S1 : Off V_{10} = 1 V_{rms} V_o = 4 V_{rms}		0.5	3	%
OVERALL CIRCUIT						
$\frac{S+N}{N}$	Signal to Noise Ratio (*)	$V_i \geq$ 1 mV V_o = 4 V_{rms} Δf = 0		70		dB
d	Distortion (*)	P_o = 50 mW $\Delta f = \pm$ 7.5 Hz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		 0.5 0.5		 % %
M	Muting (*)	V_o = 4 V_{rms}@ no V_1 ; V_1 = 0	100			dB
Δf	Deviation Sensitivity	P_2 = 0 V_o = 4 V_{rms}		3	6	kHz

* Test Bandwidth = 20KHz.

TEST CIRCUIT



88DSTDA8190-03

TEST CONDITIONS (unless otherwise specified)

V_S = 24V ;	Q_o = 60 ;	f_o = 4.5MHz;
V_{in} = 1mV ;	f_m = 400Hz ;	$\Delta f = \pm$ 25KHz ;
P_1 = 12KΩ ;	$R_L = \infty$;	S1 = on ;

Figure 1 : Relative Audio Output Voltage and Output Noise vs. Input Signal.

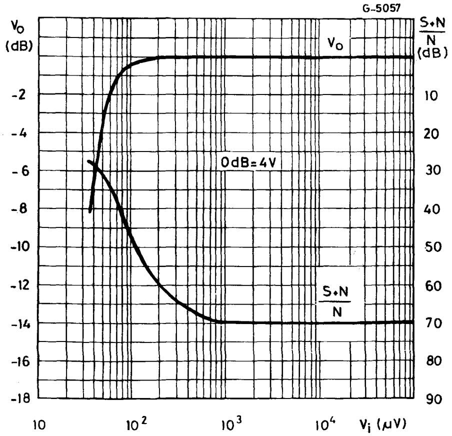


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Figure 2 : Output Voltage Alternation vs. DC Volume Control Resistance (a) or Vs. DC Volume Control Voltage (b).

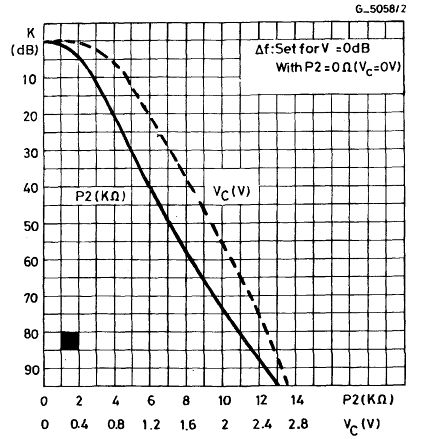

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Figure 3 : DC Tone Control Cut of the High Audio Frequencies for some Values of Resistance adjusted by P1.

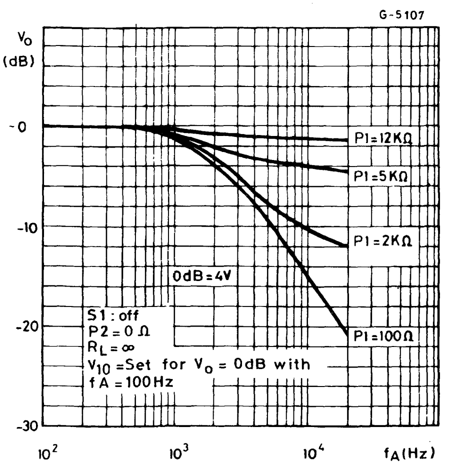

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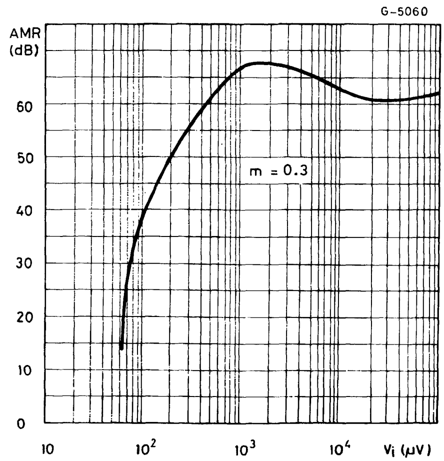
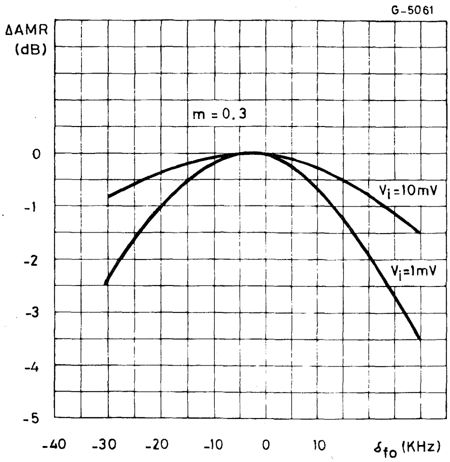
Figure 4 : Amplitude Modulation Rejection vs. Input Signal.



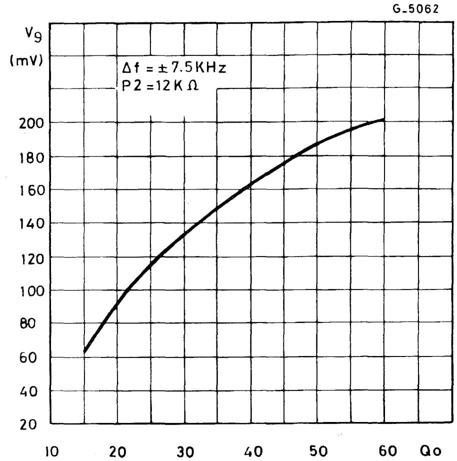
88DSTDA8190-07

Figure 5 : ΔAMR vs. Timing Frequency Change.



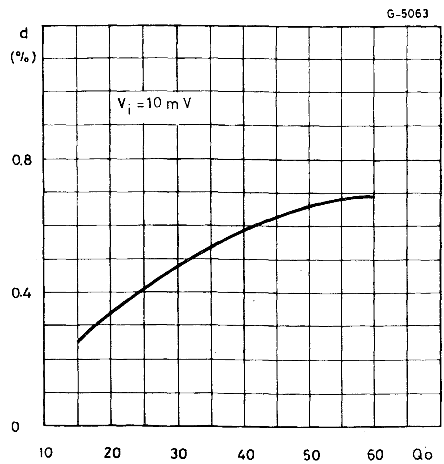
88DSTDA8190-08

Figure 6 : Recovered udio Voltage vs. Unloaded Q – factor of the Detector Coil.



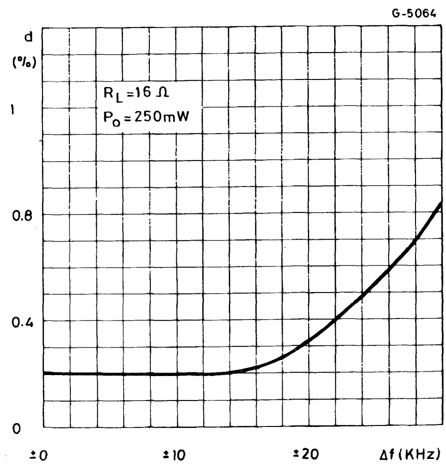
88DSTDA8190-09

Figure 7 : Distortion vs. Unloaded Q – factor of the Detector Coil.



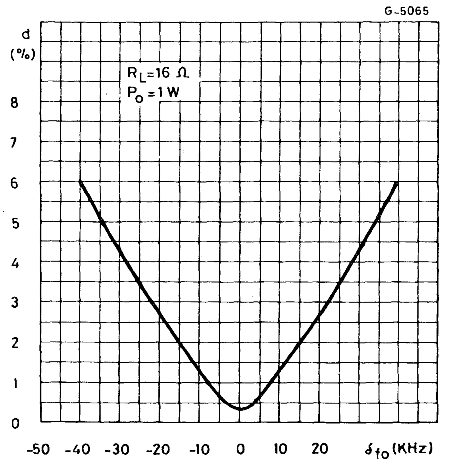
88DSTDA8190-10

Figure 8 : Distortion vs. Frequency Variation.



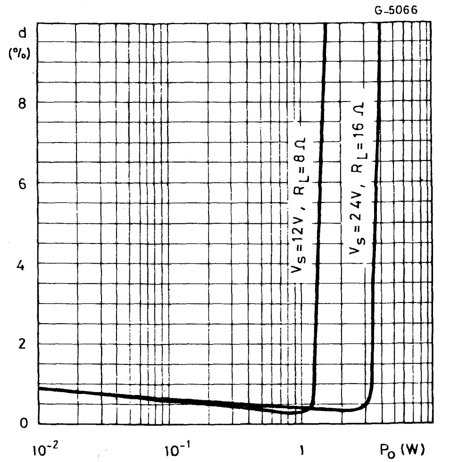
88DSTDA8190-11

Figure 9 : Distortion vs. Tuning Frequency Change.



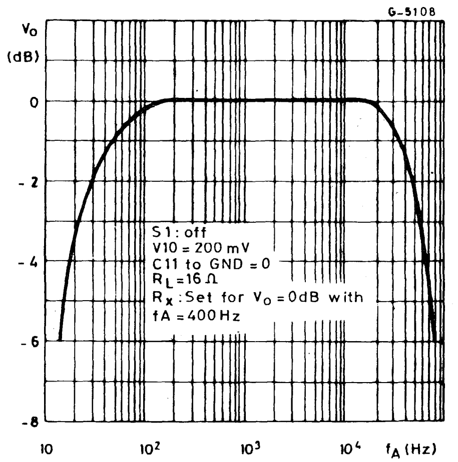
88DSTDA8190-12

Figure 10 : Distortion vs. Output Power.



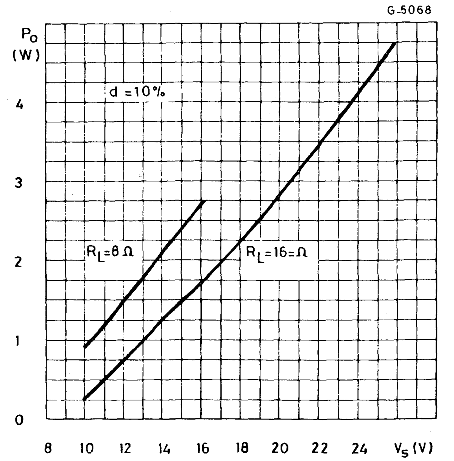
88DSTDA8190-13

Figure 11 : Audio Amplifier Frequency Response.



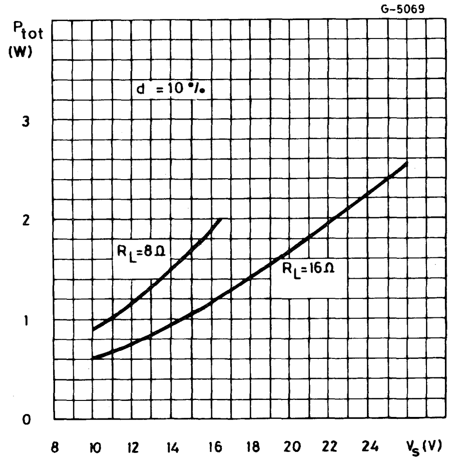
88DSTDA8190-14

Figure 12 : Output Power vs. Supply Voltage.



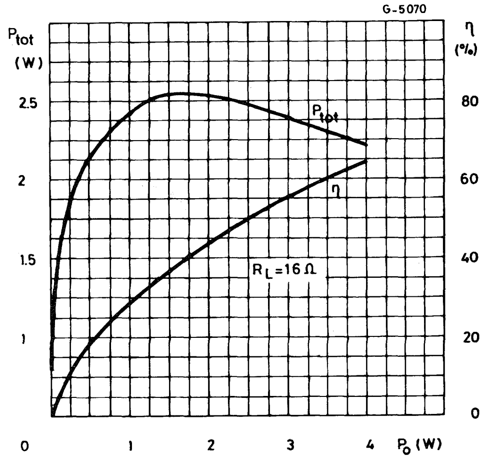
88DSTDA8190-15

Figure 13 : Power Dissipation vs. Supply Voltage(sine wave operation).



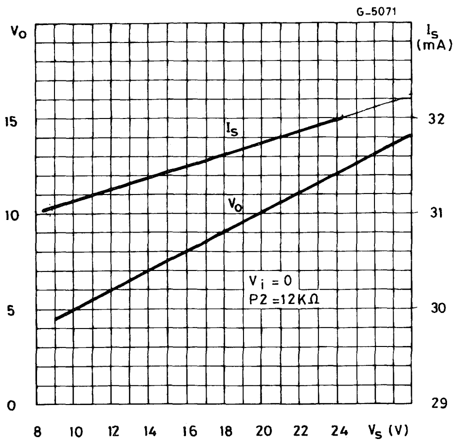
88DSTDA8190-16

Figure 14 : Power Dissipation and Efficiency vs. Output Power.



88DSTDA8190-17

Figure 15 : Quiescent Drain and Quiescent Output Voltage vs. Supply Voltage.



88DSTDA8190-18

SGS-THOMSON MICROELECTRONICS

APPLICATION INFORMATION (refer to the block diagram)

IF AMPLIFIER-LIMITER

It is made by six differential stages of 15dB gain each so that an open loop gain of 90dB is obtained.

While a unity DC gain is provided, the AC closed loop gain is internally fixed at 70dB that allows a typical input sensitivity of 50µV.

The differential output signal is single ended by a 20dB gain amplifier that through a buffer stage, feeds the detector system.

Internal diodes protect the inputs against overloads.

- Pin 2 is the IF non-inverting input
- Pin 3 is decoupled by a capacitor to open the AC loop
- Pin 4 grounded by a capacitor, allows a typical sensitivity of 50µV. (see VCR facility too).

LOW-PASS FILTER, FM DETECTOR AND AMPLIFIER

The IF signal is detected by converting the frequency modulation into amplitude modulation and then detecting it.

Since the available modulated signal is a square wave, a 40 dB/decade low-pass filter cuts its harmonics so that a sine wave can feed the two-resonances external network L1, C8 and C9.

This network defines the working frequency value, the amplitude of the recovered audio signal and its distortion at the highest frequency deviations.

The two resonances f1 (series resonance) and f2 (parallel resonance) can be computed respectively by :

$$X_{C9} = \frac{X_{L1} \cdot X_{C8}}{X_{L1} + X_{C8}} \quad \text{and } X_{L1} = X_{C8}$$

The ratio of these frequencies defines the peak-to-peak separation of the "S" curve :

$$\frac{f_2}{f_1} = \sqrt{1 + \frac{C_9}{C_8}}$$

A differential peak detector detects the audio frequency signal that amplified, reaches the deemphasis network R0 ; C11.

The AF amplifier can be muted (see turn-on and turn-off switch and VCR facility).

- Pin 7 is the output of the low-pass filter and one input of the differential peak detector
- Pin 8 is the other input of the differential peak detector
- Pin 9 is used to provide the required deemphasis time constant by grounding it with C11. At this pin, the internal impedance of which is typically of 1.1K, is available the recovered audio signal as auxiliary output.

DC TONE CONTROL

The same signal available or applied to pin 10, after a voltage to current converter, reaches, the DC Tone Control block. It operates, inside the 10KHz bandwidth, by cutting the high audio frequencies with a variable slope of an RC network, by means of P_1.

The maximum slope of the RC network is of 20dB per decade and its pole is defined by :

X_{C11} = 6.8K, typically.

Pin 11 - At this pin is tied the tone capacitor.

Pin 12 - Is the DC Tone Control input.

DC VOLUME CONTROL

After tone control regulation, the AF current signal reaches the DC volume control block that controls its intensity. The normal control, for which the block has been designed for a narrow spread, is produced by P2 ; however, without P2, a voltage control can be operated by forcing a voltage at pin 13 through R8.

- Pin 12, already seen as a DCTC input, is the reference voltage for the DCVC. Because of this, a small interface between tone and volume regulation can be expected.
- Pin 13 is the DC volume control input.
- Pin 14 after a current to voltage converter, the audio frequency signal comes out at this pin.

AUDIO FREQUENCY POWER AMPLIFIER AND THERMAL PROTECTION

Through C12 the signal reaches the amplifier non-inverting input. The closed loop gain is defined by the feedback at pin 19 (inverting input) or by the ratio :

$$G_v = 20 \text{ Log } \frac{\overline{R5 + R4}}{R5} \quad \text{(dB)}$$

The amplifier, thermally protected, can supply 4W of power into a 16 load with 24V of supply voltage. The power output stage is a class B type.

- Pin 20 is the non-inverting input
- Pin 19 is the inverting input
- Pin 17 is the output of the AFPA.

TURN-ON AND TURN-OFF SWITCH

This block has been mainly designed to avoid, turning on the TV set, that transients, produced by the vision output, can reach the speaker.

Moreover this block, together an optimized rise time and full time of the supply voltage V_S, can avoid any pop generally produced during the turn-on and the turn-off transients.

Turninig on, pin 1 follows the supply voltage V_S by means of C7 ; a threshold is reached and the muting of the AFPA output (pin 17) is suddenly produced.

When V_S reaches it stop, C7 charges itself through the input impedance of pin 1 and the muting is removed with a time constant depending on the C7 value.

Turning off, the V_S trend, in series to the voltage V_S V_1 and which C7 is charged, drives pin 1 at a low level threshold and a sudden muting is produced again.

Since the turn-off can be operated with high output power, if the muting operates when the current through the inductance of the speaker is different from zero, a flyback is generated and then a small pop can be produced.

The flyback is clipped by integrated diodes.

The thresholds that produce the muting have been chosen in the way that 1 Vpp of ripple on the supply voltage does not produce any switching..

- Pin 1 is the turn-on and turn-off muting input.

SUPPLY

An integrated voltage regulator with different output levels, supplies all the blocks operating with small signal.

- Pin 18 is the main supply of the device.
- Pin 5 ; pin 6 ; pin 15 and pin 16 are the ground of the supply. These pins are used to drain out from the device the heat produced by the dissipated power.

Components	Units	Appl. 4.5 MHz	Appl. 5.5 MHz	Appl. 6 MHz
L1	µH	10 Q_o = 60	12 Q_o = 80	10 Q_o = 70
C5	pF	120	68	68
C4	pF	9	8.2	6.8
C8	nF	68	47	47
C. F		Murata SFE 4.5 MA	Murata SFE 5.5 MB	Murata SFE 6.0 MB
C1	pF	22	18	18
R2	Ω	1000	560	470
R3	Ω	1000	560	470

Figure 16 : Application Circuit.

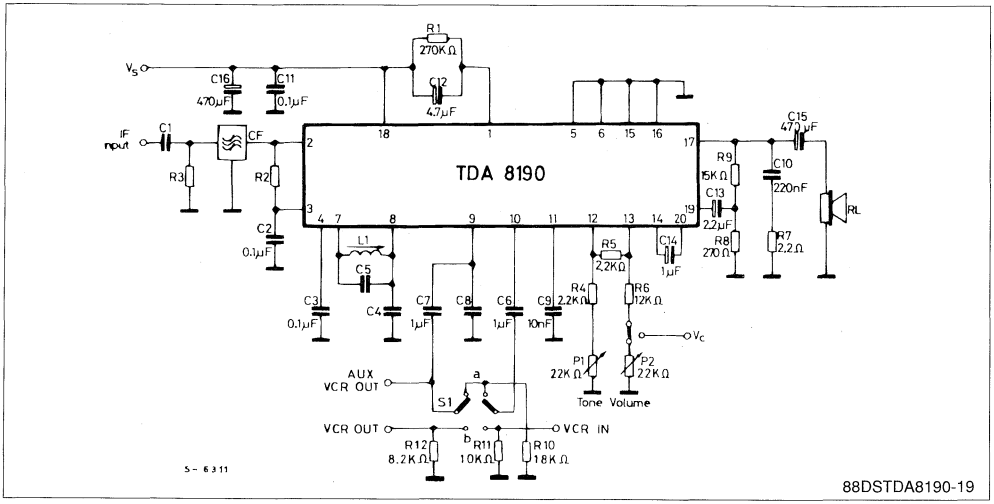
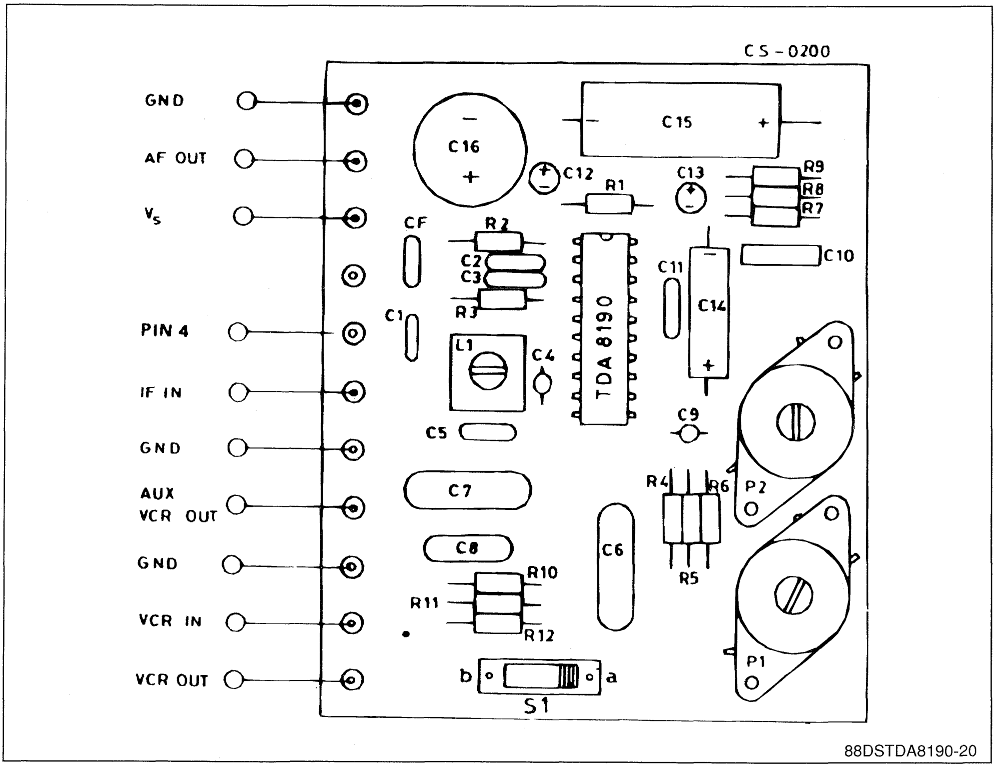
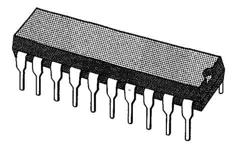


Figure 17 : PC Board and Components Layout of the Circuit of Fig. 16 (1 : 1 scale).



TV SOUND CHANNEL

- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- DC VOLUME CONTROL
- PERITELEVISION FACILITY
- 4W OUTPUT POWER
- LOW DISTORTION
- THERMAL PROTECTION
- TURN-ON AND TURN-OFF MUTING



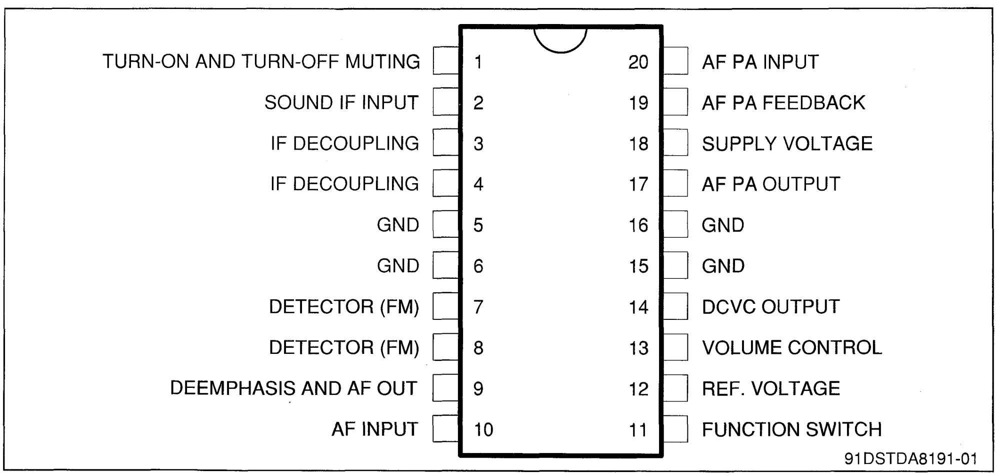
DIP20
(Plastic Package)

ORDER CODE : TDA8191

DESCRIPTION

The TDA8191 is a monolithic integrated circuit that includes all the functions needed for a complete TV sound channel. The TDA8191 is assembled in a 20 pin dual in line power package.

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vs	Supply Voltage (pin 18)	28	V
Vl	Voltage at Pin 1	± Vs	
Vi	Input Voltage (pin 2)	1	V_{PP}
Io	Output Peak Current (repetitive)	1.5	A
Io	Output Peak Current (non repetitive)	2	A
Ptot	Total Power Dissipation : at Tpins = 90°C at Tamb = 70°C	4.3 1	W W
Tstg, Tj	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ (j\text{-}pins)}$ $R_{th\ (j\text{-}amb)}$	Junction-pins Thermal Resistance Junction-ambient Thermal Resistance	Max Max	14 80	°C/W °C/W

ELECTRICAL CHARACTERISTICS

(Refer to fig. 1 ; V_S = 24V, R_L = 16Ω, pin 11 floating, Δf = ±50kHz, V_i = 1mV, f_o = 5.5MHz, f_m = 1kHz, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vs	Supply Voltage (pin 18)	Vc = 4.5V	10.8	24	27	V
Vo	Quiescent Output Voltage (pin 17)	Vc = 4.5V	11	12	13	V
V1	Pin 1 DC Voltage	Vc = 4.5V		5.3		V
Id	Quiescent Drain Current	Vc = 4.5V		35		mA
Vi	Input Limiting Voltage at Pin 2 (– 3dB)	Vo = 4V_{RMS}		50	100	μV
V9	Recovered Audio Voltage (pin 9)	Vc = 4.5V Δf = ± 15KHz	200		400	mV_{RMS}
R9	Deemphasis Resistance	f = 20Hz to 20KHz	500	700	1000	Ω
AMR	Amplitude Modul. Rejection	m = 0.3 Vo = 4V_{RMS}	45	60		dB
Ri	Input Resistance (pin 2)	Δf = 0		30		kΩ
Ci	Input Capacitance (pin 2)	Δf = 0 Vc =4.5V		6		pF
V12	DCVC Reference Voltage		5.6		6.2	V
Kv	Volume Attenuation	Vc = 0.5V ; Fig. 2 Vc = 4.5V ; Fig. 2	 80		1.0	dB dB
$\frac{\Delta K_V}{\Delta T_j}$	Volume Attenuation Thermal Drift	Tj = 300 to 380°K Fig. 3		– 0.05	– 0.1	dB/°C
Po	Output Power (d = 10%)		3.5	4		W
SVR	Supply Voltage Rej. (pin 17) (pin 9)	Vc = 4.5V f_{ripple} = 100Hz	20 50	26 60		dB dB
V11	Function Switch. - Television Broadc. Reproduction		0		2	V
			or Pin 11 Floating			
	- Peritelevision Reproduction		8		12	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R11	Input Resistance		10			kΩ
V10	Input Voltage ($d \leq 2\%$)	$V_O = 4V_{RMS}$; $V_{11} = 12V$		0.5	2.0	V_{RMS}
R10	Input Resistance	f = 20Hz to 20KHz	10			kΩ
CT	Crosstalk between Pins 9, 10		60			dB
$\frac{S+N}{N}$	Signal to Noise Ratio	$\Delta f = 0$; $V_O = 4V_{RMS}$	60	70		dB
d	Distortion (Po = 250mV)				2	%
Δf	Deviation Sens.	$V_C = 0.5V$; $V_O = 4V_{RMS}$		± 4	± 10	kHz

Figure 1 : Test Circuit.

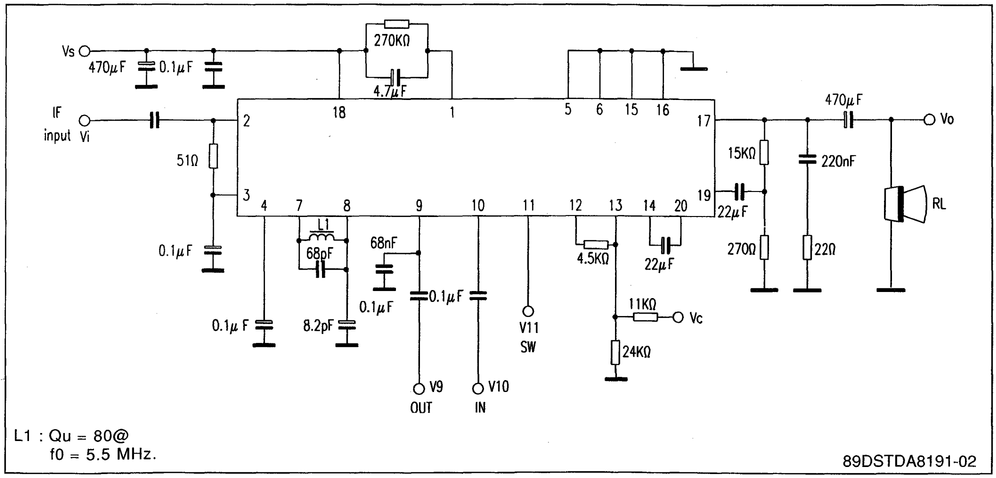
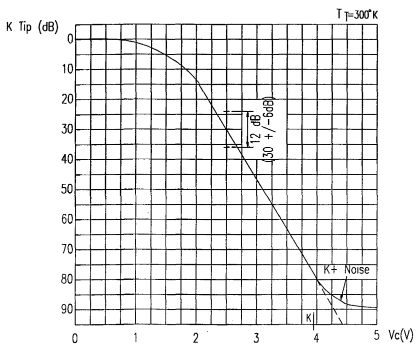
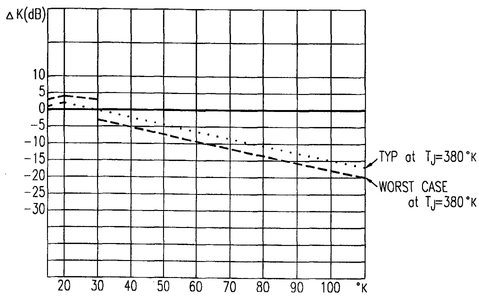


Figure 2 : Volume Attenuation vs. DC Volume Control Voltage.



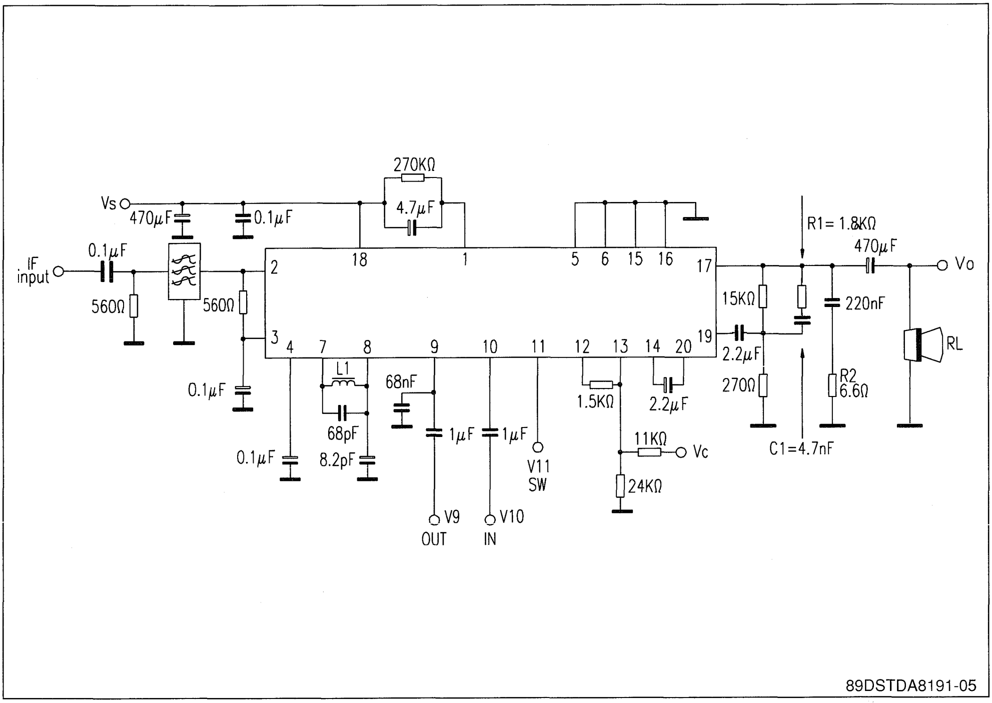
89DSTDA8191-03

Figure 3 : Volume Attenuation Thermal Drift.



89DSTDA8191-04

TYPICAL APPLICATION



L1 : Qu = 80e.
fo = 5.5MHz.

Figure 4 : AF Output Amplitude vs. AF Frequency by Using the Changes Shown on Fig. 4.

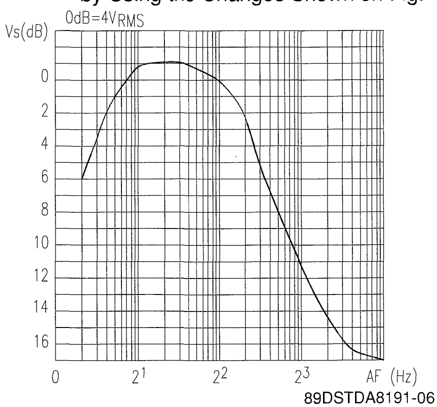


Figure 5 : Relative Audio Output Voltage and Output Noise vs. Input Signal.

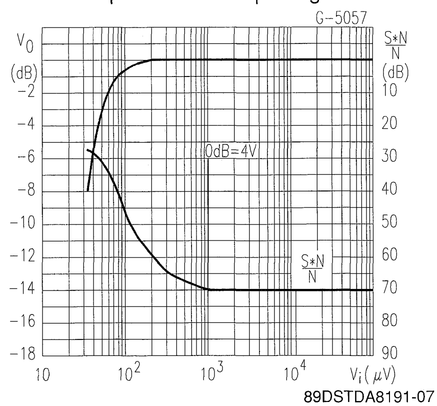
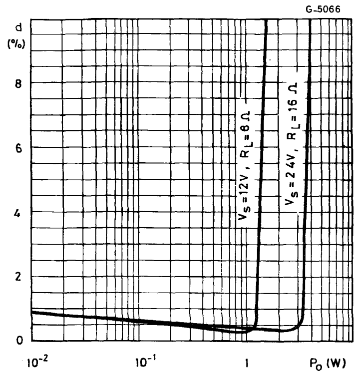
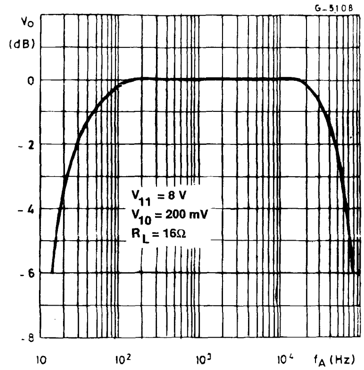


Figure 6 : Distortion vs. Output Power.



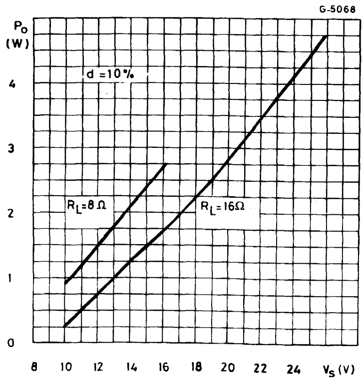
89DSTDA8191-08

Figure 7 : Audio Amplifier Frequency Response.



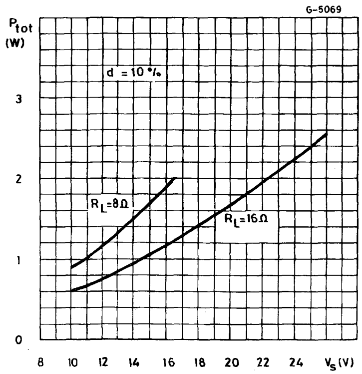
89DSTDA8191-09

Figure 8 : Output Power vs. Supply Voltage.



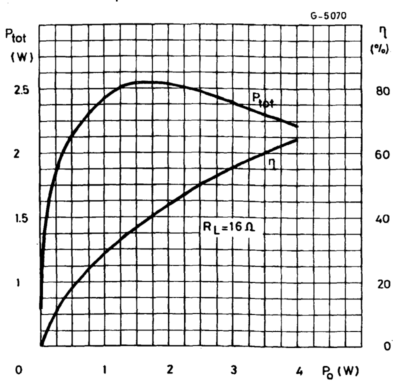
89DSTDA8191-10

Figure 9 : Power Dissipation vs. Supply Voltage (sine wave operation).



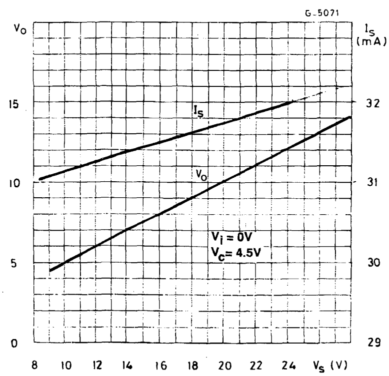
89DSTDA8191-11

Figure 10 : Power Dissipation and Efficiency vs. Output Power.



89DSTDA8191-12

Figure 11 : Quiescent Drain and Quiescent Output Voltage vs. Supply Voltage.



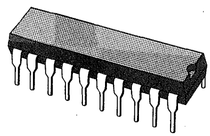
89DSTDA8191-13

MULTISTANDARD AM AND FM SOUND IF CIRCUIT FOR TV

The TDA8192 integrated circuit performs the following functions :

- A 2-STAGE GAIN CONTROLLED AMPLIFIER, PROVIDING COMPLETE IF GAIN ; (AM SECTION)
- A PEAK DETECTOR AND INTEGRATION WHICH PROVIDES AGC-VOLTAGE ; (AM SECTION)
- A 6-STAGE LIMITING AMPLIFIER FOLLOWED BY A SYNCHRONOUS DEMODULATOR AND DEEMPHASIS NETWORK ; (FM SECTION)
- AN AUDIO PREAMPLIFIER
- A CIRCUIT PROVIDING AM/FM SWITCHING AND MUTE FACILITIES
- AN EXTERNAL AUDIO INPUT CIRCUIT WITH SWITCHING FACILITIES TO DELIVER EITHER THE DEMODULATED IF, OR THE EXTERNAL AUDIO SIGNAL AT THE OUTPUT FULLY COMPATIBLE WITH THE SCART EUROPEAN NORM EN50 049
- A DC CONTROLLED VOLUME CIRCUIT

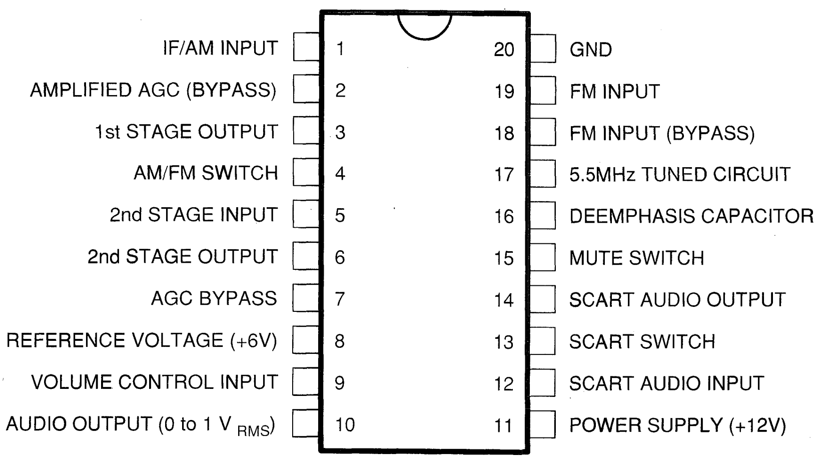
The demodulated IF signal is always available at a low impedance output.



DIP20
(Plastic Package)

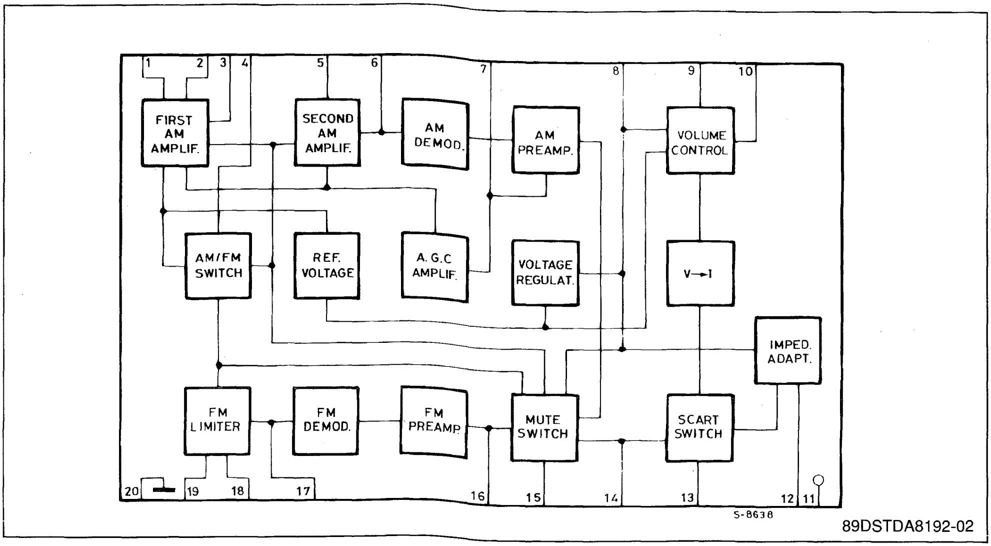
ORDER CODE : TDA8192

PIN CONNECTIONS



91DSTDA8192-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	16	V
P_{tot}	Total Power Dissipation at $T_{amb} \le 70°C$	800	mW
T_{op}	Operating Temperature	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 55 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient Max.	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 12V unless otherwise specified)

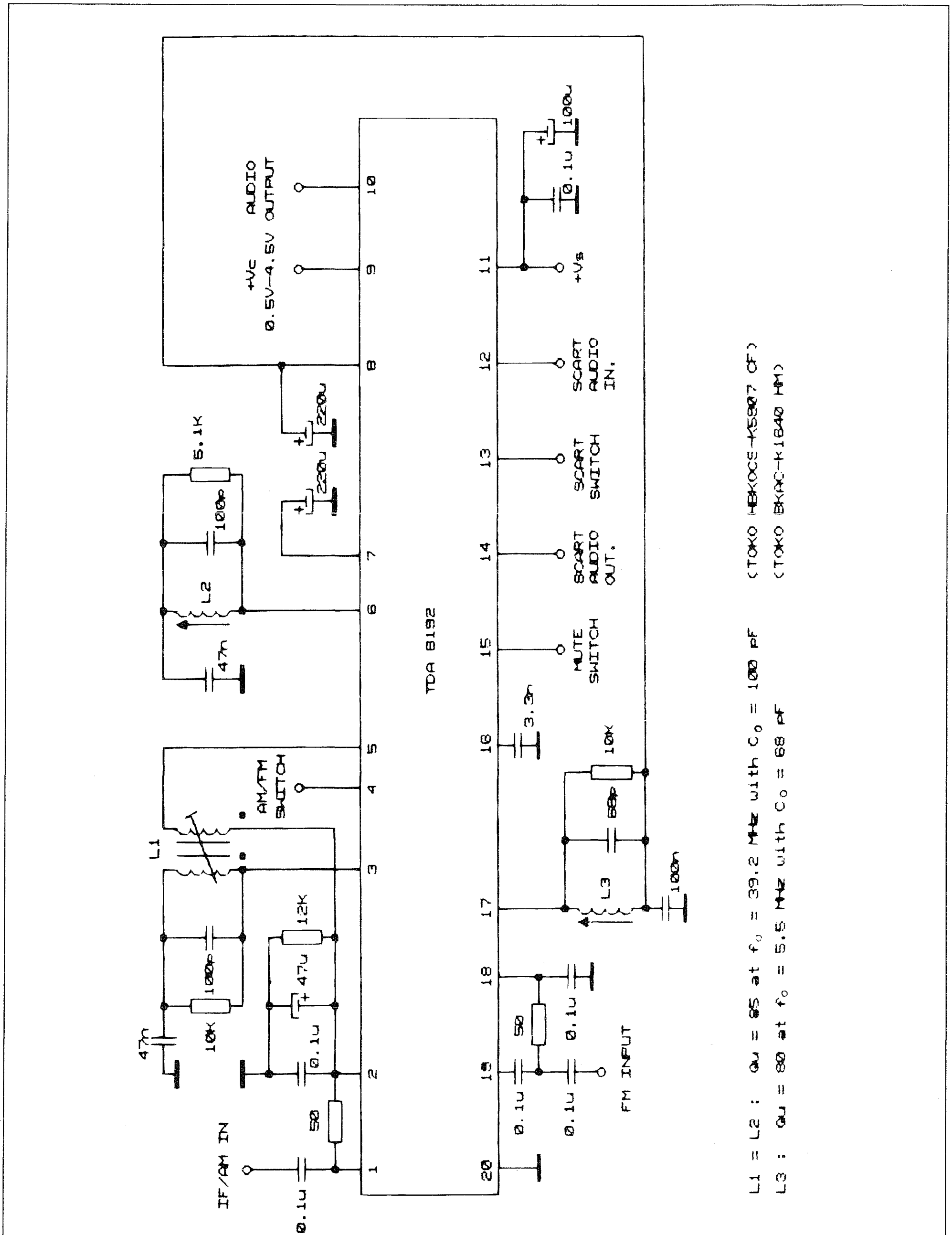
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		10.8	12	13.2	V
I_d	Current Drain	$V_i = 0$ AM FM		30 30		mA mA
AM SECTION (f_i = 39.2MHz, V_i = 1mV, m = 0.8, f_m = 1KHz unless otherwise specified)						
V_i	Input Sensitivity	S/N = 26dB		35		µV
$\frac{S+N}{N}$	Signal to Noise Ratio	V_i = 0.1mV m = 0.3 V_i = 1mV V_i = 10mV	 50	36 50 56		dB
V_i	AGC Range	ΔV_{OUT} = – 1 to + 1dB		66		dB
V_o	Recovered Audio Signal			1		V
d	Distortion (1)				3	%
d	Distortion (2)				3	%

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 12V unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AM SECTION (f_i = 39.2MHz, V_i = 1mV, m = 0.8, f_m = 1KHz unless otherwise specified)						
R_i	Input Resistance between Pins 1 and 2	m = 0	2			kΩ
C_i	Input Capacitance between Pins 1 and 2	m = 0		18		pF
FM SECTION (f_i = 5.5MHz, V_i = 1mV, Δf = ± 50KHz, f_m = 1KHz, unless otherwise specified)						
V_i	Input Limiting Voltage	– 3dB Limiting Point		30		µV
AMR	Amplitude Modulation	V_i = 30mV m = 0.3		55		dB
$\frac{S+N}{N}$	Signal to Noise Ratio	V_i = 1mV	60			dB
d	Distortion (3)				1.5	%
d	Distortion (4)			2		%
V_o	Recovered Audio Signal			1		V
R_i	Input Resistance	Δf = 0	2			kΩ
C_i	Input Capacitance	Δf = 0		14		pF
C_T	Crosstalk AM/FM			70		dB
AM/FM AND MUTE SWITCHING						
	FM "on" (pin. 4)		2.5		V_S	V
	AM "on" (pin 4)		0		0.8	V
	Mute "on" (pin 15)		0		1	V
	Mute "off" (pin 15)		5		V_S	V
	Signal Attenuation for Mute "off"		70			dB
	Mute Switch Current				50	µA
	AM/FM Switch Current		50		250	µA
SCART SWITCHING						
	Mode Selection Voltage : TV Selected (pin. 13)		0		5	V
	Mode Selection Voltage : Scart Selected (pin 13)		8		12	V
	Scart Switch Input Resistance		10			kΩ
	Scart Audio Input Amplitude (pin 12)			0.5	2	V_{rms}
	Crosstalk Between Switched Inputs (TV scart)			80		dB
DC VOLUME CONTROL						
	Audio Output Impedance (pin 10)				1	kΩ
	Control Range			90		dB
	Output/input Gain for Maximum Gain Control			0		dB
	Gain Control Voltage		0.5		4.5	V
	Noise Level (DIN 45405)			25		μV_{rms}

(1) 50% volume setting, V_i = 1mV
(2) 50% volume setting, V_i = 10mV
(3) V_i = 1mV, fm = 100 to 10.000Hz
(4) Vi = 1mV, ± 20KHz offset (detuning of phase shift filter).

TEST CIRCUIT



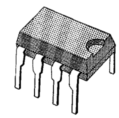
89DSTDA8192-03

SGS-THOMSON MICROELECTRONICS

TDA8196

AUDIO SWITCH AND DC VOLUME CONTROL FOR TV

- TWO AUDIO INPUTS WITH SWITCHING FACILITIES FULLY COMPATIBLE WITH THE SCART EUROPEAN NORM EN 50049
- DC VOLUME CONTROL



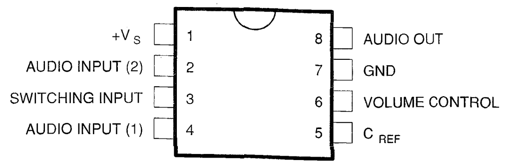
Minidip Plastic

ORDER CODE : TDA8196

DESCRIPTION

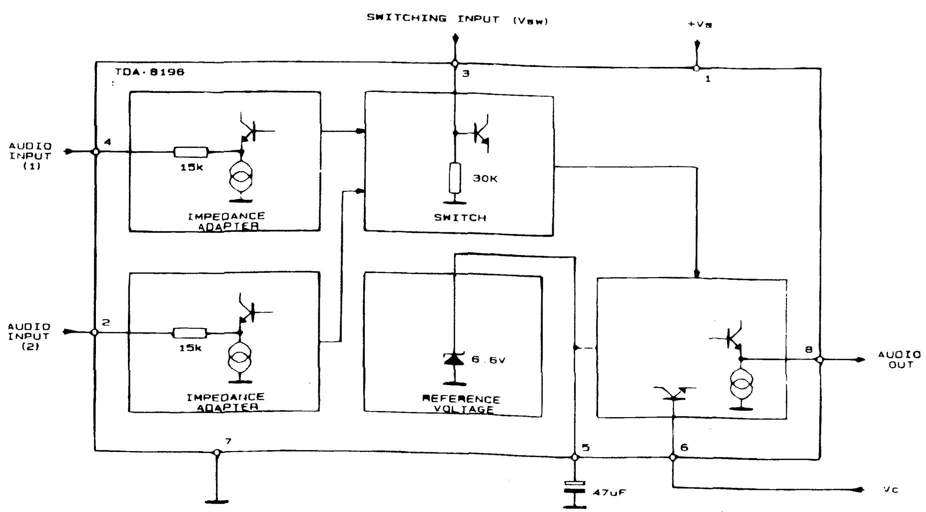
The TDA8196 is a monolithic integrated circuit in DIP8 package intended for TV applications.

PIN CONNECTION (top view)



91DSTDA8196-01

BLOCK DIAGRAM



89DSTDA8196-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 1)	16	V
T_{stg}, T_j	Storage and Junction Temperature	– 55 to 125	°C
T_{amb}	Operating Ambient Temperature	0 to 70	°C

TAB-01

THERMAL DATA

$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient Max	200	°C/W

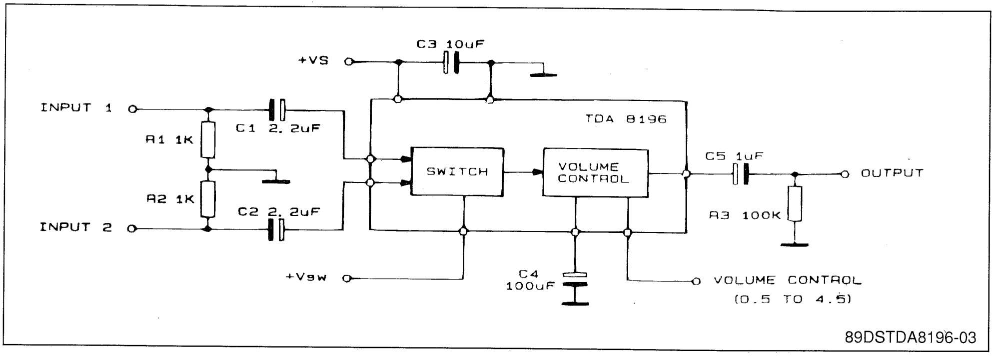
TAB-02

ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_S = 12V, T_{amb} = 25°C unless otherwise specified)

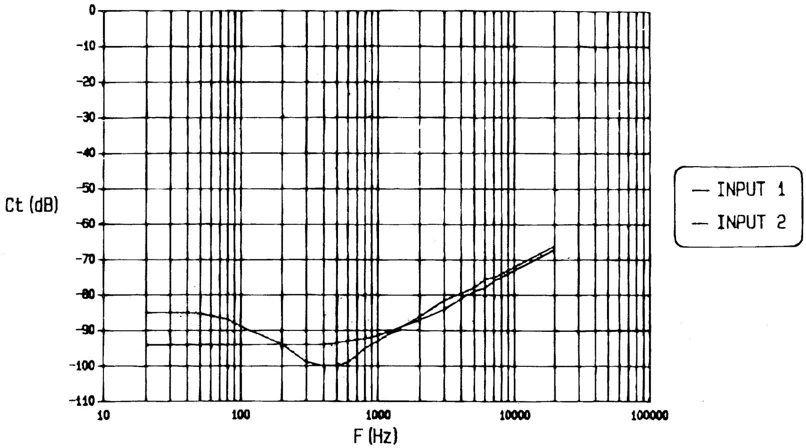
Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	1		10.8	12	13.2	V
I_S	Supply Current	1	V_i = 0, V_C = 0.5V		12		mA
V_R	Reference Voltage	5			6.6		V
V_{SW}	Switching Voltage Audio Input 1 Audio Input 2	3		 0 8		 5 12	 V V
R_{SW}	Switching Input Resistance	3	V_{SW} = 12V	20	30		kΩ
C_{SW}	Switching Input Capacitance	3				10	pF
C_t	Crosstalk between Switched Inputs		Selective Volmeter (B_W = 8Hz), see Fig.1	70	90		dB
V_i	Audio Input Amplitude (1 or 2)	4 2			0.5	2	V_{RMS}
R_i	Audio Input Resistance (1 or 2)	4 2		10	13		kΩ
K_{min}	Output / Input Gain for Max Vol				0		dB
R_O	Audio Output Resistance	8			0.2	1	kΩ
K_V	Attenuation Range		Selective Volmeter (B_W = 8Hz), see Fig.2	70	90		dB
V_C	Control Voltage Range $K_V = K_{MAX}$ (Vol. min) $K_V = K_{MIN}$ (Vol. max)	6			 0.5 4.5		 V V
THD	Distortion	8	V_i = 2 V_{RMS} @ V_C = 4.5V		0.4	1	%
En	Output Noise Level	8	DIN45405 V_C = 0.5V Weighted		40		μV_{RMS}
En	Output Noise Level	8	DIN45405 V_C = 4.5V Weighted		120		μV_{RMS}
$\frac{K_V}{\Delta T_a}$	Vol. Attenuation Thermal Drift		T_{amb} = 0 to 70°C K_V = 30dB, see Fig.3		0.04		dB/°C
SVR	Supply Voltage Rejection	8	V_C = 0.5V, f = 100Hz V_{ripple} = 1V_{PP} Selective Volmeter (B_W = 8Hz), see Fig.4 and 5		38		dB
V_O	Output DC Shift	8	V_C = 0.5 + 4.5V, V_i = 2 V_{RMS}		0.25		V

TEST CIRCUIT



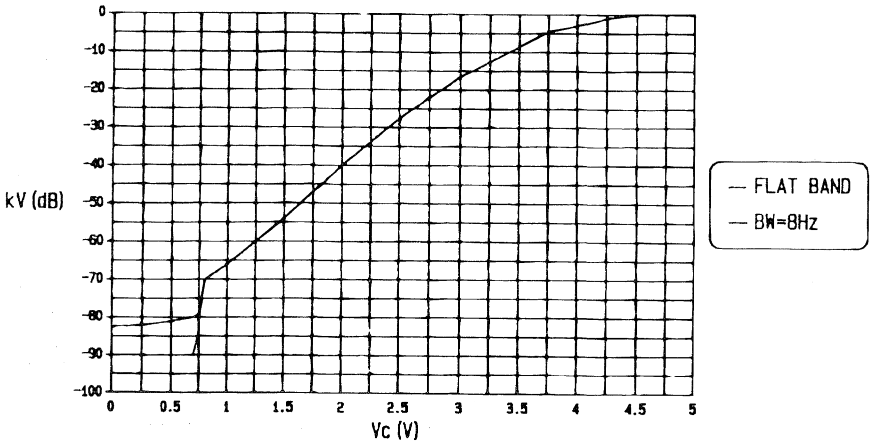
89DSTDA8196-03

Figure 1 : TDA8196 Crosstalk.



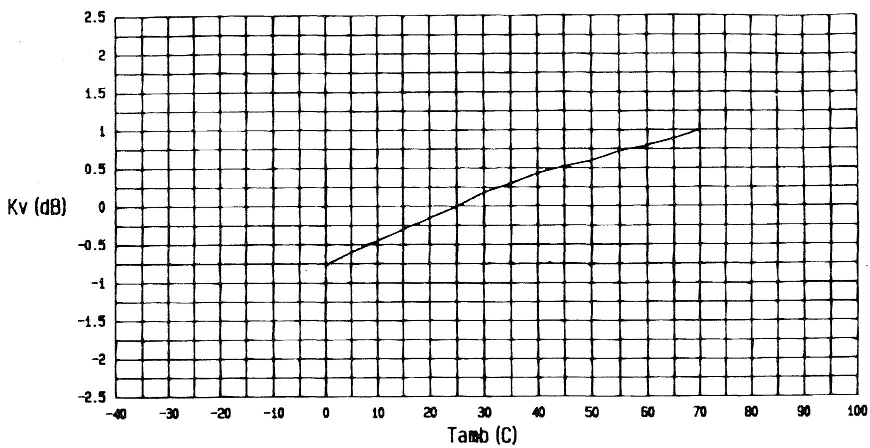
89DSTDA8196-04

Figure 2 : Output Attenuation versus DC Volume Control Voltage.



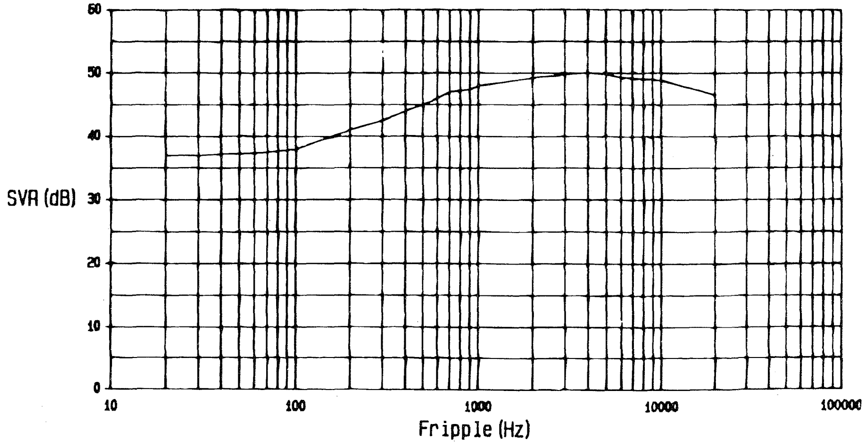
89DSTDA8196-05

Figure 3 : K_v Drift vs. T_{amb} Variation.



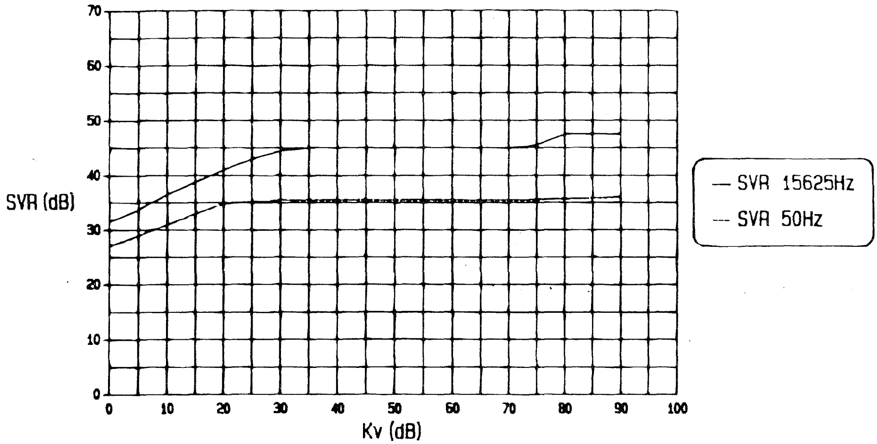
89DSTDA8196-06

Figure 4 : SVR vs. Ripple Frequency.



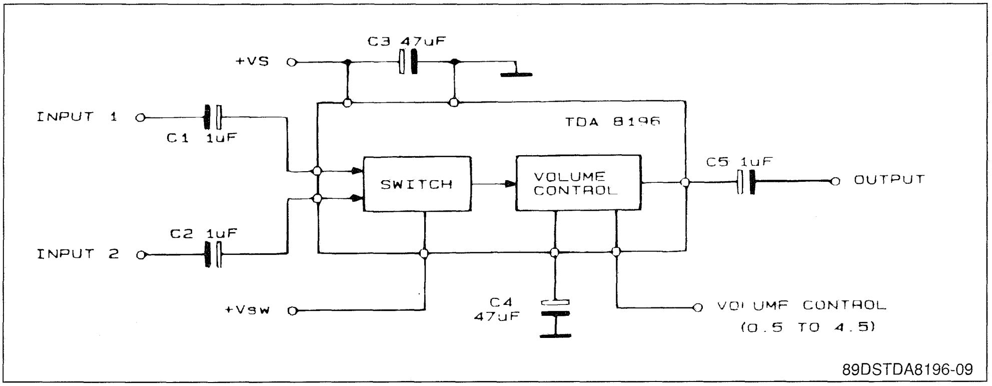
89DSTDA8196-07

Figure 5 : SVR vs. Volume Attenuation.



89DSTDA8196-08

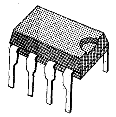
APPLICATION CIRCUIT



STEREO AMPLIFIER AND DC VOLUME CONTROL FOR TV

ADVANCE DATA

- STEREO CIRCUIT
- DC VOLUME CONTROL
- 12dB MAXIMUM GAIN



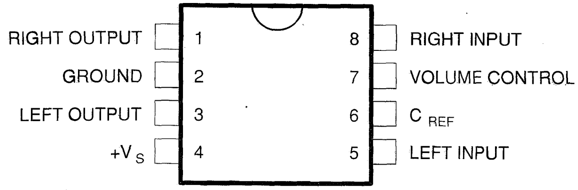
Minidip Plastic

ORDER CODE : TDA8199

DESCRIPTION

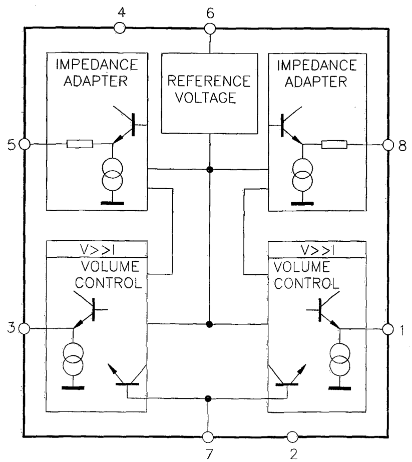
The TDA8199 is a monolithic integrated circuit in DIP8 package intented for TV applications.

PIN CONNECTIONS



91DSTDA8199-01

BLOCK DIAGRAM



91DSTDA8199-02

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

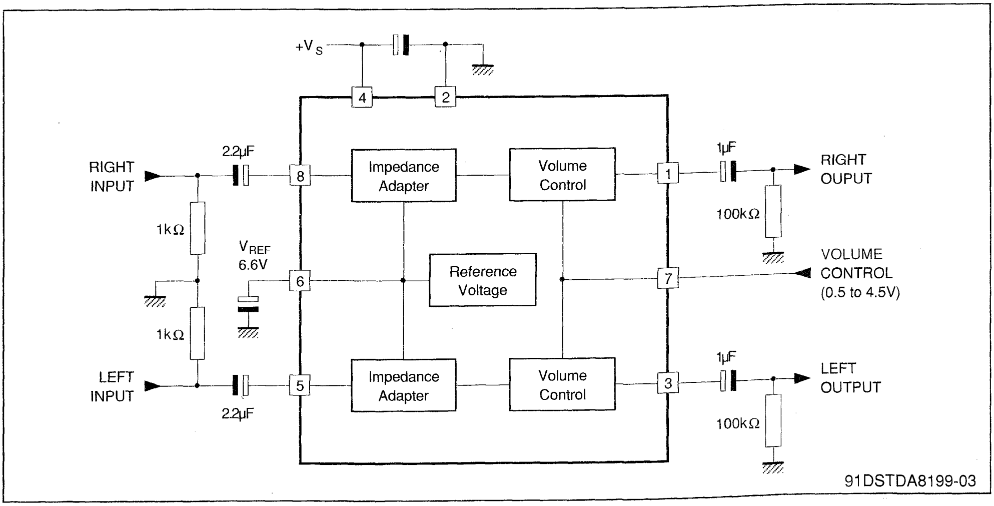
Symbol	Parameter	Value	Unit
V_S	Supply Voltage	16	V
T_{STG}	Storage Temperature	-55 to +125	°C
T_{OP}	Operating Ambient Temperature	0 to +70	°C

ELECTRICAL CHARACTERISTICS

Measured according to the following conditions, unless otherwise specified : $T_{AMB} = 25^{o}C$, $V_S = +12V$.

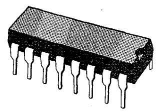
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	10.8	12	13.2	V
I_S	Supply Current ($V_{IN} = 0$, $V_C = 0.5V$)		17		mA
V_R	Reference Voltage	6.5	6.9		V
V_I	Audio Input Amplitude		0.125	0.5	V_{RMS}
THD	Distortion for $V_I = 2V$ at Maximum Volume		0.35	1	%
C_C	Crosstalk between Channels		70		dB
R_I	Audio Input Resistance		22		kΩ
R_O	Audio Output Resistance		0.3	1	kΩ
ΔK	Attenuation Range	70	85		dB
K_{MAX}	Output/Input Gain for Maximum Volume		12		dB
V_C	Voltage Control Range volume minimum volume maximum	 4.5		 0.5	V
OUTPUT	Noise Level (DIN45 405) @ $V_7 = 4.5V$ weighted		 300		μV_{RMS}
$\frac{\Delta K}{\Delta T}$	Volume thermal stability ($K = -30dB$, $0 < T_{AMB} < 60^{o}C$)		0.04		dB/°C

APPLICATION DIAGRAM



POWER SINGLE OPERATIONAL AMPLIFIER

- OUTPUT CURRENT UP TO 500 mA
- OFFSET VOLTAGE NULL CAPABILITY
- SHORT-CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION
- PLASTIC PACKAGE FOR EASY ASSEMBLY



N
DIP16
(Plastic Package)

DESCRIPTION

The TDB7910 is an internally compensated medium power operational amplifier intended for use in those applications requiring load currents of several hundred milliamperes. Applications include servo amplifiers, driver interfaces, precision power comparators and motor speed control.

The amplifier is designed to operate from a single or dual power supplies and the input common-mode range includes the negative supply if balance inputs are tied to the negative supply.

The TDB7910 is thermal overload and short-circuit protected.

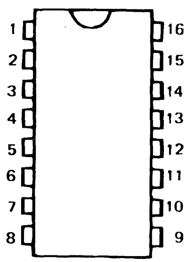
ORDER CODES

Part Number	Temperature Range	Package N
TDB7910	0 °C to + 70 °C	•
Example : TDB7910N		

PIN CONNECTIONS (top view)

DIP16

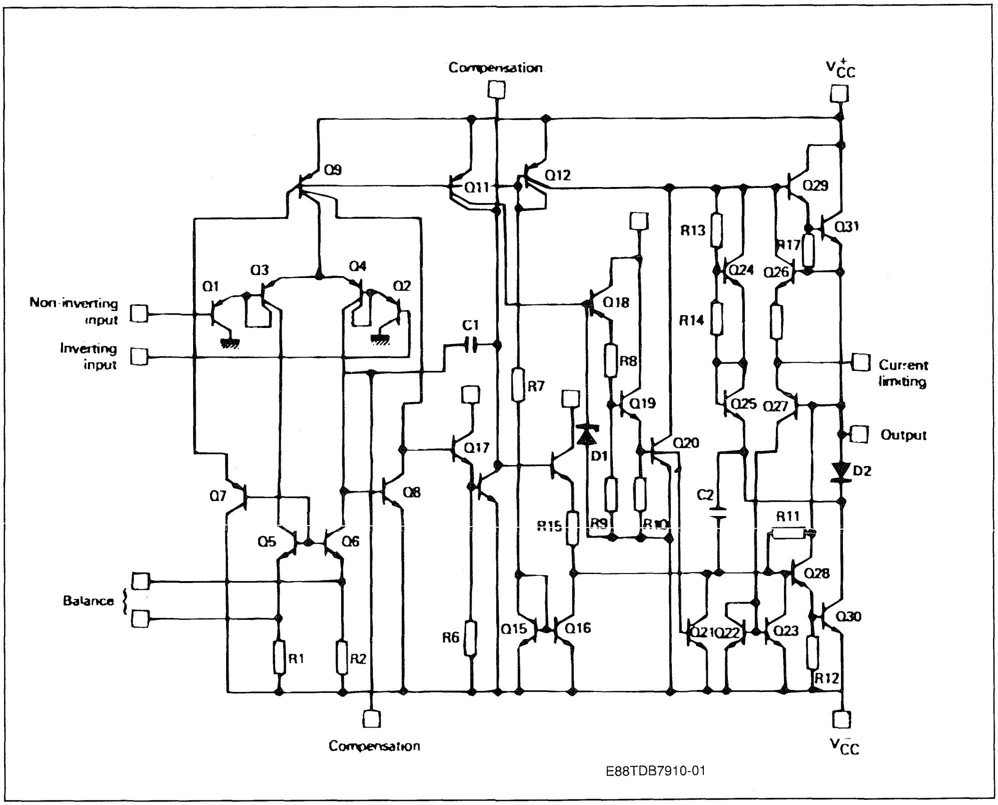
1 - V_{CC}^-
2 - V_{CC}^-
3 -NC
4 - V_{CC}^-
5 - V_{CC}^-
6 - Output
7 - V_{CC}^+
8 - Current limiting



9 - Compensation
10 - Inverting input
11 - Non-inverting input
12 - V_{CC}^-
13 - V_{CC}^-
14 - Balance
15 - Balance
16 - Compensation

E88TDB7910-06

SCHEMATIC DIAGRAM



Case	V_{CC}^{-}	NC	V_{CC}^{+}	Output	Current Limiting	Compensation	Non-Inverting Input	Inverting input	Balance
DIP16	1, 2 4, 5 12, 13	3	7	6	8	9, 16	11	10	1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 18	V
V_I	Input Voltage	± 15	V
V_{ID}	Differential Input Voltage	± 30	V
I_O	Output Current*	0.75	A
P_{tot}	Power Dissipation	7.5	W
T_{oper}	Operating Free-air Temperature Range	0 to + 70	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

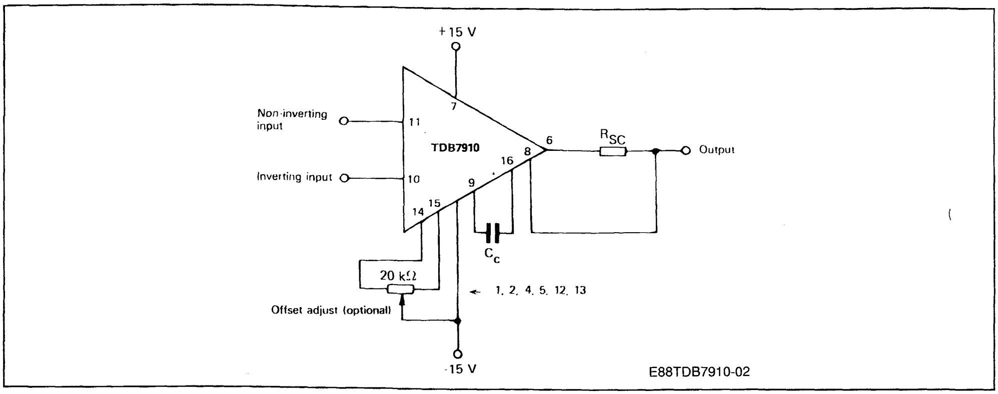
* Under short-circuit conditions, the safe operating area and dc power dissipation limitations must be observed.

ELECTRICAL CHARACTERISTICS

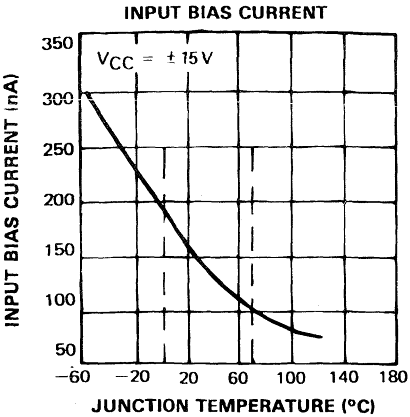
TDB7910 : 0 °C ≤ T_{amb} ≤ + 70 °C, V_{CC} = + 15 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage (R_S ≤ 10 kΩ) T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		2	6 7.5	mV
I_{IO}	Input Offset Current T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		20	200 300	nA
I_{IB}	Input Bias Current T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		80	500 800	nA
A_{VD}	Large Signal Voltage Gain T_{amb} = + 25 °C (R_L = 47 Ω) $T_{min} \leq T_{amb} \leq T_{max}$ (R_L = 2 kΩ)	20 15			V/mV
I^+_{CC}, I^-_{CC}	Supply Currents (no signal) T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$			20 25	mA
V_I	Input Voltage Range	± 12	± 13		V
I_{OS}	Output Circuit Current T_{amb} = + 25 °C, R_{SC} = 1.5 Ω		0.5		A
SVR	Supply Voltage Rejection Ratio			150	µV/V
CMR	Common-mode Rejection Ratio	70			dB
Z_I	Input Impedance (T_{amb} = + 25 °C)	0.3	1		MΩ
V_{OPP}	Output Voltage Swing (R_{SC} = 0, R_L = 47 Ω) T_j = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	± 11.5 ± 10	± 12.5		V
V_{IOR}	Offset Voltage Adjustment Range		± 15		mV
SVO	Slew Rate (R_L = 47 Ω, T_{amb} = + 25 °C, A_V = 1)		0.5		V/µs
GW_R	Small Signal Bandwidth (C_C = 0, T_{amb} = + 25 °C)		1		MHz
RTH	Thermal Resistance		60		°C/W

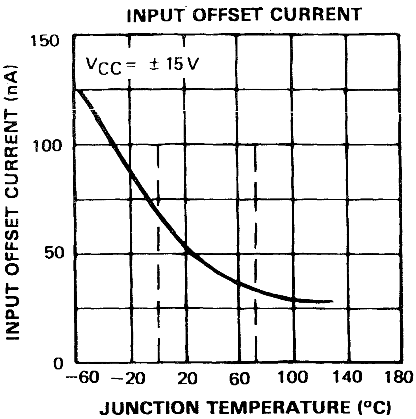
BASIC DIAGRAM



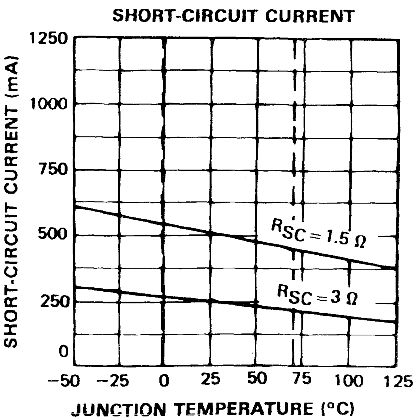
E88TDB7910-02



E88TDB7910-03



E88TDB7910-04

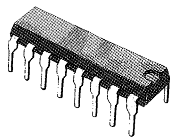


E88TDB7910-05

FM STEREO DECODER

- REQUIRES NO INDUCTORS
- LOW EXTERNAL PART COUNT
- ONLY OSCILLATOR FREQUENCY ADJUSTMENT NECESSARY
- INTEGRAL STEREO/MONAURAL SWITCH WITH HIGH LAMP DRIVING CAPABILITY
- WIDE SUPPLY RANGE: 3V TO 14V
- EXCELLENT CHANNEL SEPARATION MAINTAINED OVER ENTIRE AUDIO FREQUENCY RANGE
- LOW DISTORTION: TYPICALLY 0.3% AT 150mV (RMS) COMPOSITE INPUT SIGNAL
- EXCELLENT SCA REJECTION (76dB TYP.)

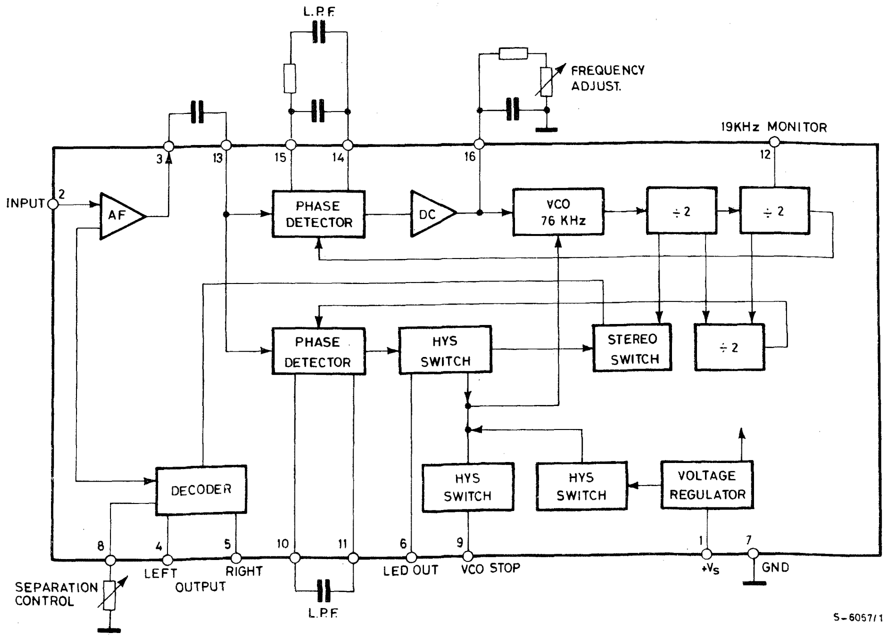
The TEA1330 is a monolithic decoder circuit for FM stereo transmissions. Packaged in a 16-pin DIP, it functions with very few external components and requires no inductors.



DIP-16 Plastic
(0.25)

ORDERING NUMBER: TEA1330

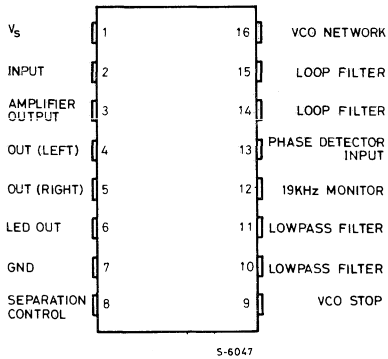
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
I_L	Lamp current	75	mA
P_{tot}	Power dissipation $T_{amb} = 70°C$	800	mW
T_{op}	Operating temperature	-25 to 75	°C
T_{stg}	Storage temperature	-55 to to 150	°C

CONNECTION DIAGRAM
(top view)



THERMAL DATA

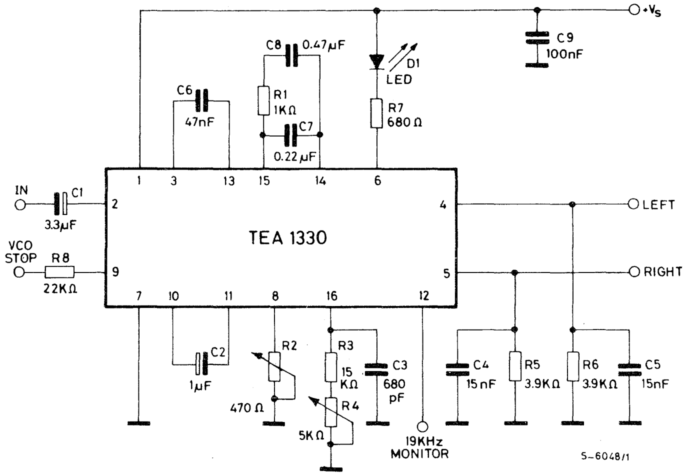
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb} = 25°C, V_s = 6V, V_i = 300 mV-RMS (L + R = 90%, Pilot 10%), f_m = 1 KHz, unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range		3		14	V
I_d	Current drain	Lamp "OFF"		18		mA
V_i	Max standard composite input signal	d = 1%	300			mV (RMS)
V_i	Max mono input signal	d = 1%	300			mV (RMS)
R_i	Input resistance			40		KΩ
Sep	Stereo channel separation	R2 = variable (*)	35	50		dB
		R2 = 270 Ω	25	40		dB
V_o	Audio output voltage			265		mV
CB	Mono channel balance	Pilot tone "OFF"	-2	0	+2	dB
d	Total harmonic distortion	V_{in} = 150 mV (RMS)		0.3		%
UR	Ultrasonic frequency rejection	f = 19 KHz		32		dB
		f = 38 KHz		48		dB
SCA-R	SCA rejection (**)	f = 67 KHz		76		dB
S/N	Signal to noise ratio			80		dB
V_{th}	Muting threshold voltage (pin 9)	ON (VCO stop)		1		V
		OFF		0.8		V
L_{on}	Pilot input level for lamp ON	f = 19 KHz	4	6	9	mV
Hys	Pilot input level hysteresis for lamp turn ON-OFF	f = 19 KHz		3		dB
CR	Capture range			± 7		%

(*) R2 has to be adjusted for best figure of channel separation.
(**) SCA = AUX. SUB. CARRIER.

Fig. 1 - Test circuit



Typical DC Voltages

Pins	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
(V)	6	1.9	1.3	3	3		0	0.18		1.4	1.4	1.2	1.4	1.4	1.4	2.2

Fig. 2 - P.C. board and components layout of the test circuit of fig. 1 (1:1 scale)

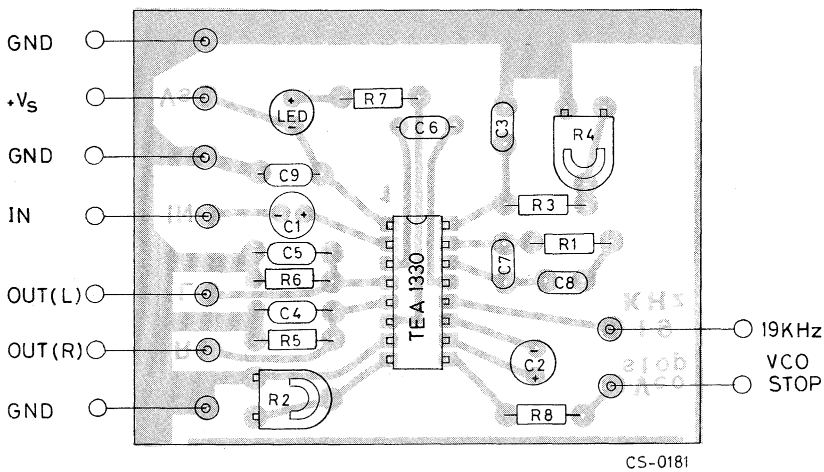


Fig. 3 - Channel separation vs. modulation frequency

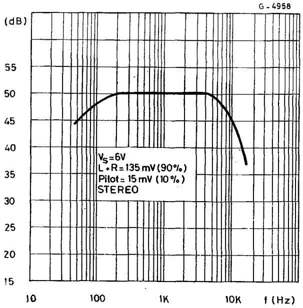


Fig. 4 - Distortion vs. modulation frequency

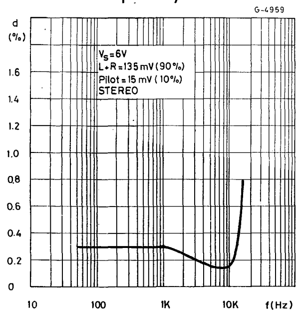


Fig. 5 - Channel separation vs. input level

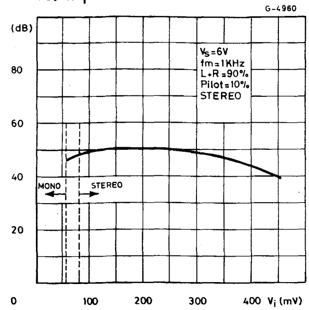


Fig. 6 - Distortion vs. input level

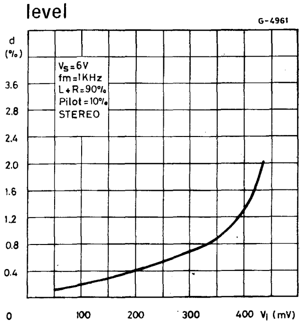


Fig. 7 - Channel separation vs. supply voltage

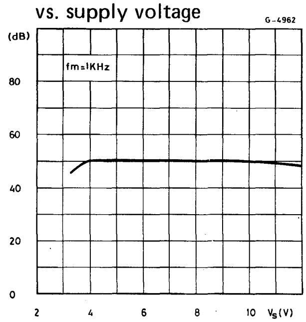
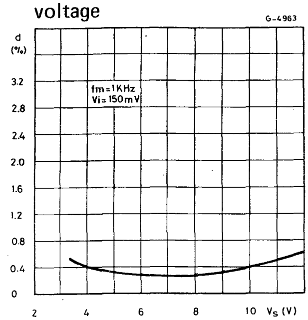


Fig. 8 - Distortion vs. supply voltage



APPLICATION SUGGESTION (see test circuit of fig. 1)

Component	Recommended value	Purpose	Smaller than recommended value	Larger than recommended value
C1	3.3 μF	Input coupling	Poor low frequency response and separation	
C2	1 μF	LPF for stereo switch level detector	Shorter time to switch mono to stereo	Longer time to switch mono to stereo
C3 (*) R3 R4	680 pF 15 KΩ 5 KΩ	Set VCO free running frequency	– High VCO jitter – Wide capture range	Narrower capture range

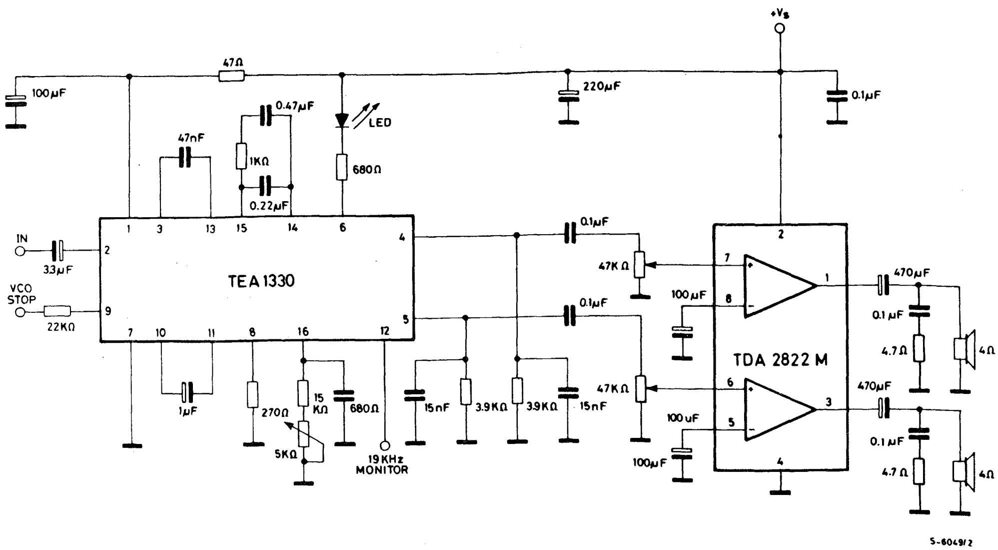
(*) Polyester ± 5%.

APPLICATION SUGGESTION (continued)

Component	Recommended value	Purpose	Smaller than recommended value	Larger than recommended value
C4 R5 (**)	15 nF 3.9 KΩ	Load and deemphasis right channel	Low output voltage	Higher distortion for low V_S
C5 R6 (**)	15 nF 3.9 KΩ	Load and deemphasis left channel	Low output voltage	Higher distortion for low V_S
C6	47 nF	Input PLL coupling	Poor low frequency response and separation	
C7 C8 R1	220 nF 470 nF 1 KΩ	Loop filter	High stereo distortion	Narrower capture range
D1		Stereo indicator		
R7		Sets lamp current	Excess IC dissipation	Dim lamp
R2 (***)	270 Ω	Channel separation		

(**) Deemphasis = 50 µs.
(***) Separation can be improved by trimmer adjustement (470 Ω).

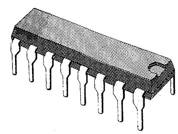
Fig. 9 - Application circuit for portable stereo radio receivers



TEA2025B

STEREO AUDIO AMPLIFIER

- DUAL OR BRIDGE CONNECTION MODES
- FEW EXTERNAL COMPONENTS
- WORKS WITH LOW SUPPLY VOLTAGE: 3V
- HIGH CHANNEL SEPARATION
- NO SHOCK NOISE WHEN SWITCH ON OR OFF
- MAXIMUM VOLTAGE GAIN OF 45dB (ADJUSTABLE WITH EXTERNAL RESISTOR)
- SOFT CLIPPING
- THERMAL PROTECTION
- $3V \leqslant V_{CC} \leqslant 12V$
- $P = 2 \times 1W, V_{CC} = 6V, R_L = 4\Omega$
  $P = 2 \times 2.3W, V_{CC} = 9V, R_L = 4\Omega$
  $P = 2 \times 0.1W, V_{CC} = 3V, R_L = 4\Omega$



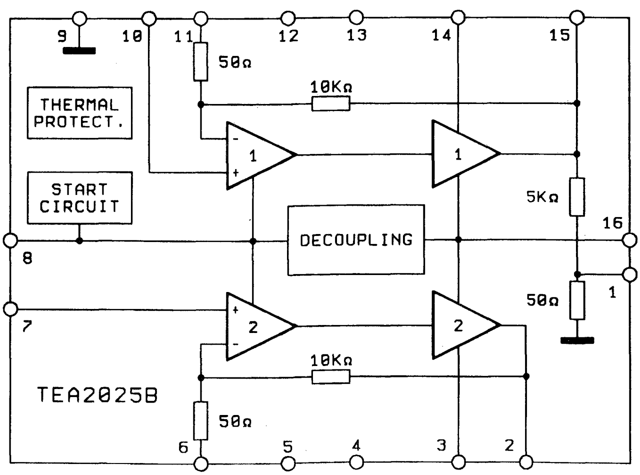
Powerdip
12 +2 +2

ORDERING NUMBER: TEA 2025B

MAXIMUM RATINGS

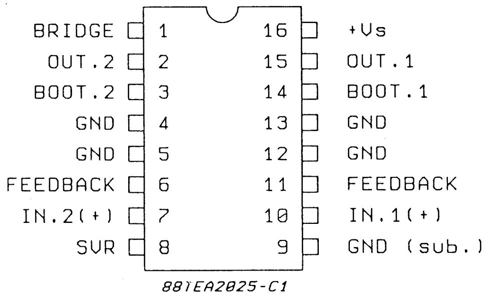
V_S	Supply voltage	15	V
I_O	Output peak current	1.5	A
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-40 to +150	°C

BLOCK DIAGRAM

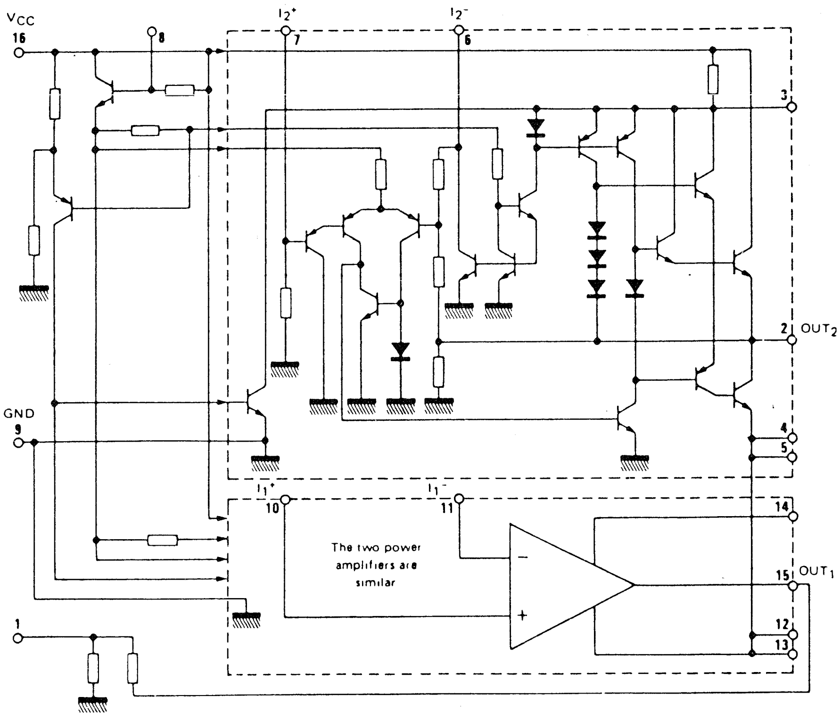


88TEA2025B-B1

PIN CONNECTION



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th(j\text{-}c)}$	Junction-case thermal resistance	15	°C/W
$R_{th(j\text{-}a)}$	Junction-ambient thermal resistance (See note)	60	°C/W

Note: The $R_{th(j\text{-}a)}$ is measured on devices bonded on a 10 x 5 x 0.15cm glass–epoxy substrate with a 35μm thick copper surface of 5 cm².

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} = 9V, Stereo unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_S	Supply voltage		3	–	12	V
I_Q	Quiescent current		–	40	50	mA
V_O	Quiescent output voltage		–	4.5	–	V
A_V	Voltage gain	Stereo	43	45	47	dB
		Bridge	49	51	53	dB
ΔA_V	Voltage gain difference		–	–	± 1	dB
R_j	Imput impedance		–	30	–	kΩ
P_O	Output power	f = 1KHz; d = 10% Stereo – per channel V_{CC} = 9V : R_L = 4Ω	1.7	2.3	–	W
		R_L = 8Ω	–	1.3	–	W
		V_{CC} = 6V : R_L = 4Ω	0.7	1	–	W
		R_L = 8Ω	–	0.6	–	W
		V_{CC} = 3V : R_L = 4Ω	–	0.1	–	W
		Bridge V_{CC} = 9V : R_L = 8Ω	–	4.7	–	W
		V_{CC} = 6V : R_L = 4Ω	–	2.8	–	W
d	Distortion	V_{CC} = 9V; R_L = 4Ω f = 1KHz; P_o = 250 mW Stereo	–	0.3	1.5	%
		Bridge	–	0.5	–	%
SVR	Supply voltage rejection	R_G = 0, A_V = 45 dB, V_{ripple} = 150mV RMS, f_{ripple} = 100Hz	40	46	–	dB
V_n	Input noise voltage	A_V = 200, Bandwidth: 20Hz to 20KHz R_G = 0	–	1.5	3	μV
		R_G = 10kΩ	–	3	6	μV
CT	Cross-talk	R_G = 10kΩ; f = 1KHz; R_L = 4Ω; P_o = 1W	40	55	–	dB

Fig. 1 - Distortion versus output power

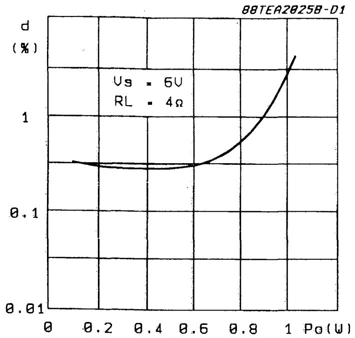


Fig. 2 - Distortion versus output power

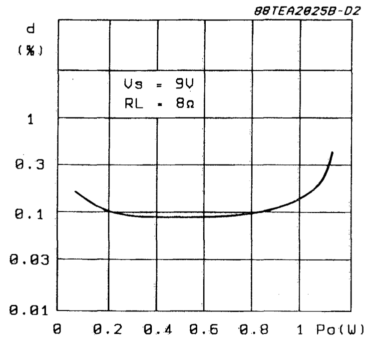


Fig. 3 - Distortion versus output frequency

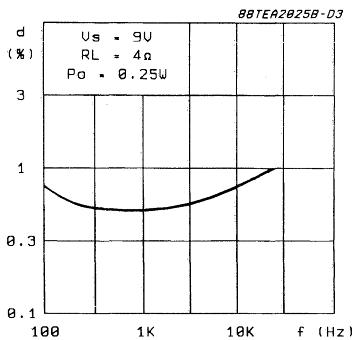


Fig. 4 - Output power/versus supply voltage

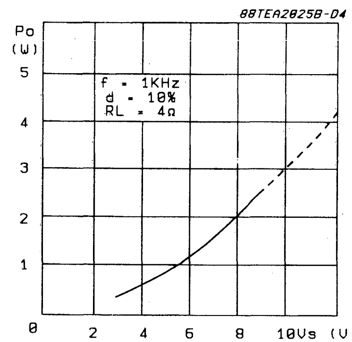


Fig. 5 - Bridge application

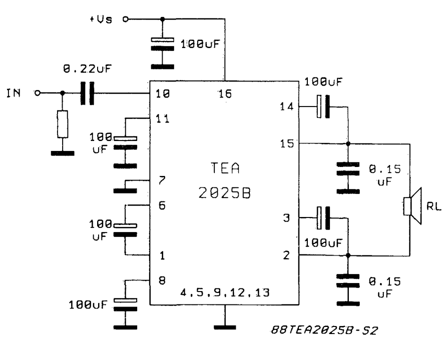
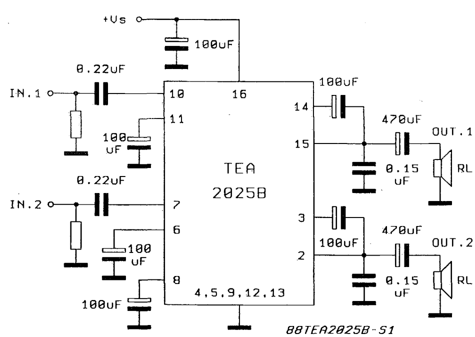


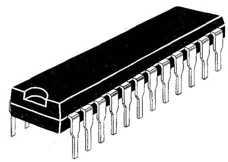
Fig. 6 - Stereo application



BUS-CONTROLLED AUDIO MATRIX

PRELIMINARY DATA

- 5 STEREO INPUTS
- 4 STEREO OUPUTS
- GAIN CONTROL 0/2/4/6DB/MUTE FOR EACH OUTPUT
- CASCADABLE (2 DIFFERRENT ADDRESSES)
- SERIAL BUS CONTROLLED
- VERY LOW NOISE



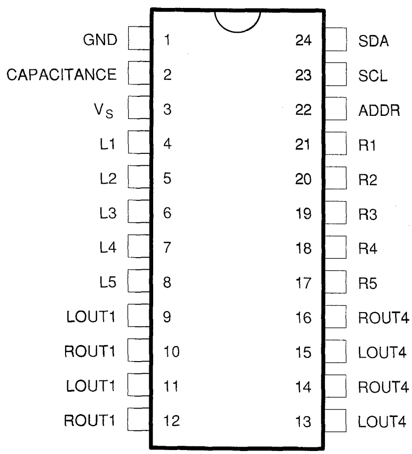
SDIP24
(plastic package)

ORDER CODE : TEA6420

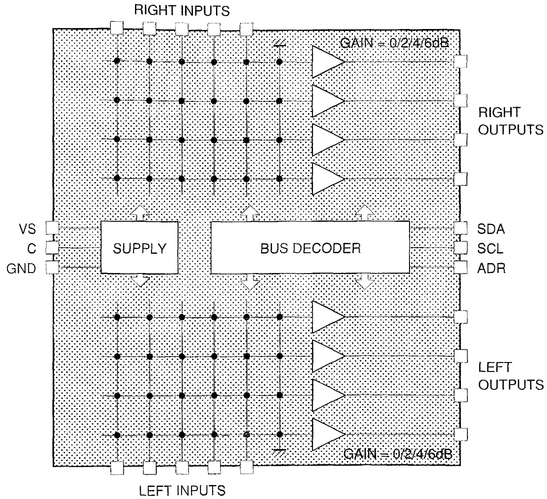
DESCRIPTION

The TEA6420 switches 5 stereo audio on 4 stereo outputs.
All the switching possibities are changed through the I^2C BUS.

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vcc	Supply Voltage	10.2	V
Toper	Operating ambient temperature	- 20 to + 85	°C
Tstg.	Storage Temperature	- 55 to + 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction - ambient thermal resistance	75	°C/W

ELECTICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = 9V$, $R_L = 10k\Omega$, $R_G = 600\Omega$, f = 1kHz (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		8	9	10.2	V
I_S	Supply Current			5	8	mA
SVR	Ripple Rejection	W_{IN} = 500mV_{RMS}, BW = 20 - 20kHz		80		dB
MATRIX						
V_{IN}	Input DC Level			5		V
R_I	Input Resistance		30	50		kΩ
C_S	Channel Separation	W_{IN} = 2V_{RMS}, BW = 20 - 20kHz		90		dB
OUTPUT BUFFER						
V_{OUT}	Output DC Level			5		V
R_{OUT}	Output Resistance			50		Ω

ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25^oC$, $V_S = 9V$, $R_L = 10k\Omega$, $R_G = 600\Omega$, f = 1kHz (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OUTPUT BUFFER (continued)						
e_{NI}	Input Noise	BW = 20 - 20kHz, flat		3		μV
S/N	Signal to Noise Ratio	$V_{IN} = V_{OUT} = 1V_{RMS}$		110		dB
G_{min}	Min. Gain		-1	0	+ 1	dB
G_{max}	Max. Gain		5	6	7	dB
d	Distortion	$V_{IN} = V_{OUT} = 1V_{RMS}$		0.01		%
V_{CL}	Clipping Level	d = 0.3%	2	2.5		V_{RMS}
R_L	Output Load Resistance		2			kΩ
BUS INPUT						
V_{IL}	Input Low Voltage				1	V
V_{IN}	Input High Voltage (pin 24)		4			V
I_I	Input Current		- 10		10	μA
V_O	Output Voltage	I_O = 3mA ; SDA Acknowledge pin			0.4	V
R_{pu}	ADDR Pullup Resistor	Note 1		50		kΩ

Note : 1. R_{pu} is an internal pull-up resistor connected between the address programming pin ADDR and the internal positive supply voltage. Leaving ADDR disconnected or "floating" allows it to become logic 1. Connecting ADDR externally to the GND pin forces it to logic 0.

SOFTWARE SPECIFICATION

1. Chip address

Address	HEX	ADDR
1001 1000	98	0
1001 1010	9A	1

2. Data bytes

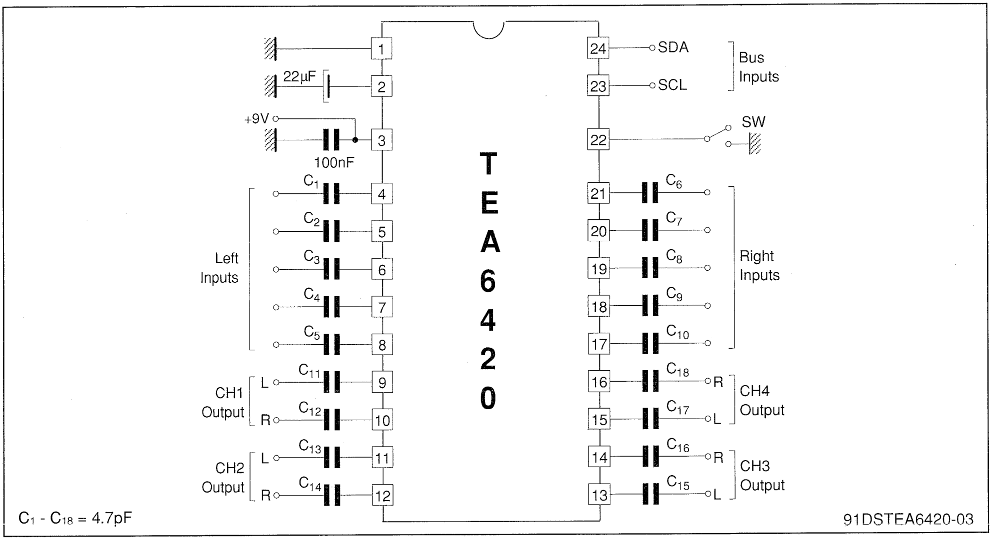
Output select								
X	0	0	G_1	G_0	I_2	I_1	I_0	Output 1
	0	1						Output 2
	1	0						Output 3
	1	1						Output 4
Input select								
X	Q_1	Q0	G_1	G_0	0	0	0	Input 0
					0	0	1	Input 1
					0	1	0	Input 2
					0	1	1	Input 3
					1	0	0	Input 4
					1	0	1	Mute
Gain select								
X	Q_1	Q0	0	0	I_2	I_1	I_0	Gain = 6 dB
			0	1				Gain = 4 dB
			1	0				Gain = 2 dB
			1	1				Gain = 0 dB

X = don't care
MSB is transmitted first

Example : 0 10 01 100 connects outputs 3 with input 4 at a gain of 4dB

The following are selected after power-on reset : input 4 selected for all outputs ; gain = 0dB.

TYPICAL APPLICATION

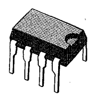


SGS-THOMSON MICROELECTRONICS

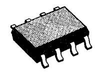
TEB1033
TEF1033 - TEC1033

BIPOLAR DUAL OPERATIONAL AMPLIFIERS

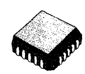
- LOW DISTORTION RATIO
- LOW NOISE
- VERY LOW SUPPLY CURRENT
- LOW INPUT OFFSET CURRENT
- VERY LOW INPUT OFFSET VOLTAGE
- LARGE COMMON-MODE RANGE
- HIGH GAIN
- HIGH OUTPUT CURRENT
- GAIN-BANDWIDTH PRODUCT : 2.5 MHz
- TEMPERATURE DRIFT : 2 μV/°C
- LONG TERM STABILITY : 8 μV/YEAR (for $T_{amb} \leq 50$ °C)
- THE TEB1033 AND TEF1033 ARE PIN TO PIN REPLACEMENT OF THE LS204C AND LS204 RESPECTIVELY



N
Minidip Plastic



D
SO8
(Plastic Micropackage)



GC
LCC20
(Tricecop (LCC))

DESCRIPTION

The TEB1033, TEF1033 and TEC1033 are high performance dual-operational amplifiers intended for active filter applications. The internal phase compensation allows stable operation as voltage follower in spite of their high gain-bandwidth products.

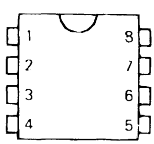
The circuits present very stable electrical characteristics over the entire supply voltage range.

ORDER CODES

Part Number	Temperature Range	Package		
		N	D	GC
TEB1033	0 °C to + 70 °C	•	•	
TEF1033	– 40 °C to + 105 °C	•	•	
TEC1033	– 55 °C to + 125 °C			•
Examples : TEB1033N, TEC1033GC				

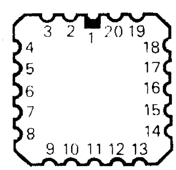
PIN CONNECTIONS (top views)

DIP8/SO8



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

LCC20

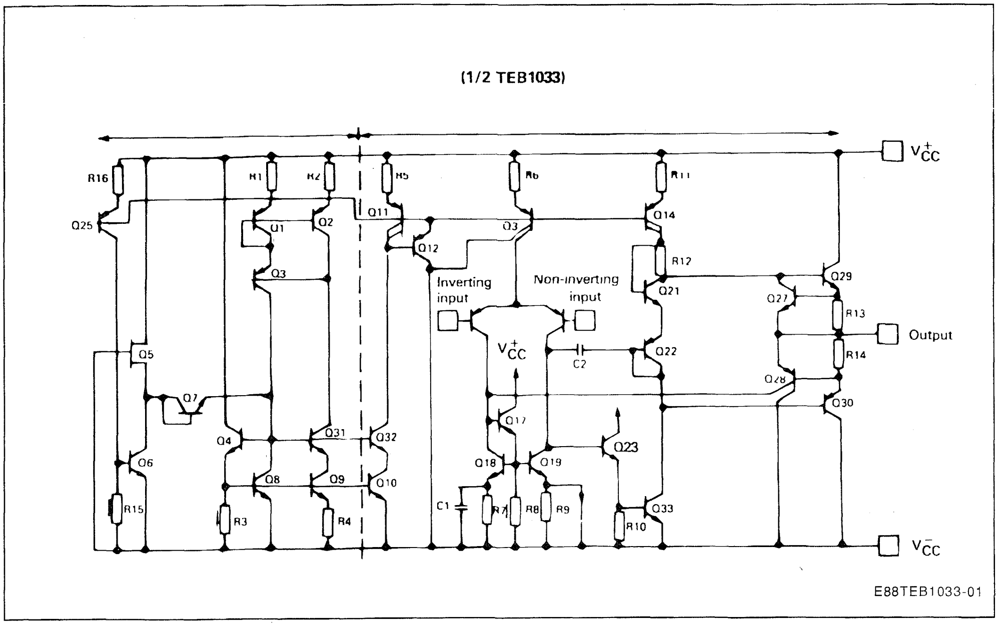


1 - NC
2 - Output 1
3 - NC
4 - NC
5 - Inverting input 1
6 - NC
7 - Non-inverting input 1
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Non-Inverting input 2
13 - NC
14 - NC
15 - Inverting Input 2
16 - NC
17 - Output 2
18 - NC
19 - NC
20 - V_{CC}^+

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 18	V
V_I	Input Voltage	± V_{CC}	V
V_{ID}	Differential Input Voltage	± (V_{CC} –1)	V
P_{tot}	Power Dissipation TEB1033D, TEF1033D TEB1033N TEC1033GC	 400 665 665	mW
T_{oper}	Operating Free-air Temperature Range TEB1033 TEF1033 TEC1033	 0 to + 70 – 40 to + 105 – 55 to + 125	°C
T_{stg}	Storage Temperature Range	– 55 to + 150	°C

BLOCK DIAGRAM



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^+	V_{CC}^-	N. C.
DIP8 **SO8**	1, 7	2, 6	3, 5	8	4	
LCC20	2, 17	5, 15	7, 12	20	10	*

* **LCC20 :** Other pins are not connected.

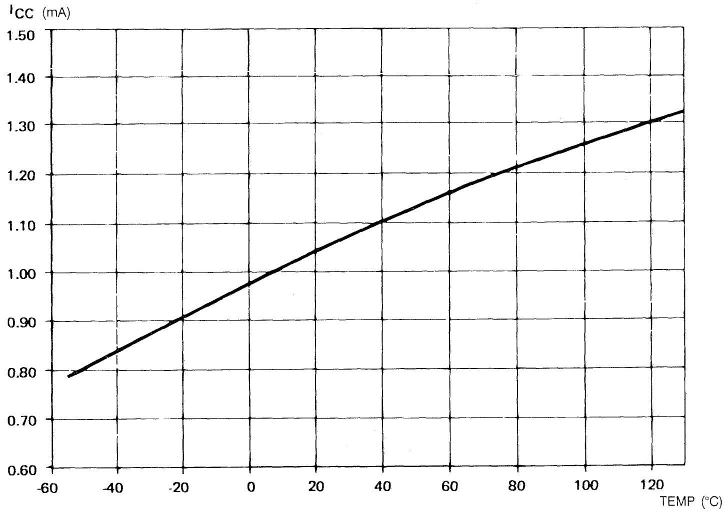
ELECTRICAL CHARACTERISTICS

V_{CC} = ± 15 V (unless otherwise specified)
TEC 1033 : – 55 ≤ T_{amb} ≤ + 125 °C
TEF 1033 : – 40 ≤ T_{amb} ≤ + 105 °C
TEB 1033 : 0 ≤ T_{amb} ≤ + 70 °C

Symbol	Parameter	TEB 1033 TEF 1033 TEC 1033			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage T_{amb} = 25 °C (RS ≤ 10 kΩ) T_{min} ≤ T_{amb} ≤ T_{max}		 0.3	 1 3	mV
DV_{IO}	Input Offset Voltage Drift		2		μV/°C
I_{IO}	Input Offset Current T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		 5	 20 40	nA
I_{IB}	Input Bias Current T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		 50	 100 200	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2 kΩ, V_O = ± 10 V) T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}	 100 100	 300		V/mV
SVR	Supply Voltage Rejection Ratio DV_{CC} from ± 15 V to ± 4 V T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}	 100 100	 110		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		 1	 1.5 2	mA
V_I	Input Voltage Range T_{amb} = 25 °C	– 12		+ 12	V
CMR	Common Mode Rejection Ratio (R_S ≤ 10 kΩ, V_I = ± 10 V) T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}	 100 100	 110		dB
I_{os}	Output Short-circuit Current T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}	 10 10	 23	 40 40	mA
± V_{opp}	Output Voltage Swing T_{amb} = 25 °C R_L = 2 kΩ T_{min} ≤ T_{amb} ≤ T_{max} R_L = 2 kΩ V_{CC} = ± 4 V, R_L = 2 KΩ V_{CC} = ± 6 V, R_L = 600 Ω	 13 12 2.8 4.6	 14 3		V
S_{vo}	Slew-rate (V_I = ± 10 V, R_L = 2 kΩ, C_L ≤ 100 pF, T_{amb} = 25 °C, unity gain)	0.6	1	3	V/μs
GBP	Gain Bandwidth Product (f = 100 KHz, T_{amb} = 25 °C, V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	1.8	2.5	3.2	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		1		MΩ

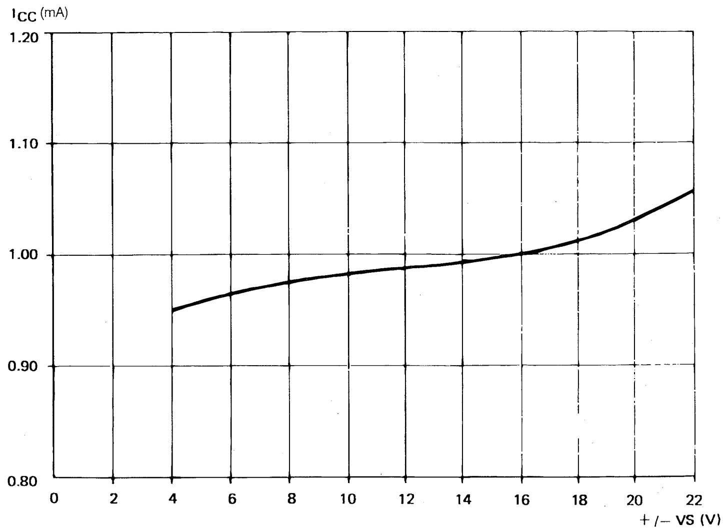
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	TEB 1033 TEF 1033 TEC 1033			Unit
		Min.	Typ.	Max.	
THD	Total Harmonic Distortion (f = 1KHz, A_v = 20 dB, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.008	0.05	%
V_n	Equivalent Input Noise Voltage (f = 1 KHz) R_S = 50 Ω R_S = 1 kΩ R_S = 10 kΩ		8 10 18	15	nV/√Hz
V_{OPP}	Large Signal Voltage Swing R_L =10 kΩ, f = 10 KHz	26	28		V
φM	Phase Margin		45		Degrees
V_{o1}/V_{o2}	Channel Separation	100	120		dB



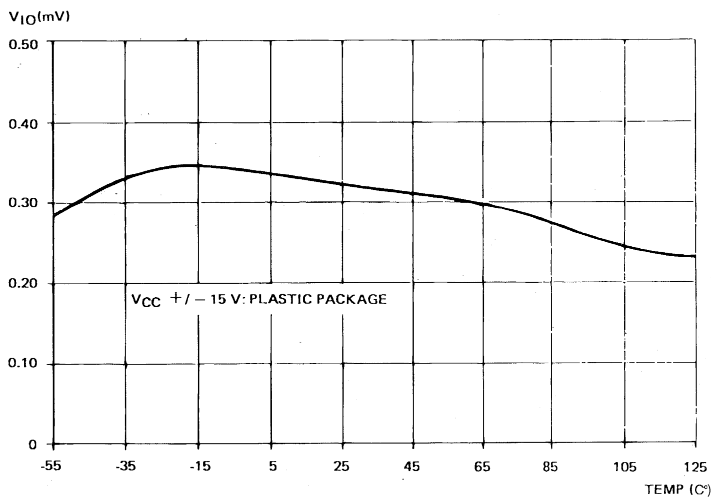
SUPPLY CURRENT VS. AMBIENT TEMPERATURE

E88TEB1033-02



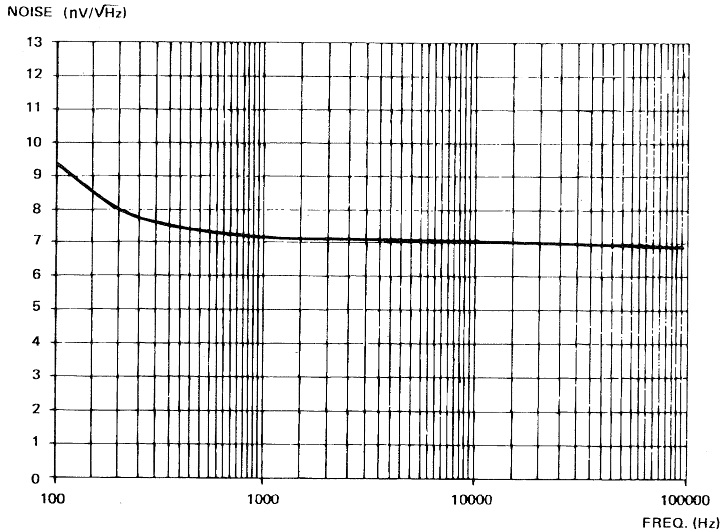
SUPPLY CURRENT VS. SUPPLY VOLTAGE

E88TEB1033-03



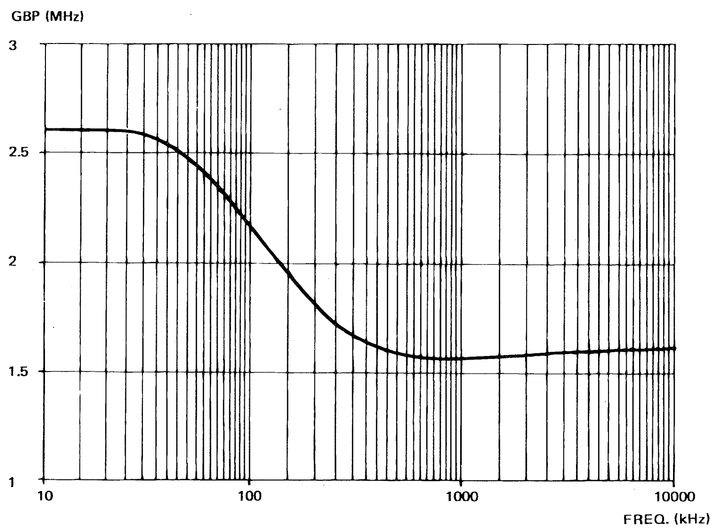
OFFSET VOLTAGE VS. AMBIENT TEMPERATURE

E88TEB1033-04



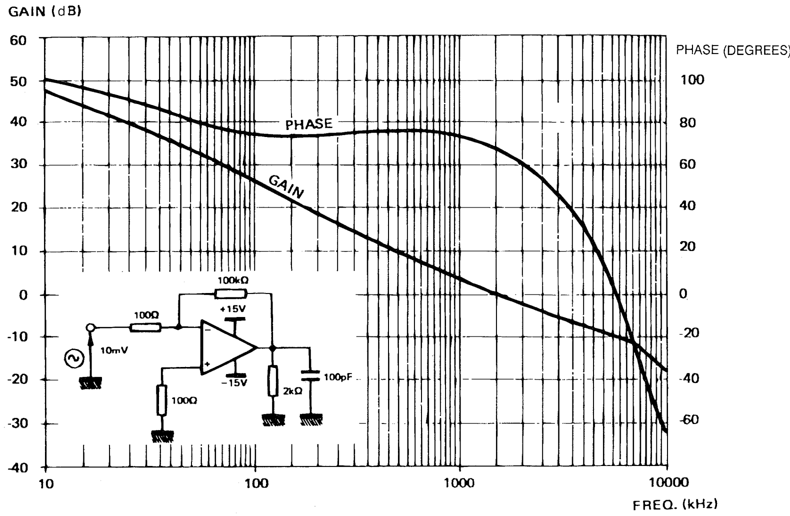
TOTAL INPUT NOISE VS. FREQUENCY

E88TEB1033-05



GAIN BANDWIDTH PRODUCT VS. FREQUENCY

E88TEB1033-06

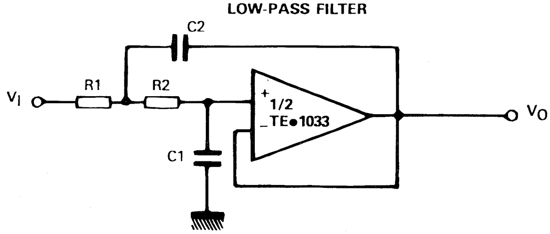


BODE PLOT

E88TEB1033-07

TYPICAL APPLICATION

LOW-PASS FILTER



E88TEB1033-08

$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

$\omega_c = 2\pi f_c$, with f_c = cutt-off frequency

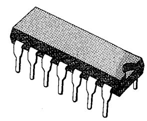
ξ = damping factor

SGS-THOMSON MICROELECTRONICS

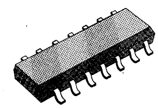
TEB4033
TEF4033 - TEC4033

BIPOLAR QUAD OPERATIONAL AMPLIFIERS

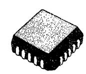
- LOW DISTORTION RATIO
- LOW NOISE
- VERY LOW SUPPLY CURRENT
- LOW INPUT OFFSET CURRENT
- VERY LOW INPUT OFFSET VOLTAGE
- LARGE COMMON-MODE RANGE
- HIGH GAIN
- HIGH OUTPUT CURRENT
- GAIN-BANDWIDTH PRODUCT : 2.5 MHz
- TEMPERATURE DRIFT : 2 µV/°C
- LONG TERM STABILITY : 8 µV/YEAR (for $T_{amb} \leq 50$ °C)
- THE TEB4033 AND TEF4033 ARE PIN TO PIN REPLACEMENT OF THE LS404C AND LS404 RESPECTIVELY



N
DIP14
(Plastic Package)
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)



GC
LCC20
(Tricecop (LCC))

DESCRIPTION

The TEB4033, TEF4033 and TEC4033 are high performance quad-operational amplifiers intended for active filter applications. The internal phase compensation allows stable operation as voltage follower in spite of their high gain-bandwidth products.

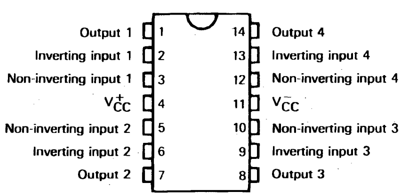
The circuits present very stable electrical characteristics over the entire supply voltage range.

ORDER CODES

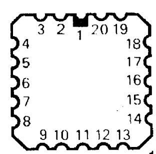
Part Number	Temperature Range	Package		
		N	D	GC
TEB4033	0 °C to + 70 °C	•	•	
TEF4033	– 40 °C to + 105 °C	•	•	
TEC4033	– 55 °C to + 125 °C			•
Examples : TEB4033N, TEC4033GC				

PIN CONNECTIONS (top views)

DIP14/CERDIP14
SO14



LCC20

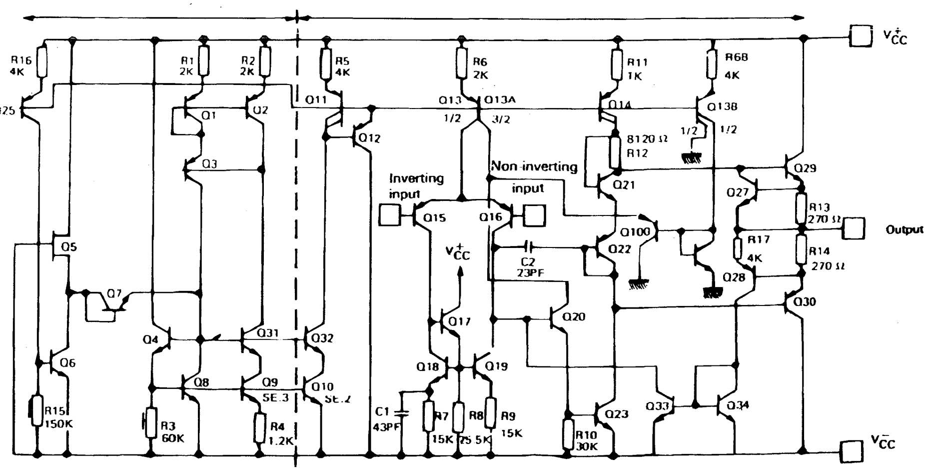


1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - NC
6 - V^{+}_{CC}
7 - NC
8 - Non-inverting input 2
9 - Inverting input 2
10 - Output 2
11 - NC
12 - Output 3
13 - Inverting input 3
14 - Non-inverting input 3
15 - NC
16 - V^{-}_{CC}
17 - NC
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 18	V
V_I	Input Voltage	± V_{CC}	V
V_{ID}	Differential Input Voltage	± (V_{CC} –1)	V
P_{tot}	Power Dissipation TEB4033D, TEF4033D TEB4033N, TEF4033N TEC4033GC	 400 665 665	mW
T_{oper}	Operating Free-air Temperature Range TEB4033 TEF4033 TEC4033	 0 to + 70 – 40 to + 105 – 55 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

BLOCK DIAGRAM



E88TEB4033-01

Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^+	V_{CC}^-	N. C.
DIP14 CERDIP14 SO14	1, 7 8, 14	2, 6 9, 13	3, 5 10, 12	4	11	
LCC20	2, 10 12, 20	3, 9 13, 19	4, 8 14, 18	6	16	*

* **LCC20 :** Other pins are not connected.

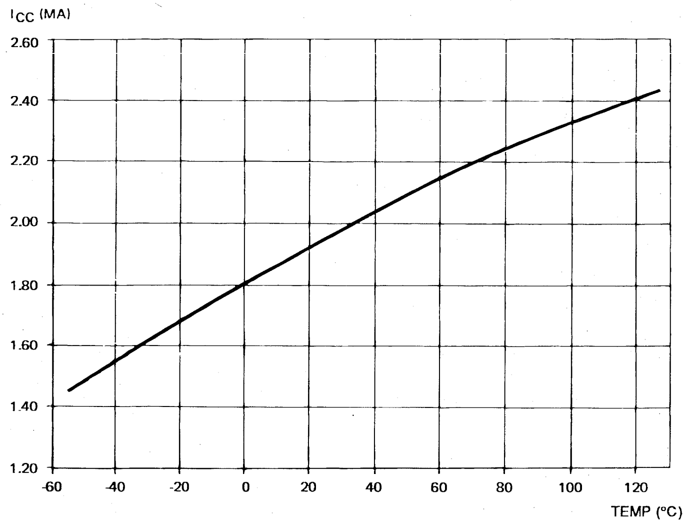
ELECTRICAL CHARACTERISTICS

V_{CC} = ± 15 V (unless otherwise specified)
TEC 4033 : – 55 ≤ T_{amb} ≤ + 125 °C
TEF 4033 : – 40 ≤ T_{amb} ≤ + 105 °C
TEB 4033 : 0 ≤ T_{amb} ≤ + 70 °C

Symbol	Parameter	TEB 4033 TEF 4033 TEC 4033			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage T_{amb} = 25 °C (R_S ≤ 10 kΩ) T_{min} ≤ T_{amb} ≤ T_{max}		 0.3	 1 3	mV
DV_{IO}	Input Offset Voltage Drift		2		µV/°C
I_{IO}	Input Offset Current T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		 5	 20 40	nA
I_{IB}	Input Bias Current T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		 50	 100 200	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2 kΩ, V_O = ± 10 V) T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}	 100 100	 300		V/mV
SVR	Supply Voltage Rejection Ratio DV_{CC} from ± 15 V to ± 4 V T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}	 100 100	 110		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}		 2	 3 4	mA
V_I	Input Voltage Range T_{amb} = 25 °C	 – 12		 + 12	V
CMR	Common Mode Rejection Ratio (R_S ≤ 10 kΩ, V_I = ± 10 V) T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}	 100 100	 110		dB
Ios	Output Short-circuit Current T_{amb} = 25 °C T_{min} ≤ T_{amb} ≤ T_{max}	 10 10	 23	 40 40	mA
± V_{opp}	Output Voltage Swing T_{amb} = 25 ° C R_L = 2 kΩ T_{min} ≤ T_{amb} ≤ T_{max} R_L = 2 kΩ V_{CC} = ± 4 V, R_L = 2 kΩ V_{CC} = ± 6 V, R_L = 600 Ω	 13 12 2.8 4.6	 14 3		V
S_{vo}	Slew-rate (V_I = ± 10 V, R_L = 2 kΩ C_L ≤ 100 pF, T_{amb} = 25°C, unity gain)	0.6	1	3	V/µs
GBP	Gain Bandwidth Product (f = 100 KHz, T_{amb} = 25 °C, V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	1.8	2.5	3.2	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		1		MΩ

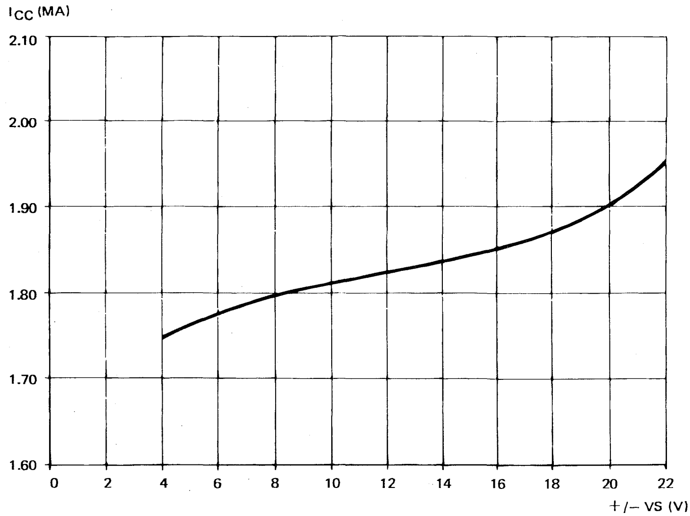
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	TEB 4033 TEF 4033 TEC 4033			Unit
		Min.	Typ.	Max.	
THD	Total Harmonic Distortion (f = 1KHz, A_v = 20 dB, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.008	0.05	%
V_n	Equivalent Input Noise Voltage (f = 1 KHz) R_S = 50 Ω R_S = 1 kΩ R_S = 10 kΩ		8 10 18	15	nV/√Hz
V_{OPP}	Large Signal Voltage Swing R_L = 10 kΩ, f = 10 KHz	26	28		V
φM	Phase Margin		45		Degrees
V_{o1}/V_{o2}	Channel Separation	100	120		dB



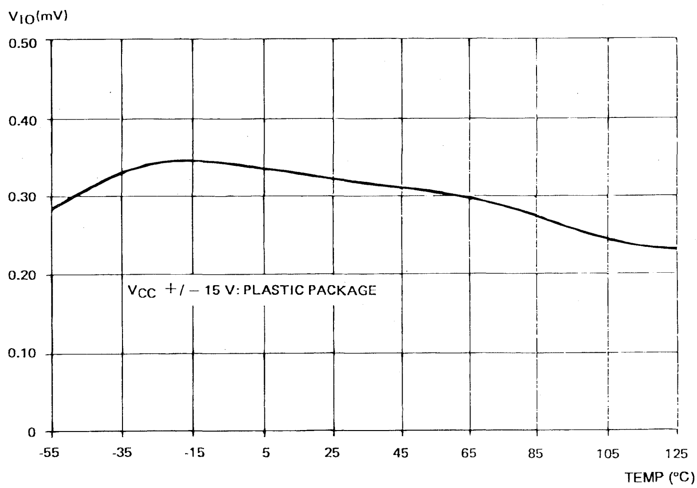
SUPPLY CURRENT VS. AMBIENT TEMPERATURE

E88TEB4033-02



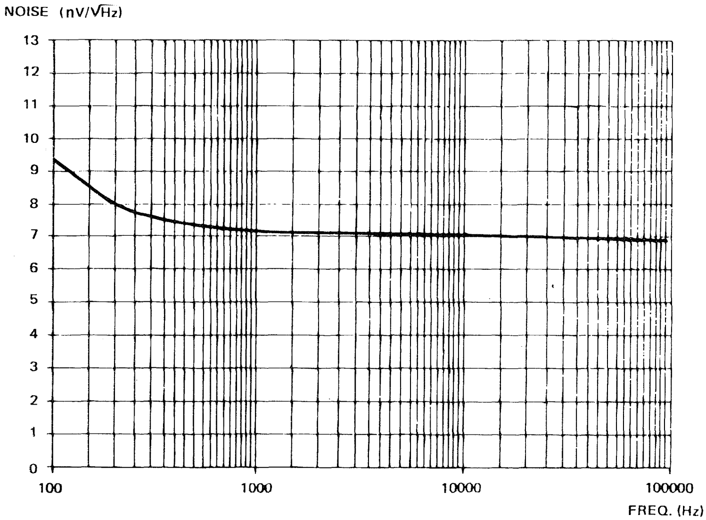
SUPPLY CURRENT VS. SUPPLY VOLTAGE

E88TEB4033-03



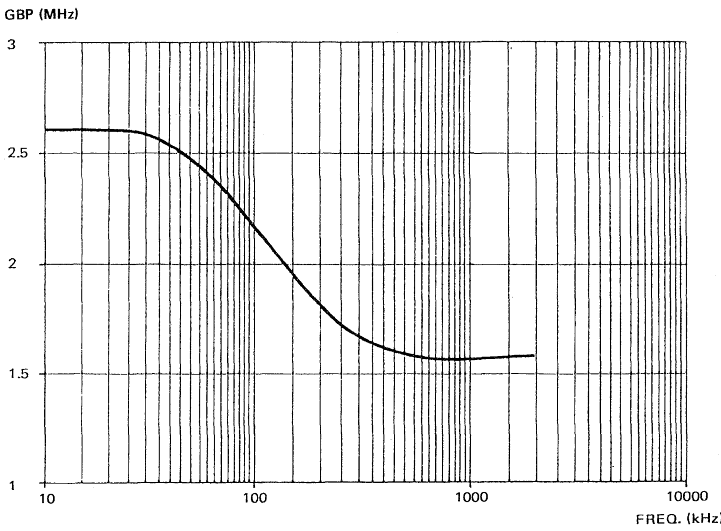
OFFSET VOLTAGE VS. AMBIENT TEMPERATURE

E88TEB4033-04



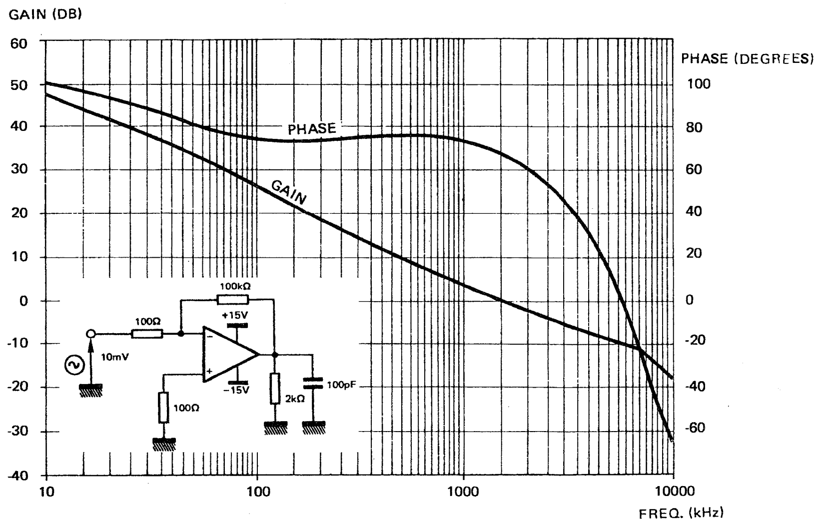
TOTAL INPUT NOISE VS. FREQUENCY

E88TEB4033-05



GAIN BANDWIDTH PRODUCT VS. FREQUENCY

E88TEB4033-06

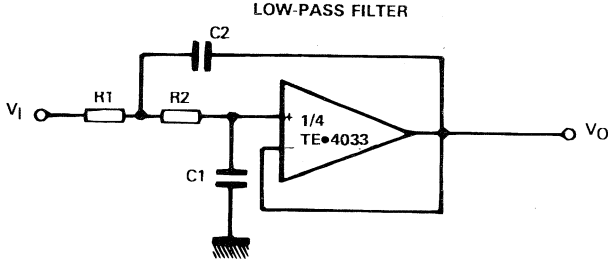


BODE PLOT

E88TEB4033-07

TYPICAL APPLICATION

LOW-PASS FILTER



E88TEB4033-08

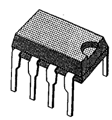
$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_C} + \frac{S^2}{\omega_C^2}}$$

$\omega_C = 2\pi f_C$, with f_C = cutt-off frequency

ξ = damping factor

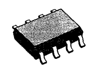
PROGRAMMABLE SINGLE CMOS OP-AMPs

- OFFSET NULL CAPABILITY (by external compensation)
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- THE TRANSFER FUNCTION IS LINEAR
- CONSUMPTION CURRENT AND DYNAMIC PARAMETERS ARE STABLE REGARDING THE VOLTAGE POWER SUPPLY VARIATIONS
- DYNAMIC CHARACTERISTICS ADJUSTABLE BY I_{SET}
- VERY LARGE I_{SET} RANGE
- PIN TO PIN COMPATIBLE WITH SINGLE OPERATIONAL AMPLIFIER (UA776)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N

Minidip Plastic



D

SO8

(Plastic Micropackage)

J

CERDIP8

(Cerdip Package)

DESCRIPTION

The TS271 is low cost, low power single operational amplifier designed to operate with single or dual supplies. This operational amplifiers uses the SGS-THOMSON silicon gate LIN MOS process giving it an excellent consumption-speed ratio. This amplifier is ideally suited for low consumption applications.

The power supply is externally programmable with a resistor connected between pins 8 and 4. It allows to choose the best consumption-speed ratio and the consumption can be minimized according to the required speed. These devices are specified for the following I_{SET} current values : 1.5µA, 25µA, 130µA.

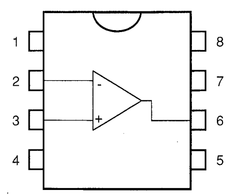
The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS271C/AC/BC	0°C to + 70°C	•	•	•
TS271I/AI/BI	- 40°C to + 105°C	•	•	•
TS271M/AM/BM	- 55°C to + 125°C	•	•	•
Example : TS271ACN				

PIN CONNECTIONS (Top view)

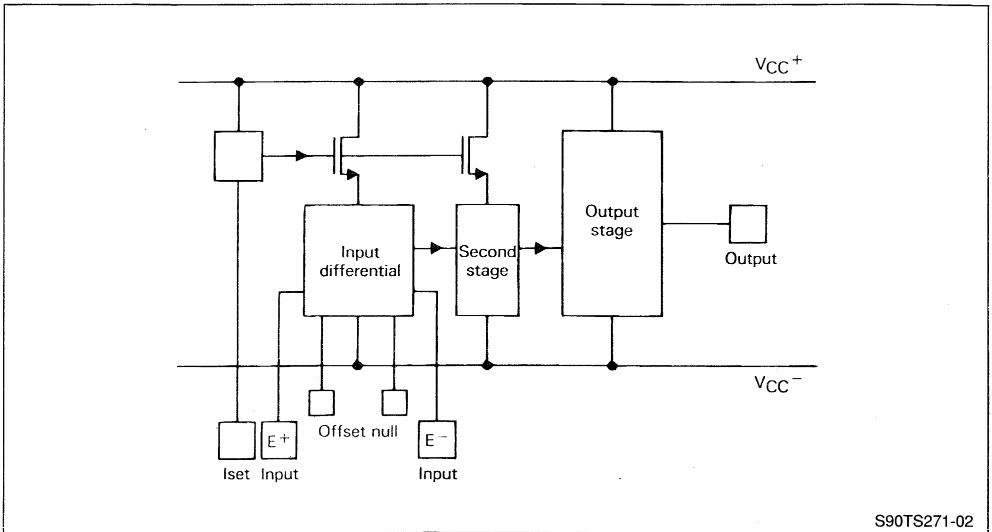
DIP8 - CERDIP 8 - SO8



1 - Offset Null
2 - Inverting Input
3 - Non-inverting Input
4 - V_{CC}^-
5 - Offset Null 2
6 - Output
7 - V_{CC}^+
8 - I_{SET}

S90TS271-01

BLOCK DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS271C/AC/BC TS271I/AI/BI TS271M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

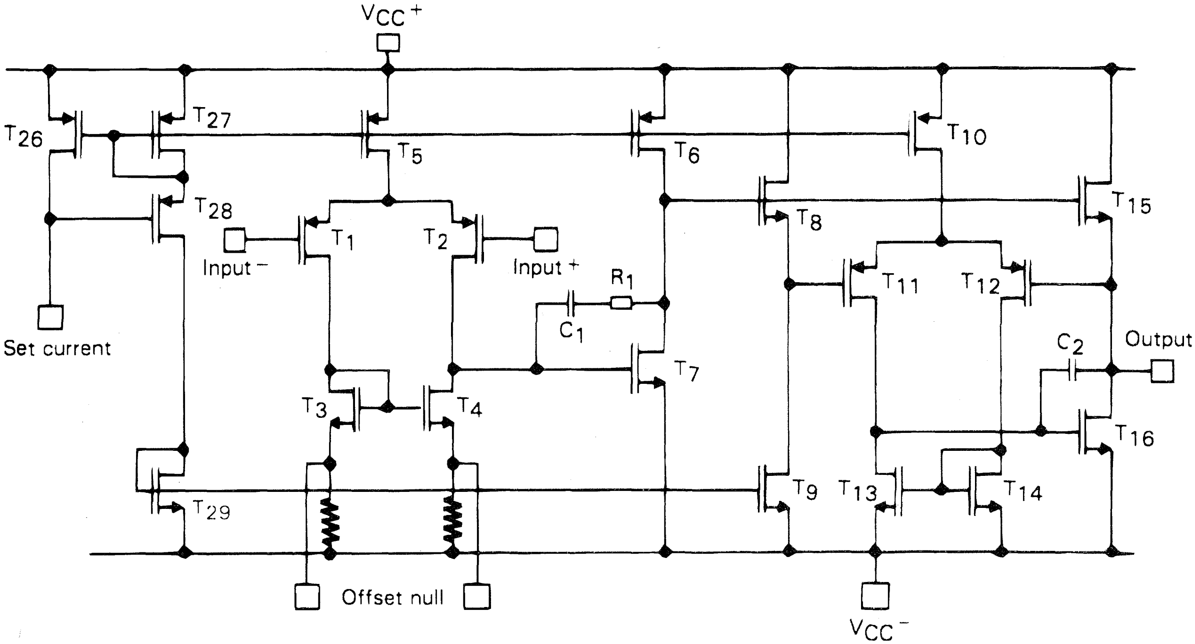
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3* to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

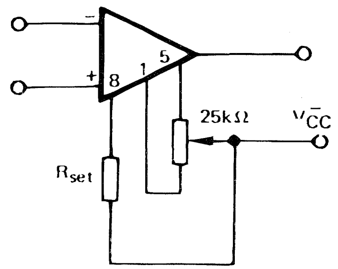
* Selected devices only.

SCHEMATIC DIAGRAM



S90TS271-03

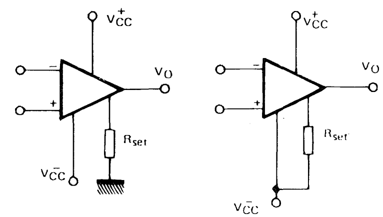
OFFSET VOLTAGE NULL CIRCUIT



S90TS271-04

OFFSET COMPENSATION GUARANTEED FOR TS271BCX (I_{SET} > 25µA), TS271ACX (I_{SET} > 90µA)

RESISTOR BIASING

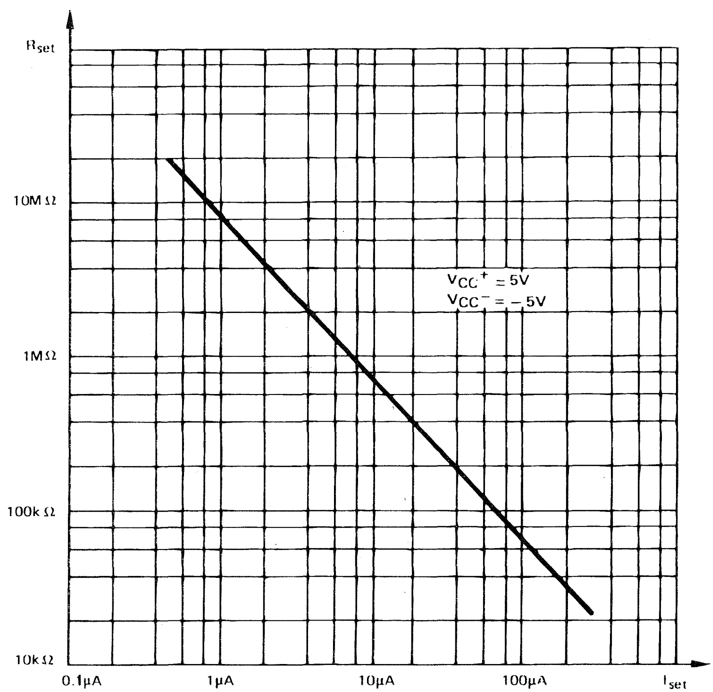


S90TS271-05

R_{SET} CONNECTED TO GROUND

R_{SET} CONNECTED TO V_{CC}^- (R_{SET} VALUE :SEE FIG.1)

Figure 1 : R_{SET} Connected to V_{CC}^-.



S90TS271-06

ELECTRICAL CHARACTERISTICS FOR I_{SET} = 1.5μA

$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{AMB} = 25^oC$ (unless otherwise specified)

Symbol	Parameter	TS271C/AC/BC			TS271I/AI/BI TS271M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_i = 0V$ TS271C/I/M TS271AC/AI/AM TS271BC/BI/BM $T_{MIN} \leq T_{AMB} \leq T_{MAX}$ TS271C/I/M TS271AC/AI/AM TS271BC/BI/BM		 1.1 0.9 0.25	 10 5 2 12 6.5 3		 1.1 0.9 0.25	 10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		0.7			0.7		μV/°C
I_{io}	Input Offset Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		 1	 100		 1	 200	pA
I_{ib}	Input Bias Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		 1	 150		 1	 300	pA
V_{OH}	High Level Output Voltage $V_i = 10mV$, $R_L = 1M\Omega$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 8.8 8.7	 9		 8.8 8.6	 9		V
V_{OL}	Low Level Output Voltage (Vi = - 10mV)			50			50	mV
A_{vd}	Large Signal Voltage Gain $V_o = 1V$ to $6V$, $R_L = 1M\Omega$, $V_i = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 30 20	 100		 30 20	 100		V/mV
GBP	Gain Bandwidth Product ($A_v = 40dB$, $R_L = 1M\Omega$, $C_L = 100pF$, $f_{in} = 10$ kHz)		 0.1			 0.1		MHz
CMR	Common Mode Rejection Ratio $V_o = 1.4V$, $V_i = 1V$ to $7.4V$	 60	 80		 60	 80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ =$ 5V to 10V, $V_o = 1.4V$	 60	 80		 60	 80		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		 10	 15 17		 10	 15 18	μA
I_o	Output Short Circuit Current $V_i = 10mV$, $V_o = 0V$	 45	 60	 85	 45	 60	 85	mA
I_{sink}	Output Sink Current Vi = - 10mV, $V_o = V_{CC}$	 35	 45	 65	 35	 45	 65	mA
S_{vo}	Slew-Rate at Unity Gain $R_L = 1M\Omega$, $C_L = 100pF$		 0.04			 0.04		V/μs
∅ m	Phase Margin at Unity Gain $A_v = 40$ dB, $R_L = 1M\Omega$ $C_L = 10pF$ $C_L = 100pF$		 35 10			 35 10		degrees
K_{ov}	Overshoot Factor $C_L = 10pF$ $C_L = 100pF$		 40 70			 40 70		%
V_n	Equivalent Input Noise Voltage f = 1kHz, $R_S = 10\Omega$		 68			 68		$nV/\sqrt{Hz}$

TYPICAL CHARACTERISTICS FOR $I_{SET} = 1.5\mu A$

Figure 2 : Supply Current (each amplifier) versus Supply Voltage.

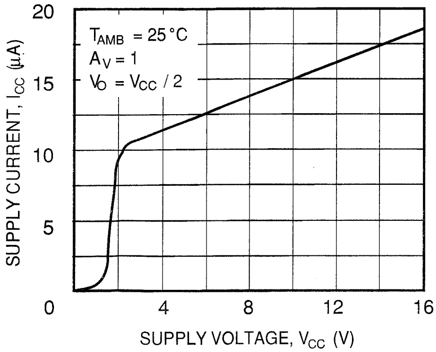


Figure 3 : Input Bias Current versus Free Air Temperature.

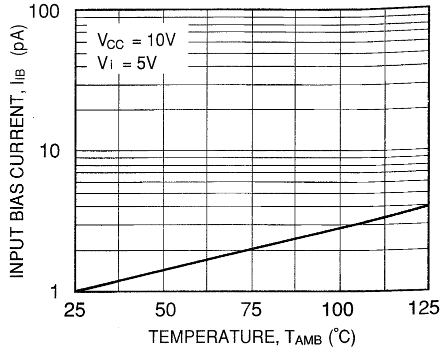


Figure 4a : High Level Output Voltage versus High Level Output Current.

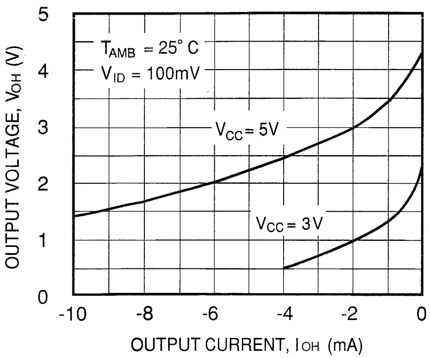


Figure 4b : High Level Output Voltage versus High Level Output Current.

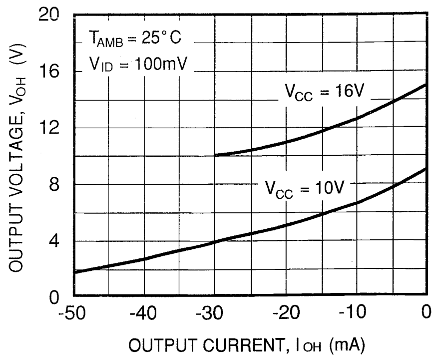


Figure 5a : Low Level Output Voltage versus Low Level Output Current.

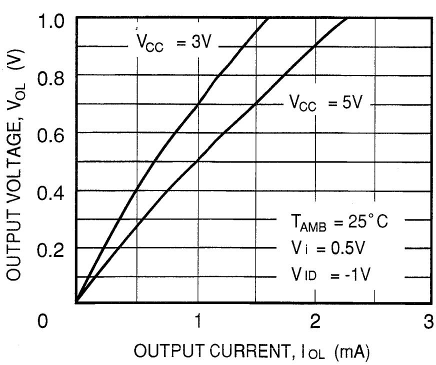
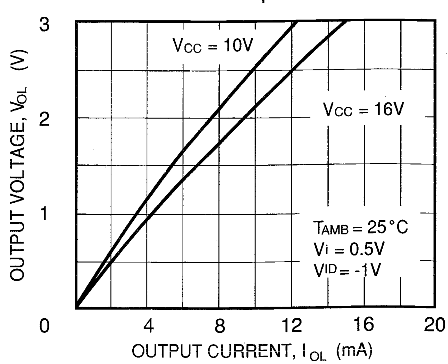


Figure 5b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS FOR I_{SET} = 1.5μA (continued)

Figure 6 : Open Loop Frequency Response and Phase Shift.

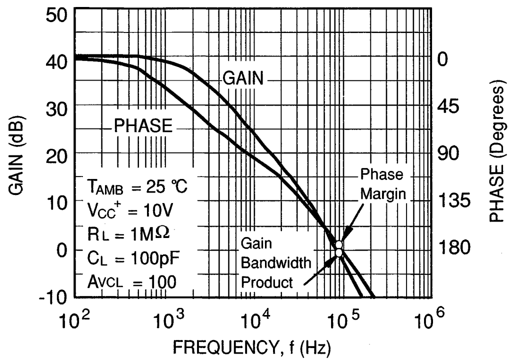


Figure 7 : Gain Bandwidth Product versus Supply Voltage.

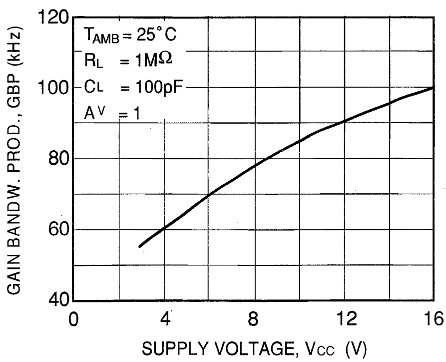


Figure 8 : Phase Margin versus Supply Voltage.

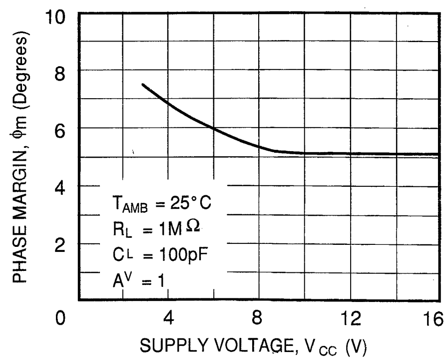


Figure 9 : Phase Margin versus Capacitive Load.

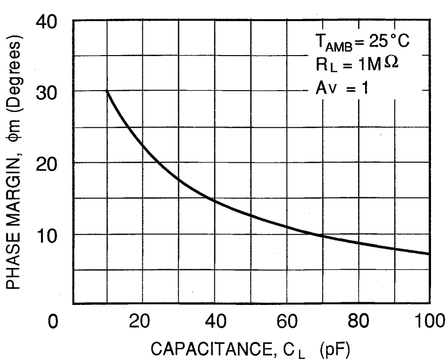
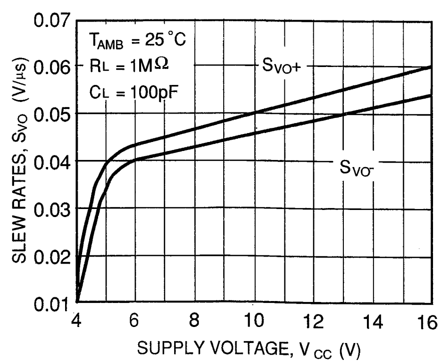


Figure 10 : Slew Rates versus Supply Voltage.



ELECTRICAL CHARACTERISTICS FOR I_{SET} = 25µA

V_{CC}^+ = + 10V, V_{CC}^- = 0V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	TS271C/AC/BC			TS271I/AI/BI TS271M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_O = 1.4V, V_i = 0V TS271C/I/M TS271AC/AI/AM TS271BC/BI/BM $T_{MIN} \le T_{AMB} \le T_{MAX}$ TS271C/I/M TS271AC/AI/AM TS271BC/BI/BM		 1.1 0.9 0.25	 10 5 2 12 6.5 3		 1.1 0.9 0.25	 10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5V, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		 1	 100		 1	 200	pA
I_{ib}	Input Bias Current V_i = 5V, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		 1	 150		 1	 300	pA
V_{OH}	High Level Output Voltage V_i = 10mV, R_L = 100kΩ $T_{MIN} \le T_{AMB} \le T_{MAX}$	 8.7 8.6	 8.9		 8.7 8.5	 8.9		V
V_{OL}	Low Level Output Voltage (Vi = - 10mV)			50			50	mV
A_{vd}	Large Signal Voltage Gain V_o = 1V to 6V, R_L = 100kΩ, V_i = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$	 30 20	 50		 30 10	 50		V/mV
GBP	Gain Bandwidth Product (A_v = 40dB, R_L = 100kΩ, C_L = 100pF, f_{in} = 100 kHz)		 0.7			 0.7		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4V, V_i = 1V to 7.4V	 60	 80		 60	 80		dB
SVR	Supply Voltage Rejection Ratio V_{CC}^+ = 5V to 10V ,V_o = 1.4V	 60	 80		 60	 80		dB
I_{CC}	Supply Current (per amplifier) A_v = 1, no load, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		 150	 200 250		 150	 200 300	µA
I_o	Output Short Circuit Current V_i = 10mV, V_o = 0V	 45	 60	 85	 45	 60	 85	mA
I_{sink}	Output Sink Current Vi = - 10mV, V_o = V_{CC}	 35	 45	 65	 35	 45	 65	mA
S_{vo}	Slew-Rate at Unity Gain R_L = 100kΩ, C_L= 100pF		 0.6			 0.6		V/µs
∅ m	Phase Margin at Unity Gain A_v = 40 dB, R_L = 100kΩ C_L= 10pF C_L= 100pF		 50 30			 50 30		degrees
K_{ov}	Overshoot Factor C_L = 10pF C_L = 100pF		 30 50			 30 50		%
V_n	Equivalent Input Noise Voltage f = 1kHz, R_S = 10Ω		 38			 38		nV/√Hz

TYPICAL CHARACTERISTICS FOR $I_{SET} = 25\mu A$

Figure 11 : Supply Current (each amplifier) versus Supply Voltage.

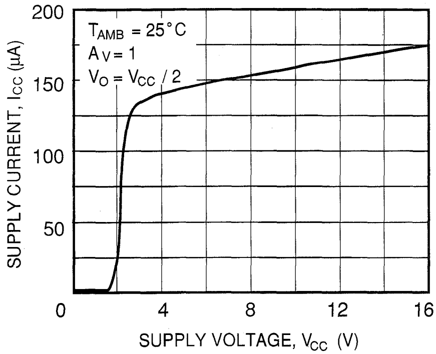


Figure 12 : Input Bias Current versus Free Air Temperature.

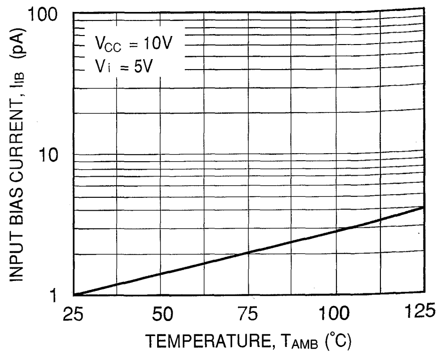


Figure 13a : High Level Output Voltage versus High Level Output Current.

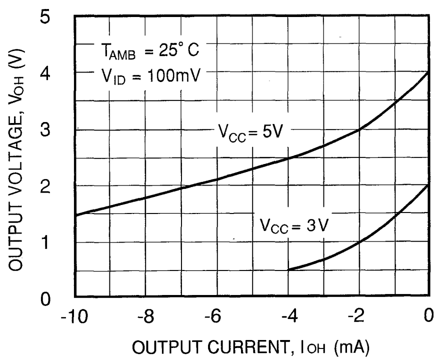


Figure 13b : High Level Output Voltage versus High Level Output Current.

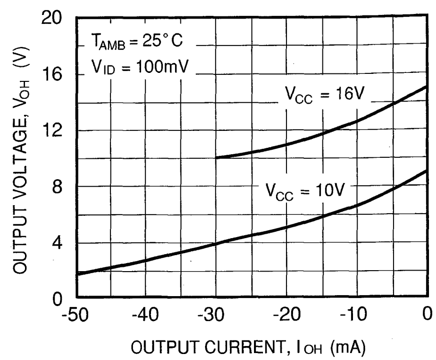


Figure 14a : Low Level Output Voltage versus Low Level Output Current.

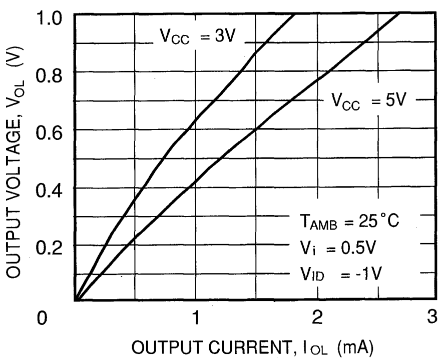
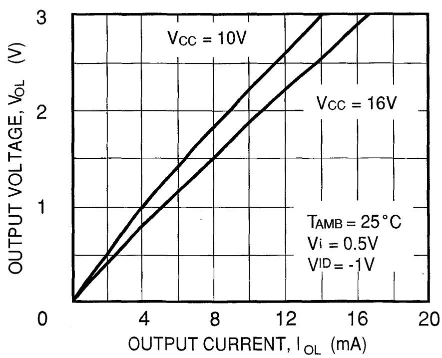


Figure 14b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS FOR I_{SET} = 25μA (continued)

Figure 15 : Open Loop Frequency Response and Phase Shift.

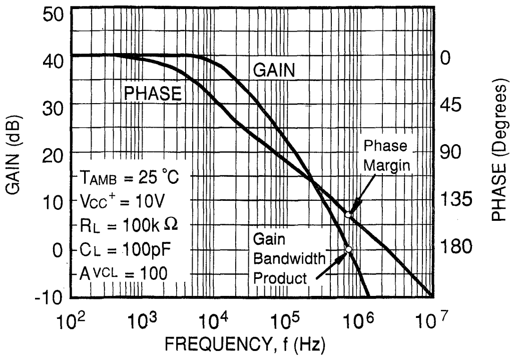


Figure 16 : Gain Bandwidth Product versus Supply Voltage.

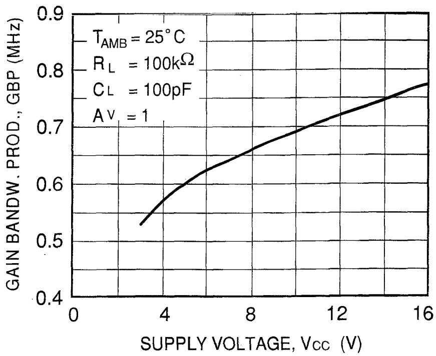


Figure 17 : Phase Margin versus Supply Voltage.

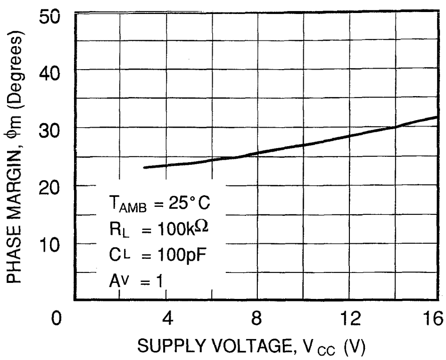


Figure 18 : Phase Margin versus Capacitive Load.

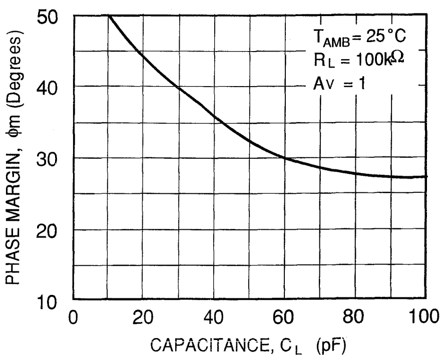
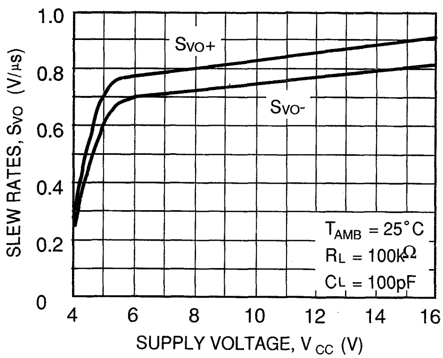


Figure 19 : Slew Rates versus Supply Voltage.



ELECTRICAL CHARACTERISTICS FOR I_{SET} = 130µA

V_{CC}^+ = + 10V, V_{CC}^- = 0V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	TS271C/AC/BC			TS271I/AI/BI TS271M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_O = 1.4V, V_i = 0V TS271C/I/M TS271AC/AI/AM TS271BC/BI/BM $T_{MIN} \le T_{AMB} \le T_{MAX}$ TS271C/I/M TS271AC/AI/AM TS271BC/BI/BM		1.1 0.9 0.25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5V, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		1	100		1	200	pA
I_{ib}	Input Bias Current V_i = 5V, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		1	150		1	300	pA
V_{OH}	High Level Output Voltage V_i = 10mV, R_L = 10kΩ $T_{MIN} \le T_{AMB} \le T_{MAX}$	8.2 8.1	8.4		8.2 8	8.4		V
V_{OL}	Low Level Output Voltage (Vi = - 10mV)			50			50	mV
A_{vd}	Large Signal Voltage Gain V_o = 1V to 6V, R_L = 10kΩ, V_i = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$	10 7	15		10 6	15		V/mV
GBP	Gain Bandwidth Product (A_v = 40dB, R_L = 10kΩ, C_L = 100pF, f_{in} = 200 kHz)		2.3			2.3		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4V, V_i = 1V to 7.4V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC}^+ = 5V to 10V ,V_o = 1.4V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_v = 1, no load, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		800	1300 1400		800	1300 1500	µA
I_o	Output Short Circuit Current V_i = 10mV, V_o = 0V	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current Vi = - 10mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{vo}	Slew-Rate at Unity Gain R_L = 10kΩ, C_L= 100pF		4.5			4.5		V/µs
∅ m	Phase Margin at Unity Gain A_v = 40 dB, R_L = 10kΩ C_L= 10pF C_L= 100pF		65 50			65 50		degrees
K_{ov}	Overshoot Factor C_L = 10pF C_L = 100pF		30 30			30 30		%
V_n	Equivalent Input Noise Voltage f = 1kHz, R_S = 10Ω		30			30		nV/√Hz

TYPICAL CHARACTERISTICS FOR I_{SET} = 130μA

Figure 20 : Supply Current (each amplifier) versus Supply Voltage.

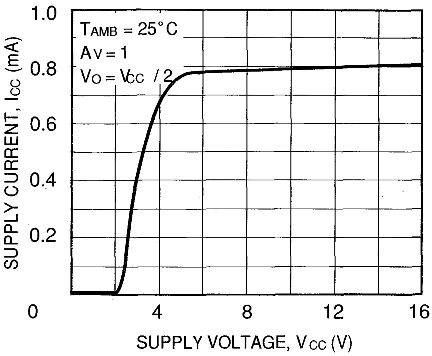


Figure 21 : Input Bias Current versus Free Air Temperature.

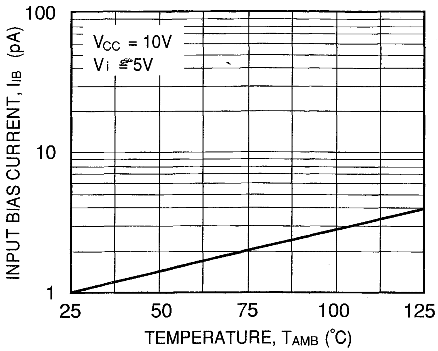


Figure 22a : High Level Output Voltage versus High Level Output Current.

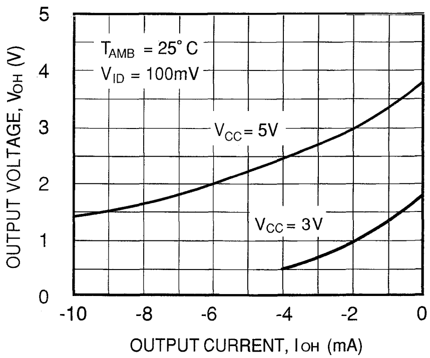


Figure 22b : High Level Output Voltage versus High Level Output Current.

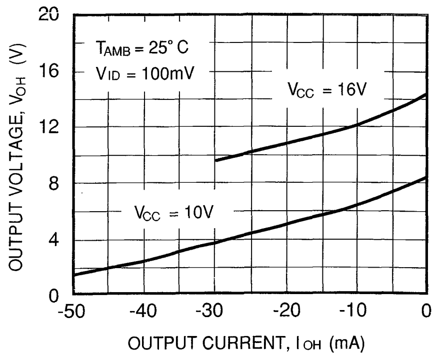


Figure 23a : Low Level Output Voltage versus Low Level Output Current.

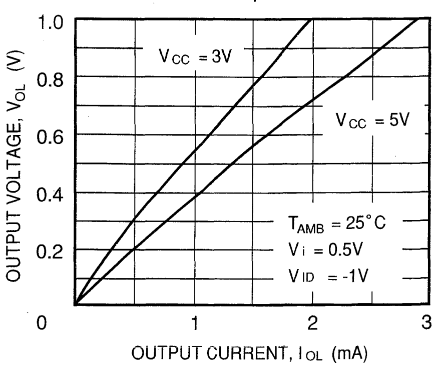
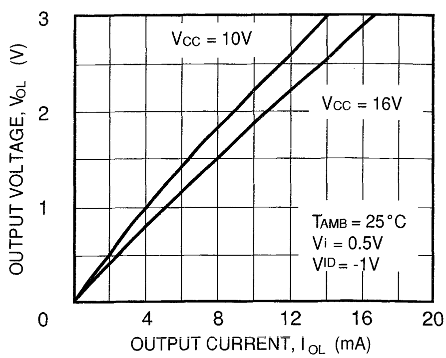


Figure 23b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS FOR I_{SET} = 130µA (continued)

Figure 24 : Open Loop Frequency Response and Phase Shift.

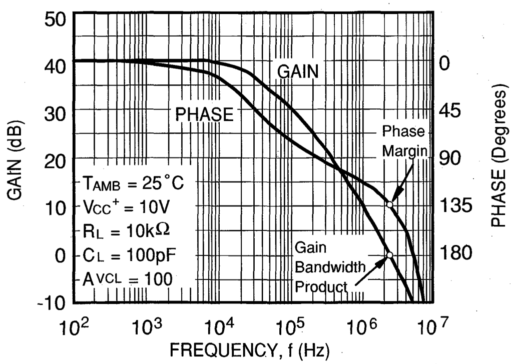


Figure 25 : Gain Bandwidth Product versus Supply Voltage.

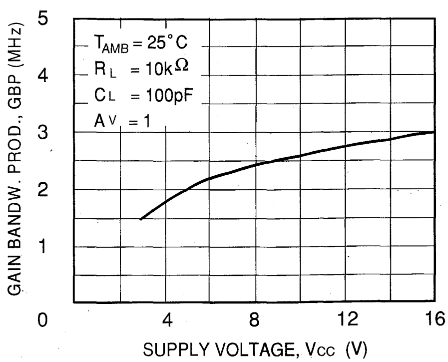


Figure 26 : Phase Margin versus Supply Voltage.

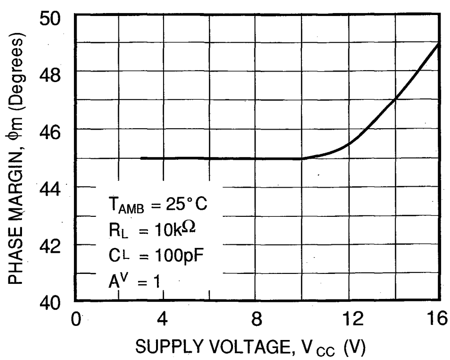


Figure 27 : Phase Margin versus Capacitive Load.

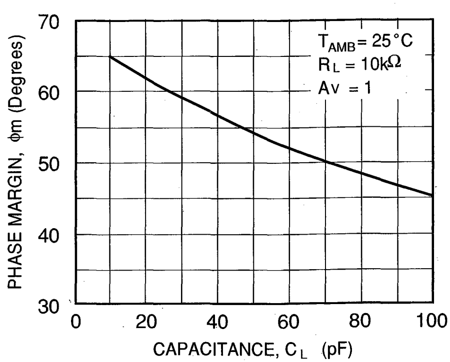
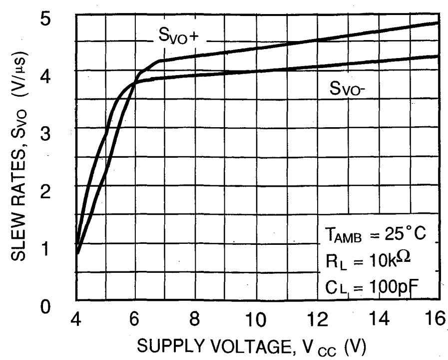
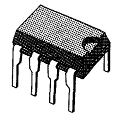


Figure 28 : Slew Rates versus Supply Voltage.

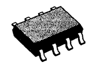


VERY LOW POWER DUAL CMOS OP-AMPs

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL082 -LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
Minidip Plastic



D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS27L2C/AC/BC	0°C to + 70°C	•	•	•
TS27L2I/AI/BI	- 40°C to + 105°C	•	•	•
TS27L2M/AM/BM	- 55°C to + 125°C	•	•	•
Example : TS27L2ACN				

DESCRIPTION

The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

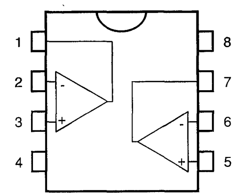
Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L2 (very low power)
- I_{CC}= 150µA/amp. : TS27M2 (low power)
- I_{CC}= 1mA/amp. : TS272 (high speed)

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

PIN CONNECTIONS (Top view)

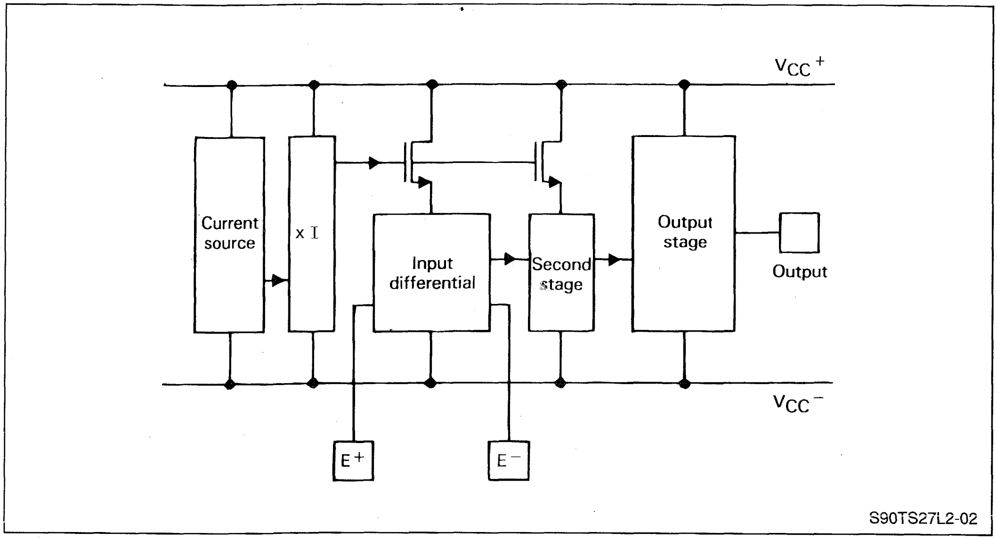
DIP8 - CERDIP 8 - SO8



1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

S90TS27L2-01

BLOCK DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS27L2C/AC/BC TS27L2I/AI/BI TS27L2M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

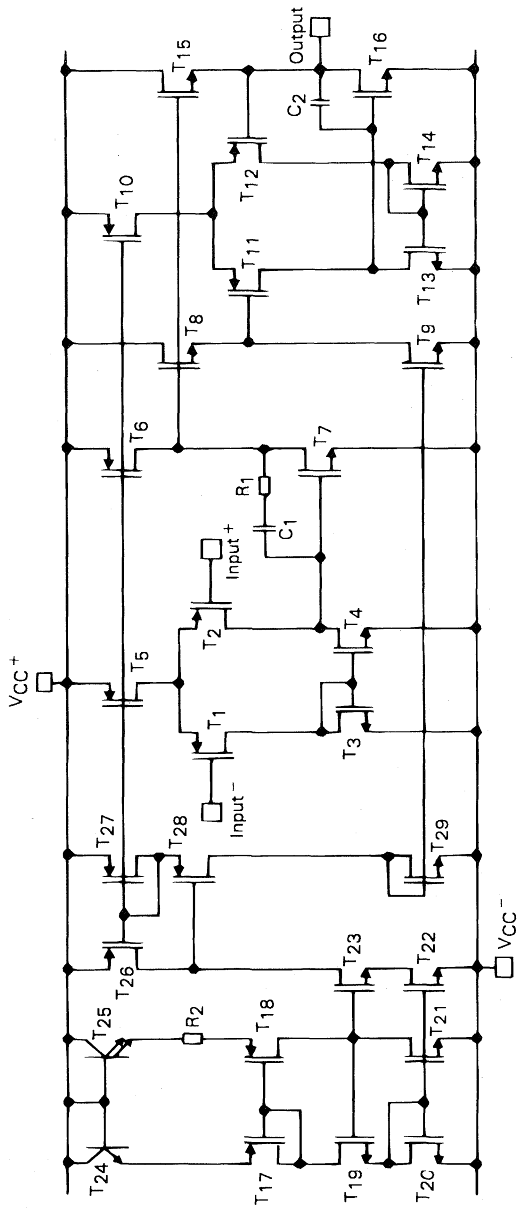
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3* to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/2 TS27L2)



S90TS27L2-03

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{AMB} = 25^oC$ (unless otherwise specified)

Symbol	Parameter	TS27L2C/AC/BC			TS27L2I/AI/BI TS27L2M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_i = 0V$ TS27L2C/I/M TS27L2AC/AI/AM TS27L2BC/BI/BM $T_{MIN} \leq T_{AMB} \leq T_{MAX}$ TS27L2C/I/M TS27L2AC/AI/AM TS27L2BC/BI/BM		1.1 0.9 0.25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		0.7			0.7		µV/°C
I_{io}	Input Offset Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		1	100		1	200	pA
I_{ib}	Input Bias Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		1	150		1	300	pA
V_{OH}	High Level Output Voltage $V_i = 10mV$, $R_L = 1M\Omega$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	8.8 8.7	9		8.8 8.6	9		V
V_{OL}	Low Level Output Voltage $Vi = -10mV$			50			50	mV
A_{vd}	Large Signal Voltage Gain $V_o = 1V$ to $6V$, $R_L = 1M\Omega$, $V_i = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	60 45	100		60 40	100		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 1M\Omega$, $C_L = 100pF$ $f_{in} = 10$ kHz		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio $V_o = 1.4V$, $V_i = 1V$ to $7.4V$	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to $10V$, $V_o = 1.4V$	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		10	15 17		10	15 18	µA
I_o	Output Short Circuit Current $V_i = 10mV$, $V_o = 0V$	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current $Vi = -10mV$, $V_o = V_{CC}$	35	45	65	35	45	65	mA
S_{vo}	Slew-Rate at Unity Gain $R_L = 1M\Omega$, $C_L = 100pF$		0.04			0.04		V/µs
∅ m	Phase Margin at Unity Gain $A_v = 40$ dB, $R_L = 1M\Omega$, $C_L = 100pF$		45			45		degrees
K_{ov}	Overshoot Factor		30			30		%
V_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_S = 10\Omega$		68			68		$nV/\sqrt{Hz}$
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

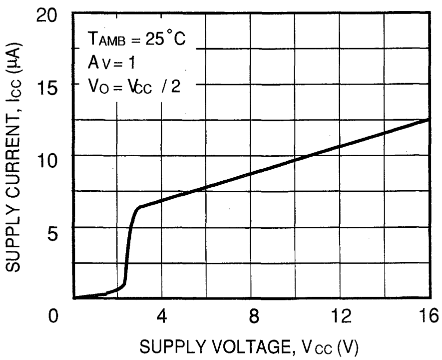


Figure 2 : Input Bias Current versus Free Air Temperature.

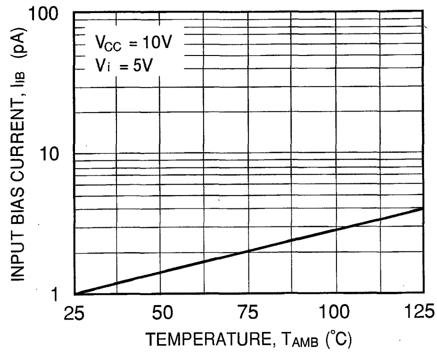


Figure 3a : High Level Output Voltage versus High Level Output Current.

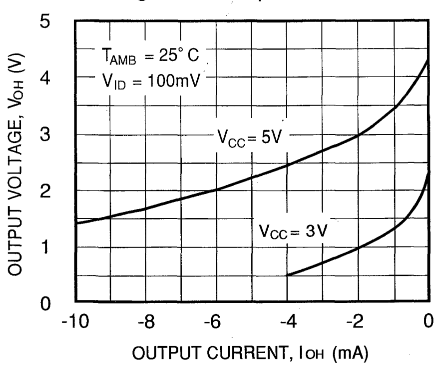


Figure 3b : High Level Output Voltage versus High Level Output Current.

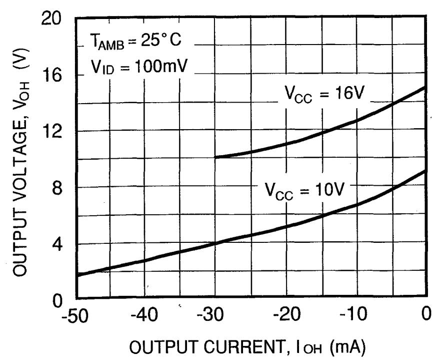


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

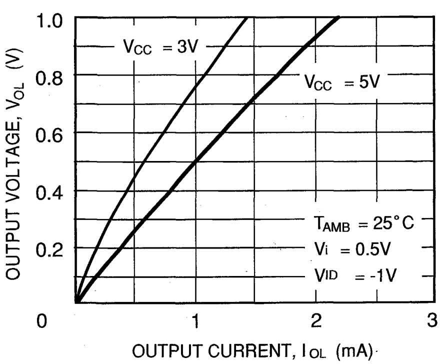
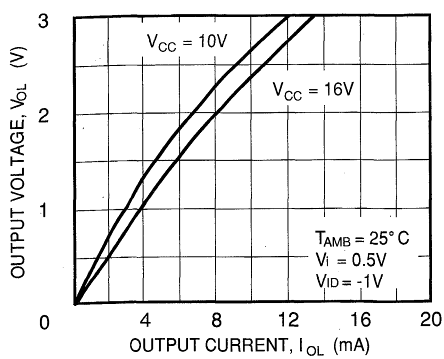


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift.

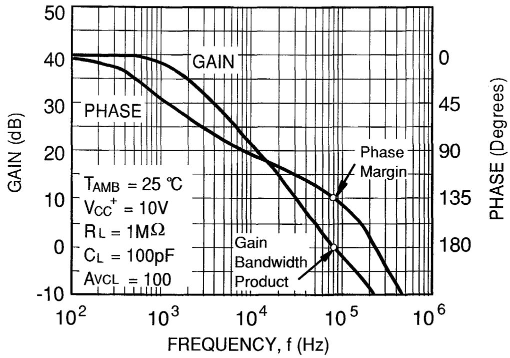


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

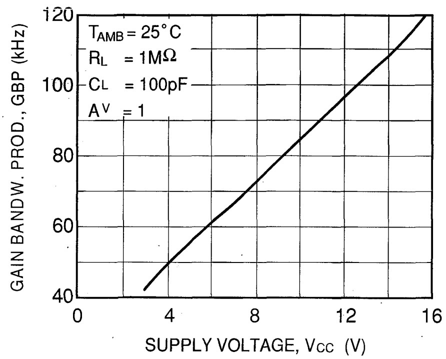


Figure 7 : Phase Margin versus Supply Voltage.

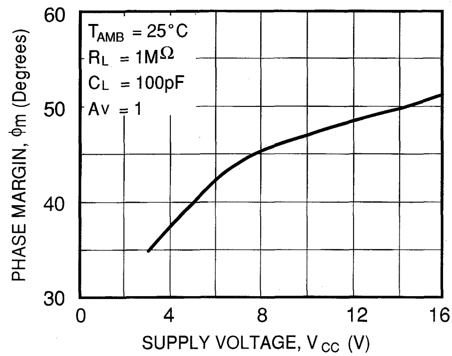


Figure 8 : Phase Margin versus Capacitive Load.

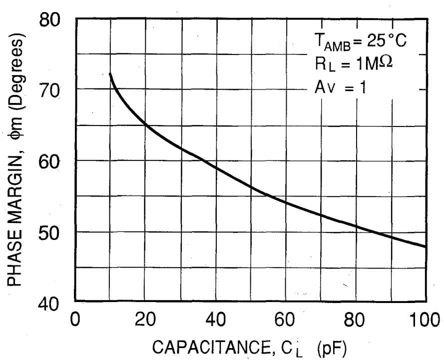
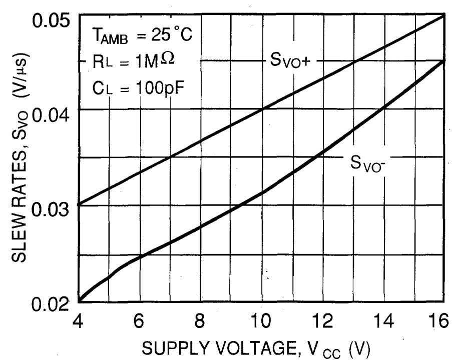
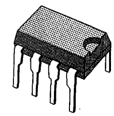


Figure 9 : Slew Rates versus Supply Voltage.

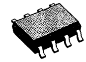


LOW POWER DUAL CMOS OP-AMPs

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL082 -LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
Minidip Plastic



D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS27M2C/AC/BC	0°C to + 70°C	•	•	•
TS27M2I/AI/BI	- 40°C to + 105°C	•	•	•
TS27M2M/AM/BM	- 55°C to + 125°C	•	•	•

Example : TS27M2ACN

DESCRIPTION

The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

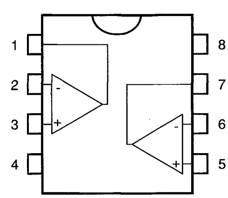
Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L2 (very low power)
- I_{CC}= 150µA/amp. : TS27M2 (low power)
- I_{CC}= 1mA/amp. : TS272 (high speed)

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

PIN CONNECTIONS (Top view)

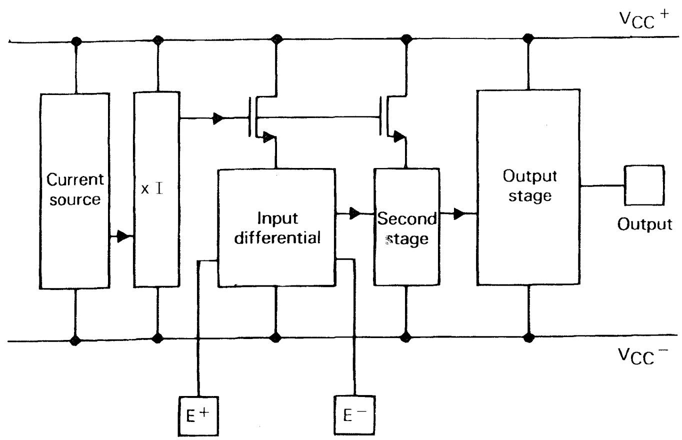
DIP8 - CERDIP 8 - SO8



1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

S90TS27M2-01

BLOCK DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq$ 15V	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS27M2C/AC/BC TS27M2I/AI/BI TS27M2M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

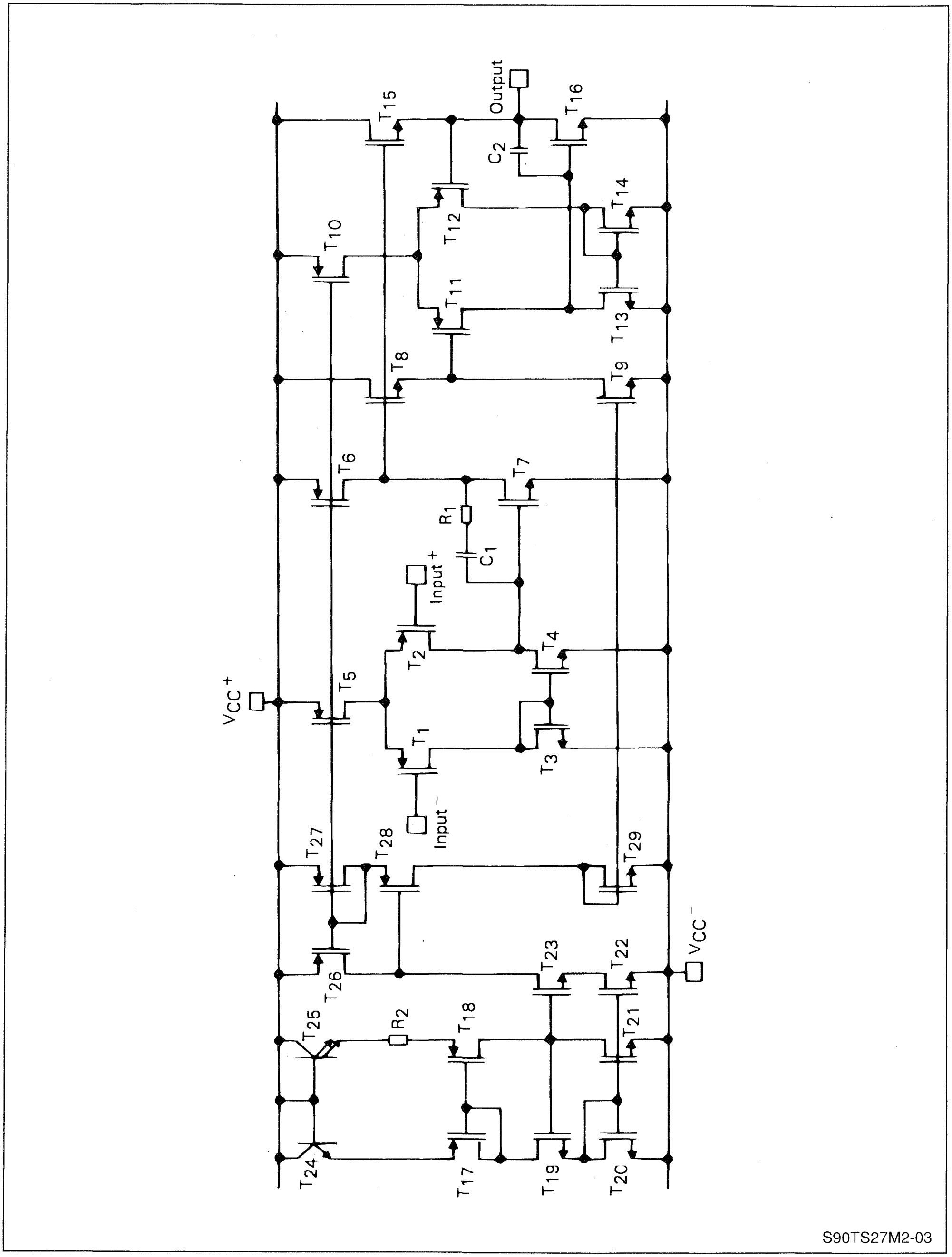
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3* to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/2 TS27M2)



ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{AMB} = 25^oC$ (unless otherwise specified)

Symbol	Parameter	TS27M2C/AC/BC			TS27M2I/AI/BI TS27M2M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_i = 0V$ TS27M2C/I/M TS27M2AC/AI/AM TS27M2BC/BI/BM $T_{MIN} \leq T_{AMB} \leq T_{MAX}$ TS27M2C/I/M TS27M2AC/AI/AM TS27M2BC/BI/BM		1.1 0.9 0.25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		1	100		1	200	pA
I_{ib}	Input Bias Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		1	150		1	300	pA
V_{OH}	High Level Output Voltage $V_i = 10mV$, $R_L = 100k\Omega$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	8.7 8.6	8.9		8.7 8.5	8.9		V
V_{OL}	Low Level Output Voltage $V_i = -10mV$			50			50	mV
A_{vd}	Large Signal Voltage Gain $V_o = 1V$ to $6V$, $R_L = 100k\Omega$, $V_i = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	30 20	50		30 10	50		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 100k\Omega$, $C_L = 100pF$ $f_{in} = 100$ kHz		1			1		MHz
CMR	Common Mode Rejection Ratio $V_o = 1.4V$, $V_i = 1V$ to $7.4V$	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to $10V$, $V_o = 1.4V$	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		150	200 250		150	200 300	µA
I_o	Output Short Circuit Current $V_i = 10mV$, $V_o = 0V$	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current $V_i = -10mV$, $V_o = V_{CC}$	35	45	65	35	45	65	mA
S_{vo}	Slew-Rate at Unity Gain $R_L = 100k\Omega$, $C_L = 100pF$		0.6			0.6		V/µs
Ø m	Phase Margin at Unity Gain $A_v = 40$ dB, $R_L = 100k\Omega$, $C_L = 100pF$		45			45		degrees
K_{ov}	Overshoot Factor		30			30		%
V_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_S = 10\Omega$		38			38		$nV/\sqrt{Hz}$
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

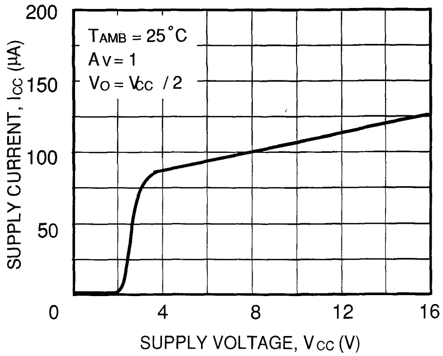


Figure 2 : Input Bias Current versus Free Air Temperature.

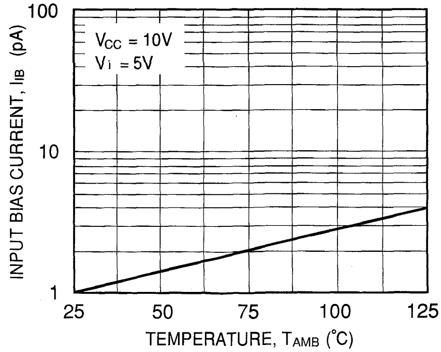


Figure 3a : High Level Output Voltage versus High Level Output Current.

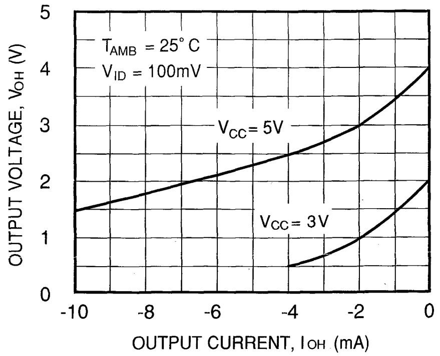


Figure 3b : High Level Output Voltage versus High Level Output Current.

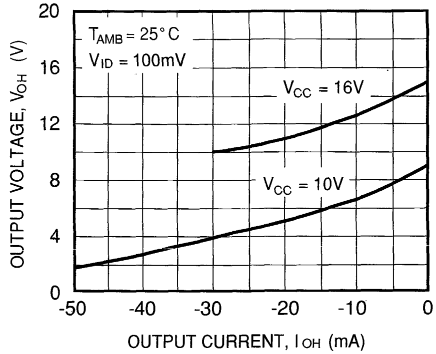


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

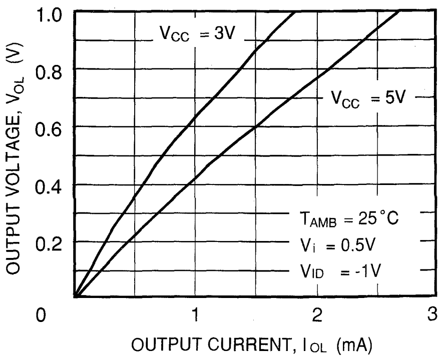
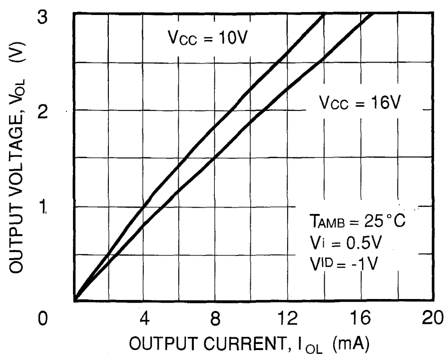


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift.

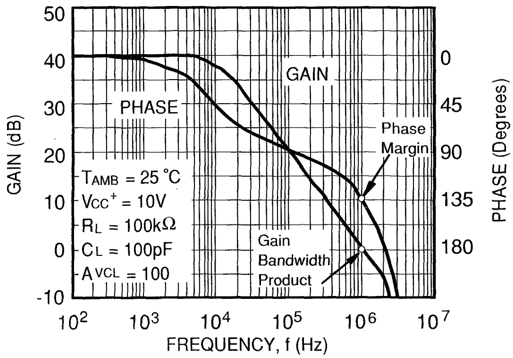


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

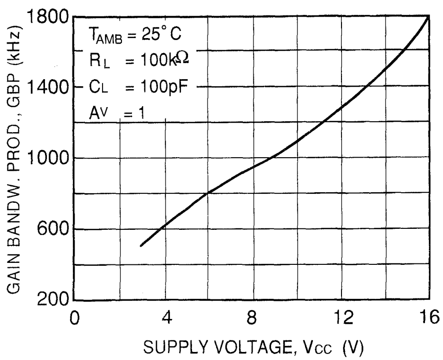


Figure 7 : Phase Margin versus Supply Voltage.

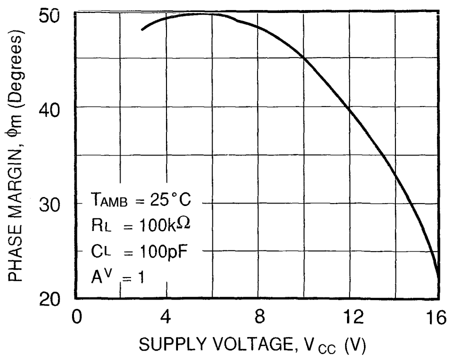


Figure 8 : Phase Margin versus Capacitive Load.

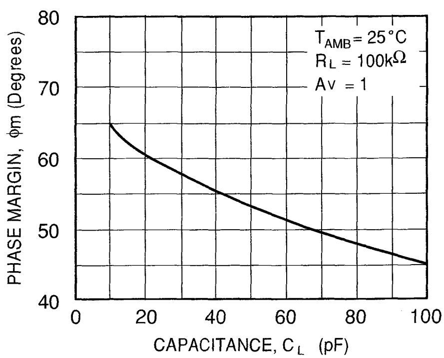
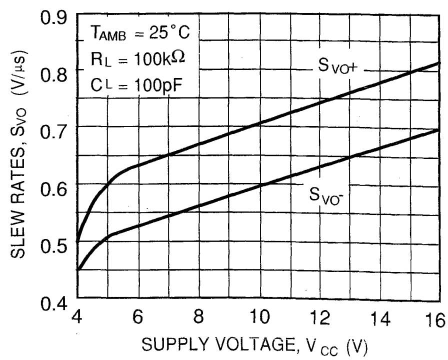
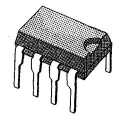


Figure 9 : Slew Rates versus Supply Voltage.

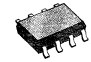


HIGH SPEED DUAL CMOS OP-AMPs

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL082 -LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
Minidip Plastic



D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

DESCRIPTION

The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10μA/amp. : TS27L2 (very low power)
- I_{CC}= 150μA/amp. : TS27M2 (low power)
- I_{CC}= 1mA/amp. : TS272 (high speed)

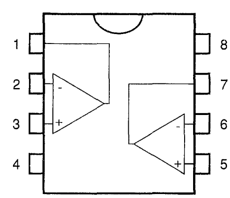
The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS272C/AC/BC	0°C to + 70°C	•	•	•
TS272I/AI/BI	- 40°C to + 105°C	•	•	•
TS272M/AM/BM	- 55°C to + 125°C	•	•	•
Example : TS272ACN				

PIN CONNECTIONS (Top view)

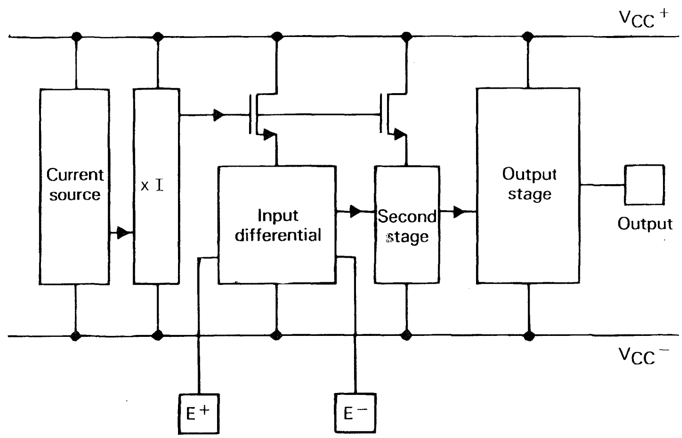
DIP8 - CERDIP 8 - SO8



1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{CC}^{-}
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^{+}

S90TS272-01

BLOCK DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS272C/AC/BC TS272I/AI/BI TS272M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

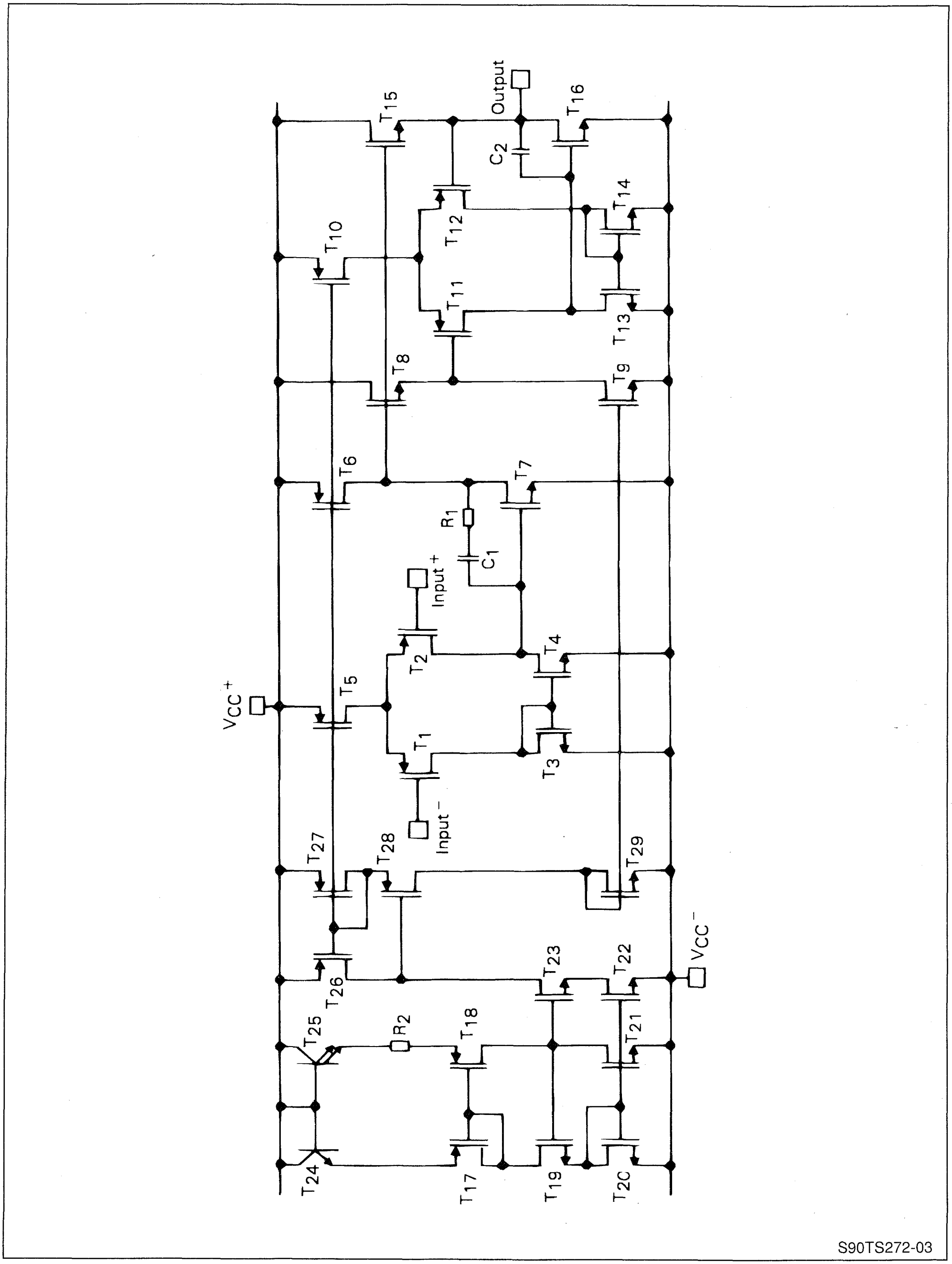
Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3 * to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/2 TS272)



ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{AMB} = 25^oC$ (unless otherwise specified)

Symbol	Parameter	TS272C/AC/BC			TS272I/AI/BI TS272M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_i = 0V$ TS272C/I/M TS272AC/AI/AM TS272BC/BI/BM $T_{MIN} \leq T_{AMB} \leq T_{MAX}$ TS272C/I/M TS272AC/AI/AM TS272BC/BI/BM		 1.1 0.9 0.25	 10 5 2 12 6.5 3		 1.1 0.9 0.25	 10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		 1	 100		 1	 200	pA
I_{ib}	Input Bias Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		 1	 150		 1	 300	pA
V_{OH}	High Level Output Voltage $V_i = 10mV$, $R_L = 10k\Omega$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 8.2 8.1	 8.4		 8.2 8	 8.4		V
V_{OL}	Low Level Output Voltage $Vi = -10mV$			 50			 50	mV
A_{vd}	Large Signal Voltage Gain $V_o = 1V$ to $6V$, $R_L = 10k\Omega$, $V_i = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 10 7	 15		 10 6	 15		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 10k\Omega$, $C_L = 100pF$ $f_{in} = 200$ kHz		 3.5			 3.5		MHz
CMR	Common Mode Rejection Ratio $V_o = 1.4V$, $V_i = 1V$ to $7.4V$	 65	 80		 65	 80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to $10V$, $V_o = 1.4V$	 60	 70		 60	 70		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		 1000	 1500 1600		 1000	 1500 1700	µA
I_o	Output Short Circuit Current $V_i = 10mV$, $V_o = 0V$	 45	 60	 85	 45	 60	 85	mA
I_{sink}	Output Sink Current $Vi = -10mV$, $V_o = V_{CC}$	 35	 45	 65	 35	 45	 65	mA
S_{vo}	Slew-Rate at Unity Gain $R_L = 10k\Omega$, $C_L = 100pF$		 5.5			 5.5		V/µs
∅ m	Phase Margin at Unity Gain $A_v = 40$ dB, $R_L = 10k\Omega$, $C_L = 100pF$		 40			 40		degrees
K_{ov}	Overshoot Factor		30			30		%
V_n	Equivalent Input Noise Voltage f = 1kHz, $R_S = 10\Omega$		 30			 30		$nV/\sqrt{Hz}$
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

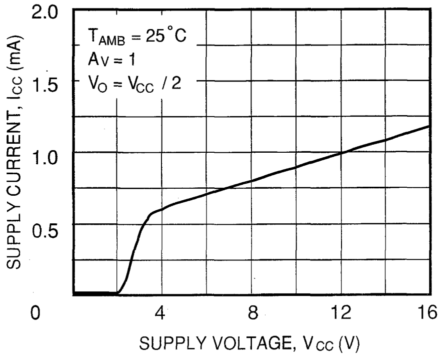


Figure 2 : Input Bias Current versus Free Air Temperature.

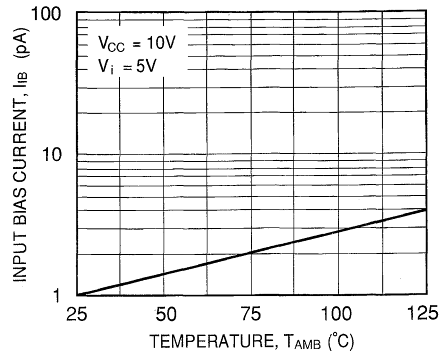


Figure 3a : High Level Output Voltage versus High Level Output Current.

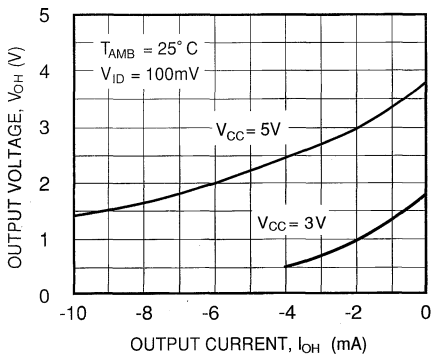


Figure 3b : High Level Output Voltage versus High Level Output Current.

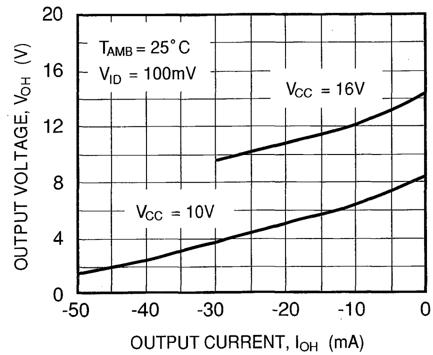


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

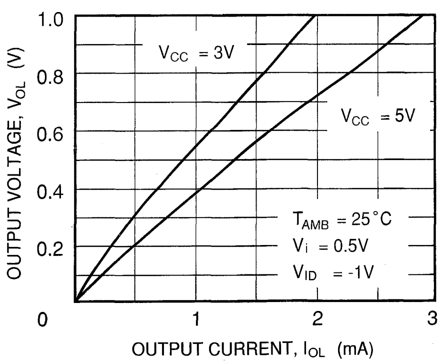
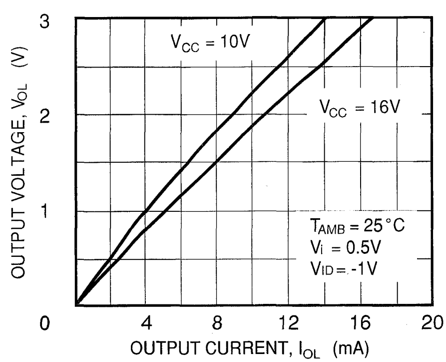


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift.

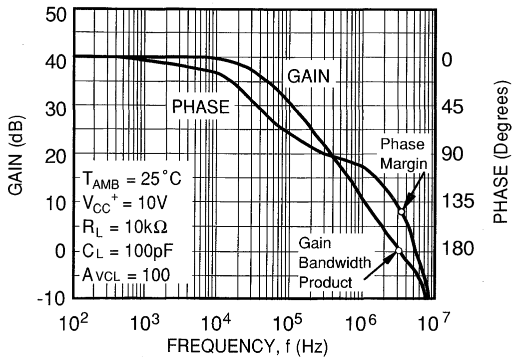


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

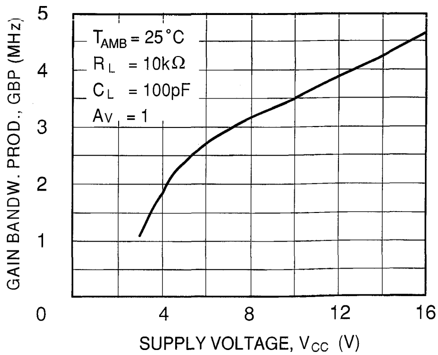


Figure 7 : Phase Margin versus Supply Voltage.

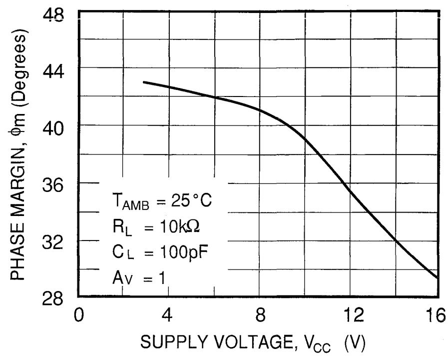


Figure 8 : Phase Margin versus Capacitive Load.

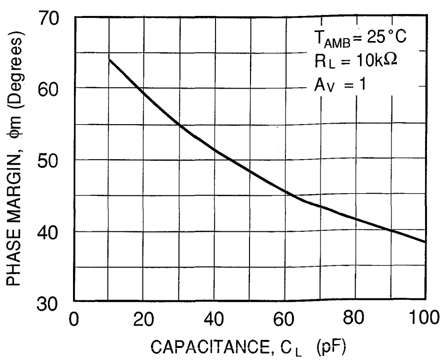
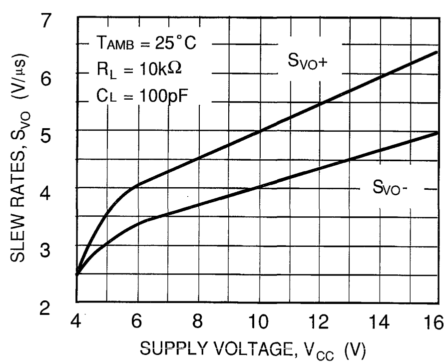
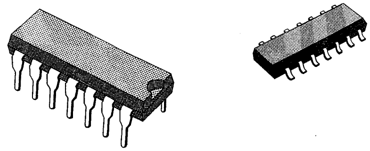


Figure 9 : Slew Rates versus Supply Voltage.



VERY LOW POWER QUAD CMOS OP-AMPs

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
DIP14
(Plastic Package)

D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

DESCRIPTION

The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L4 (very low power)
- I_{CC}= 150µA/amp. : TS27M4 (low power)
- I_{CC}= 1mA/amp. : TS274 (high speed)

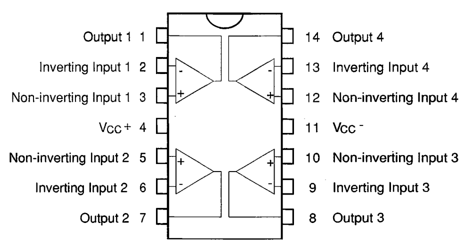
The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS27L4C/AC/BC	0°C to + 70°C	•	•	•
TS27L4I/AI/BI	- 40°C to + 105°C	•	•	•
TS27L4M/AM/BM	- 55°C to + 125°C	•	•	•
Example : TS27L4ACN				

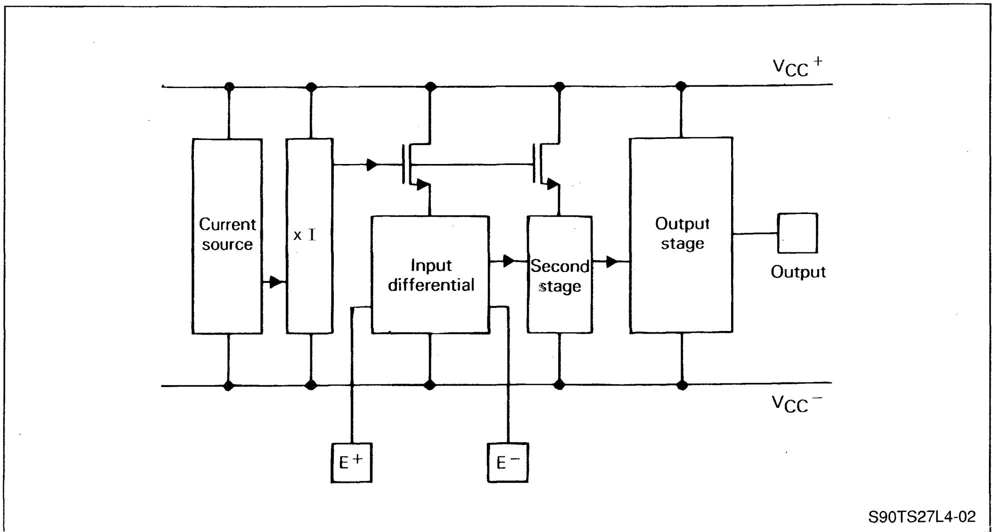
PIN CONNECTIONS (Top view)

DIP14 - CERDIP 14 - SO14



S90TS27L4-01

BLOCK DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^{+}	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^{+} \geq 15V$	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS27L4C/AC/BC TS27L4I/AI/BI TS27L4M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

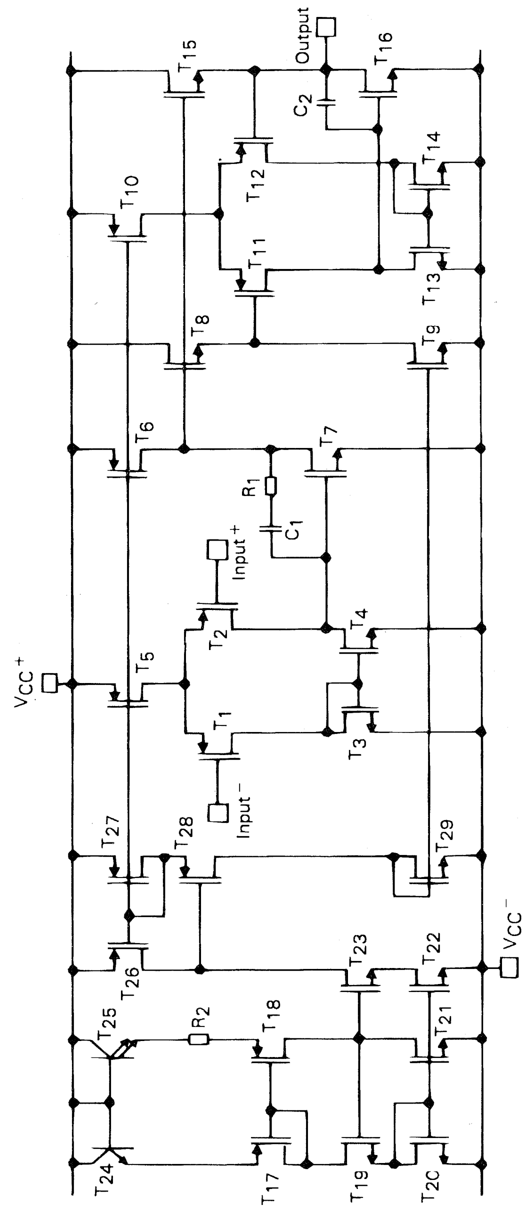
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^{+}	Supply Voltage	3* to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^{+} - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/4 TS27L4)



S90TS27L4-03

ELECTRICAL CHARACTERISTICS

$V_{CC}^{+} = +10V$, $V_{CC}^{-} = 0V$, $T_{AMB} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	TS27L4C/AC/BC			TS27L4I/AI/BI TS27L4M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_i = 0V$ TS27L4C/I/M TS27L4AC/AI/AM TS27L4BC/BI/BM $T_{MIN} \leq T_{AMB} \leq T_{MAX}$ TS27L4C/I/M TS27L4AC/AI/AM TS27L4BC/BI/BM		 1.1 0.9 0.25	 10 5 2 12 6.5 3		 1.1 0.9 0.25	 10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		0.7			0.7		µV/°C
I_{io}	Input Offset Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		 1	 100		 1	 200	pA
I_{ib}	Input Bias Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		 1	 150		 1	 300	pA
V_{OH}	High Level Output Voltage $V_i = 10mV$, $R_L = 1M\Omega$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 8.8 8.7	 9		 8.8 8.6	 9		V
V_{OL}	Low Level Output Voltage Vi = - 10mV			 50			 50	mV
A_{vd}	Large Signal Voltage Gain $V_o = 1V$ to $6V$, $R_L = 1M\Omega$, $V_i = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 60 45	 100		 60 40	 100		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 1M\Omega$, $C_L = 100pF$ $f_{in} = 10$ kHz		 0.1			 0.1		MHz
CMR	Common Mode Rejection Ratio $V_o = 1.4V$, $V_i = 1V$ to $7.4V$	 65	 80		 65	 80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^{+} = 5V$ to $10V$, $V_o = 1.4V$	 60	 80		 60	 80		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		 10	 15 17		 10	 15 18	µA
I_o	Output Short Circuit Current $V_i = 10mV$, $V_o = 0V$	 45	 60	 85	 45	 60	 85	mA
I_{sink}	Output Sink Current Vi = - 10mV, $V_o = V_{CC}$	 35	 45	 65	 35	 45	 65	mA
S_{vo}	Slew-Rate at Unity Gain $R_L = 1M\Omega$, $C_L = 100pF$		 0.04			 0.04		V/µs
∅ m	Phase Margin at Unity Gain $A_v = 40$ dB, $R_L = 1M\Omega$, $C_L = 100pF$		 45			 45		degrees
K_{ov}	Overshoot Factor		30			30		%
V_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_S = 10\Omega$		 68			 68		$nV/\sqrt{Hz}$
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

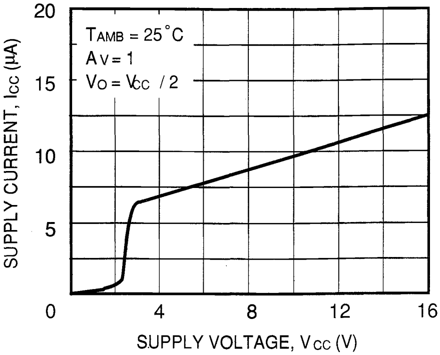


Figure 2 : Input Bias Current versus Free Air Temperature.

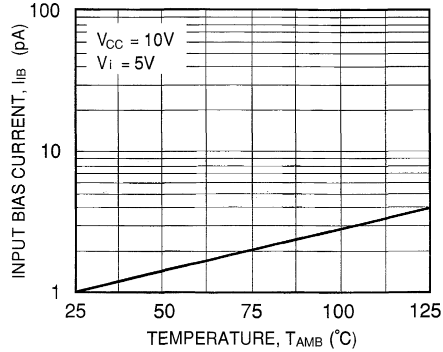


Figure 3a : High Level Output Voltage versus High Level Output Current.

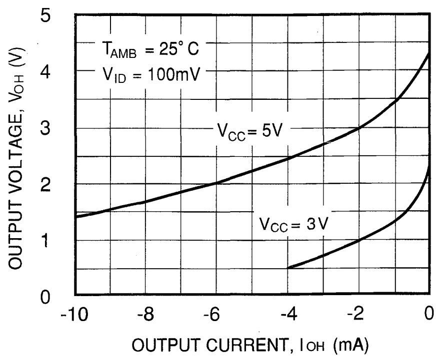


Figure 3b : High Level Output Voltage versus High Level Output Current.

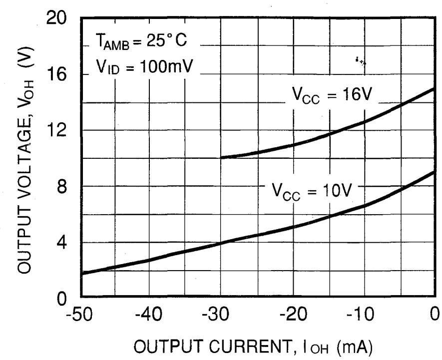


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

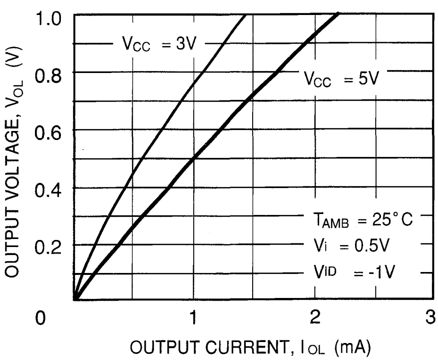
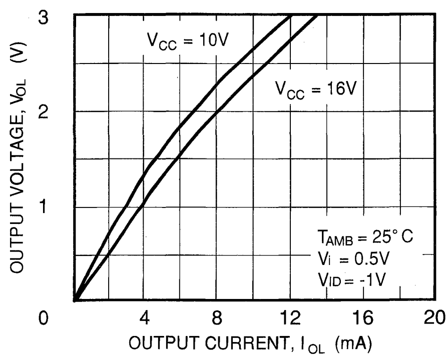


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift.

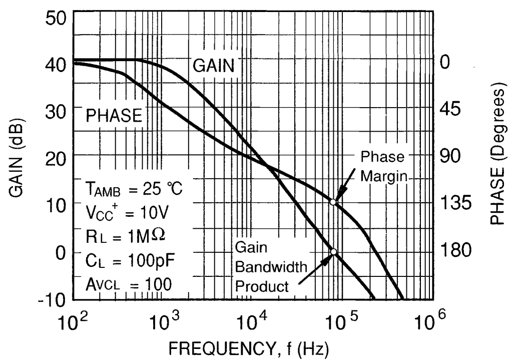


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

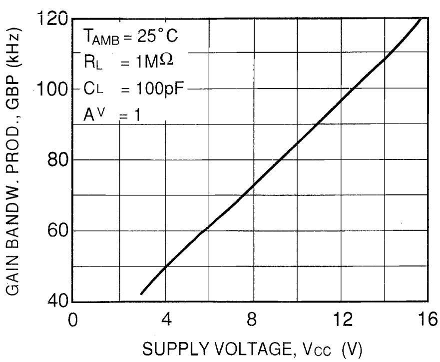


Figure 7 : Phase Margin versus Supply Voltage.

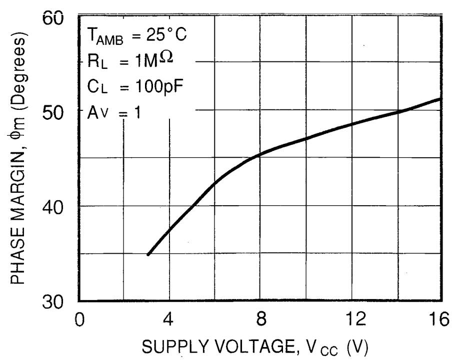


Figure 8 : Phase Margin versus Capacitive Load.

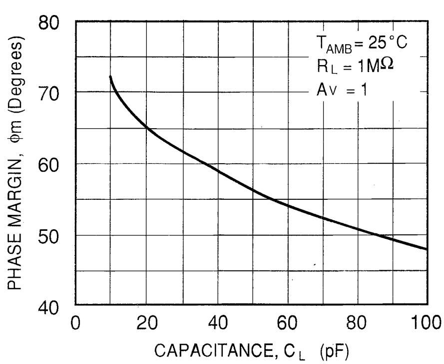
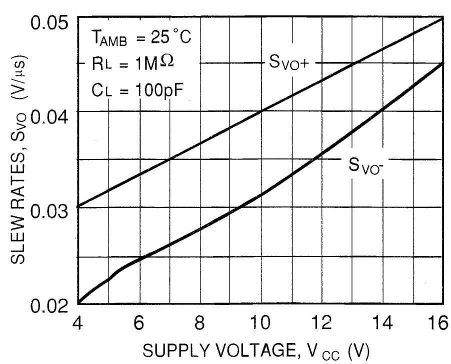


Figure 9 : Slew Rates versus Supply Voltage.

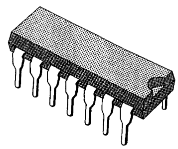


SGS-THOMSON MICROELECTRONICS

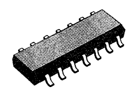
TS27M4C,I,M

LOW POWER QUAD CMOS OP-AMPs

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS27M4C/AC/BC	0°C to + 70°C	•	•	•
TS27M4I/AI/BI	- 40°C to + 105°C	•	•	•
TS27M4M/AM/BM	- 55°C to + 125°C	•	•	•
Example : TS27M4ACN				

DESCRIPTION

The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

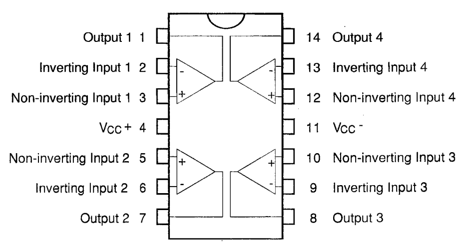
Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L4 (very low power)
- I_{CC}= 150µA/amp. : TS27M4 (low power)
- I_{CC}= 1mA/amp. : TS274 (high speed)

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

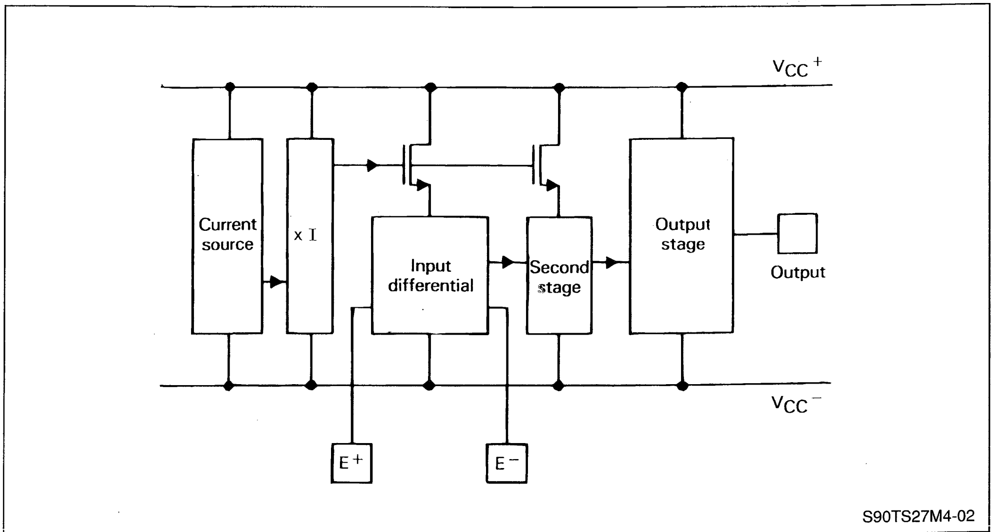
PIN CONNECTIONS (Top view)

DIP14 - CERDIP 14 - SO14



S90TS27M4-01

BLOCK DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage (Note 1)		18	V
V_{id}	Differential Input Voltage (Note 2)		± 18	V
V_i	Input Voltage (Note 3)		- 0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$		± 30	mA
T_{oper}	Operating Free-Air Temperature Range	TS27M4C/AC/BC TS27M4I/AI/BI TS27M4M/AM/BM	0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range		- 65 to + 150	°C

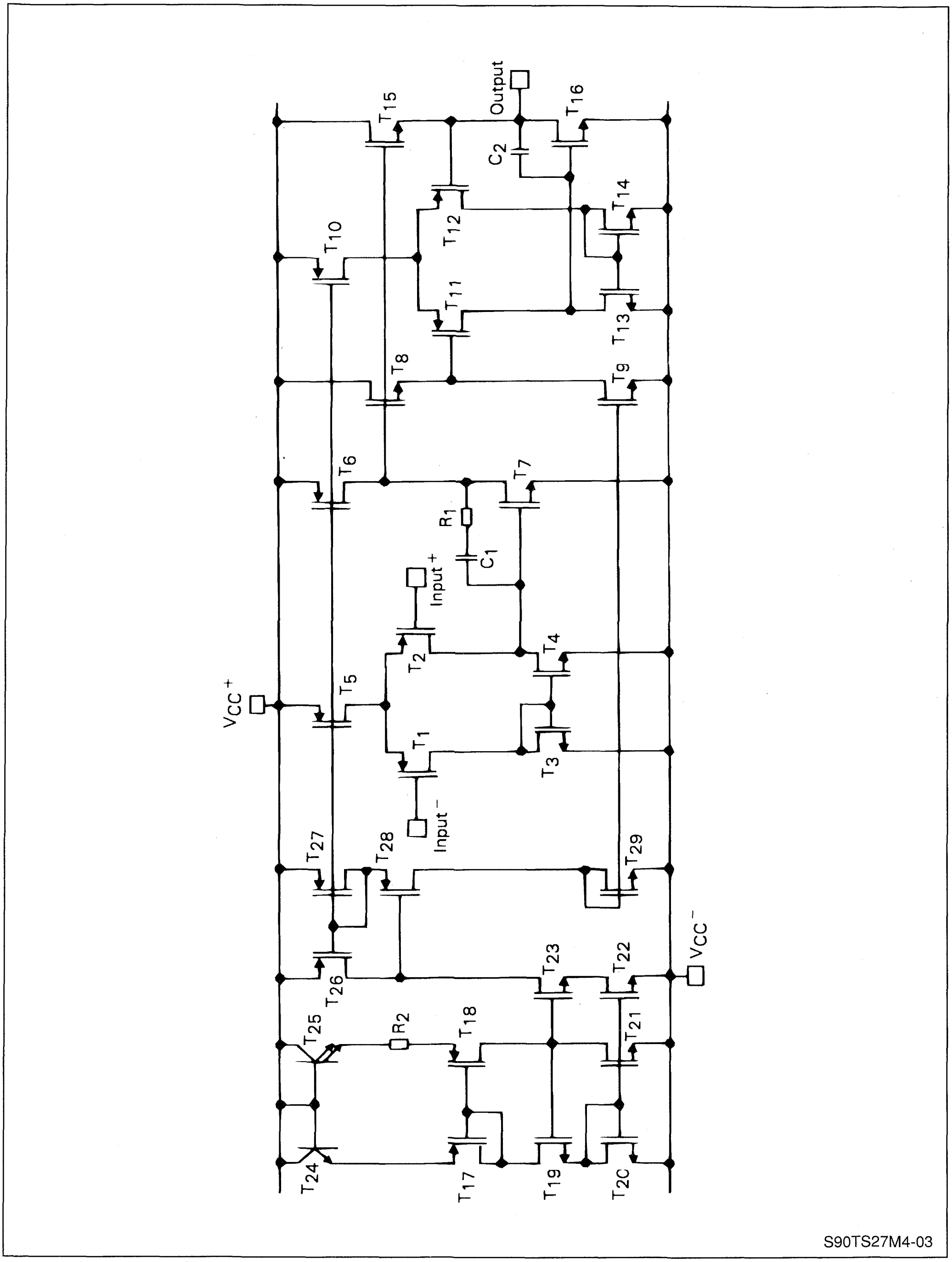
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3* to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/4 TS27M4)



ELECTRICAL CHARACTERISTICS

$V_{CC}^{+} = +10V$, $V_{CC}^{-} = 0V$, $T_{AMB} = 25^{o}C$ (unless otherwise specified)

Symbol	Parameter	TS27M4C/AC/BC			TS27M4I/AI/BI TS27M4M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_i = 0V$ TS27M4C/I/M TS27M4AC/AI/AM TS27M4BC/BI/BM $T_{MIN} \leq T_{AMB} \leq T_{MAX}$ TS27M4C/I/M TS27M4AC/AI/AM TS27M4BC/BI/BM		 1.1 0.9 0.25	 10 5 2 12 6.5 3		 1.1 0.9 0.25	 10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		 1	 100		 1	 200	pA
I_{ib}	Input Bias Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		 1	 150		 1	 300	pA
V_{OH}	High Level Output Voltage $V_i = 10mV$, $R_L = 100k\Omega$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 8.7 8.6	 8.9		 8.7 8.5	 8.9		V
V_{OL}	Low Level Output Voltage Vi = - 10mV			 50			 50	mV
A_{vd}	Large Signal Voltage Gain $V_o = 1V$ to $6V$, $R_L = 100k\Omega$, $V_i = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 30 20	 50		 30 10	 50		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 100k\Omega$, $C_L = 100pF$ $f_{in} = 100$ kHz		 1			 1		MHz
CMR	Common Mode Rejection Ratio $V_o = 1.4V$, $V_i = 1V$ to $7.4V$	 65	 80		 65	 80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^{+} = 5V$ to $10V$, $V_o = 1.4V$	 60	 80		 60	 80		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		 150	 200 250		 150	 200 300	µA
I_o	Output Short Circuit Current $V_i = 10mV$, $V_o = 0V$	 45	 60	 85	 45	 60	 85	mA
I_{sink}	Output Sink Current Vi = - 10mV, $V_o = V_{CC}$	 35	 45	 65	 35	 45	 65	mA
S_{vo}	Slew-Rate at Unity Gain $R_L = 100k\Omega$, $C_L = 100pF$		 0.6			 0.6		V/µs
∅ m	Phase Margin at Unity Gain $A_v = 40$ dB, $R_L = 100k\Omega$, $C_L = 100pF$		 45			 45		degrees
K_{ov}	Overshoot Factor		30			30		%
V_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_S = 10\Omega$		 38			 38		$nV/\sqrt{Hz}$
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

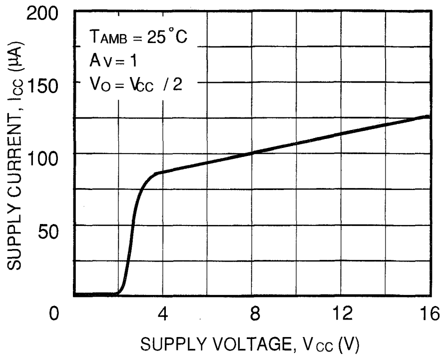


Figure 2 : Input Bias Current versus Free Air Temperature.

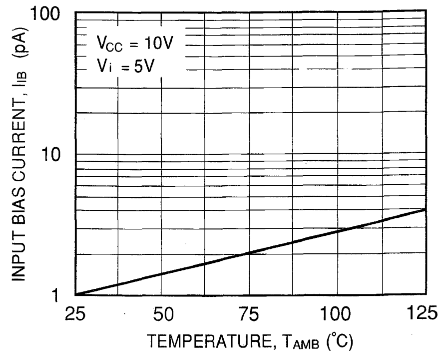


Figure 3a : High Level Output Voltage versus High Level Output Current.

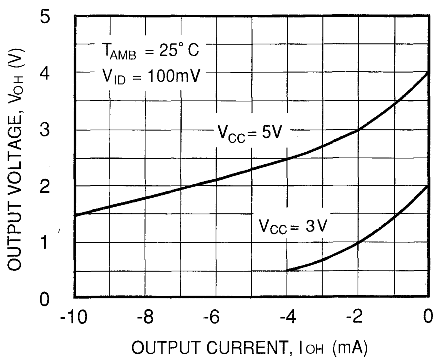


Figure 3b : High Level Output Voltage versus High Level Output Current.

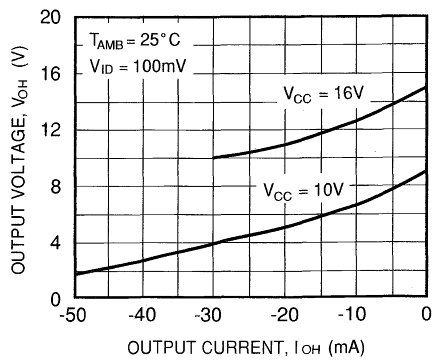


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

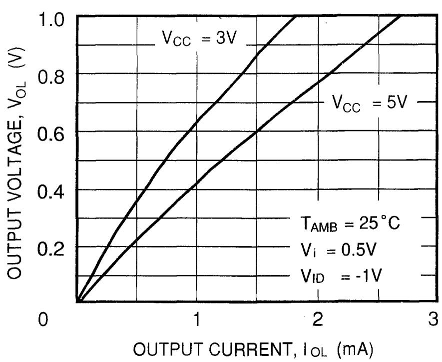
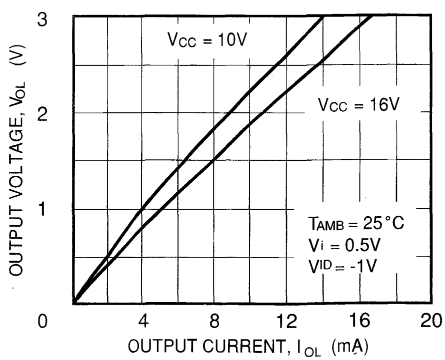


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift.

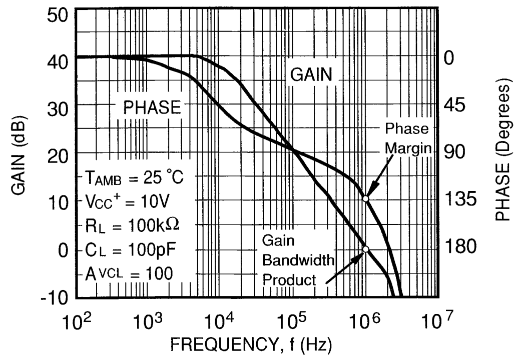


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

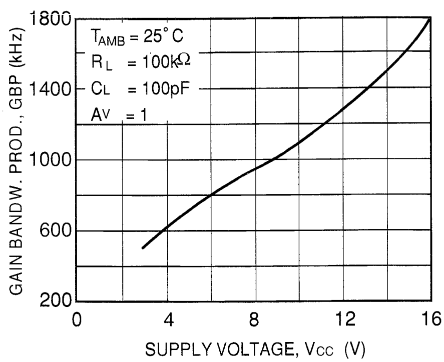


Figure 7 : Phase Margin versus Supply Voltage.

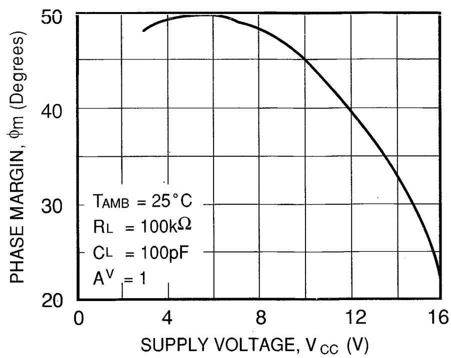


Figure 8 : Phase Margin versus Capacitive Load.

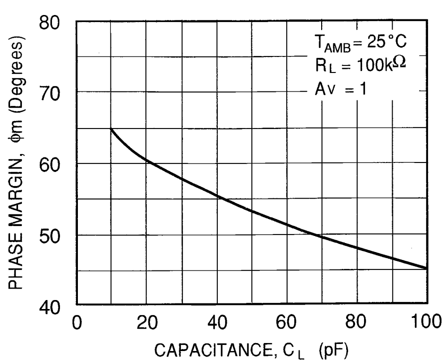
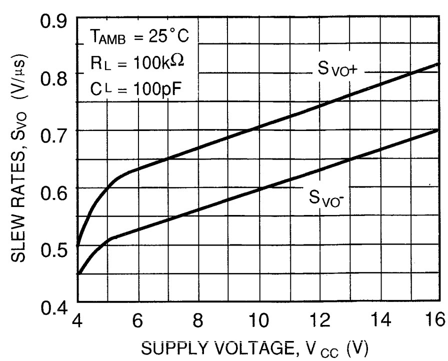


Figure 9 : Slew Rates versus Supply Voltage.

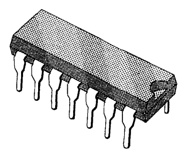


SGS-THOMSON MICROELECTRONICS

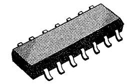
TS274C,I,M

HIGH SPEED QUAD CMOS OP-AMPs

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

DESCRIPTION

The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L4 (very low power)
- I_{CC}= 150µA/amp. : TS27M4 (low power)
- I_{CC}= 1mA/amp. : TS274 (high speed)

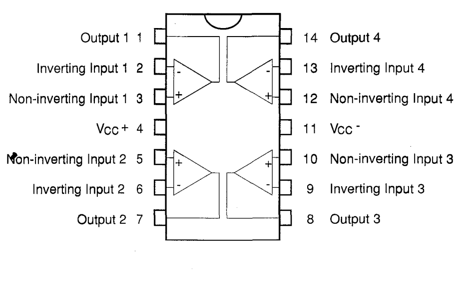
The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

ORDER CODES

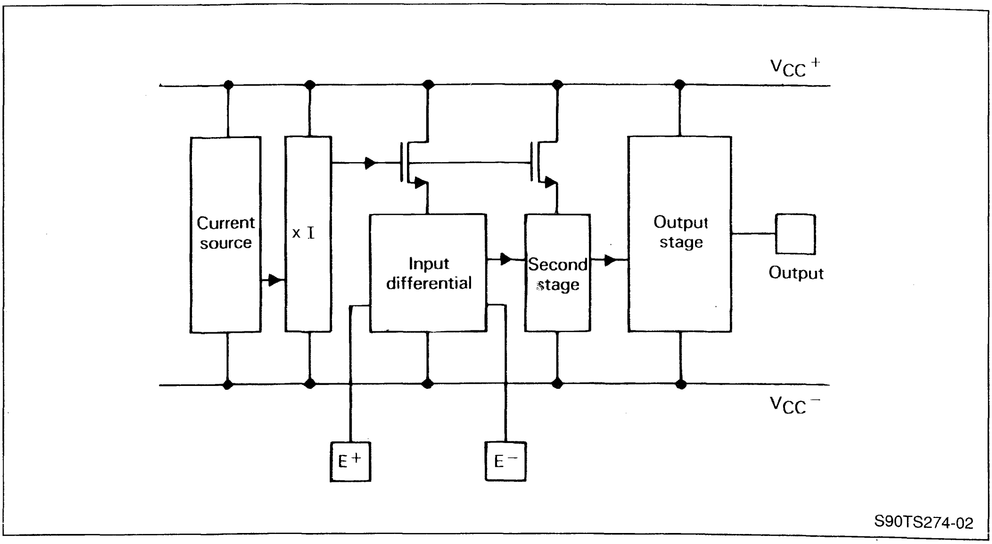
Part Number	Temperature Range	Package		
		N	J	D
TS274C/AC/BC	0°C to + 70°C	•	•	•
TS274I/AI/BI	- 40°C to + 105°C	•	•	•
TS274M/AM/BM	- 55°C to + 125°C	•	•	•
Example : TS274ACN				

PIN CONNECTIONS (Top view)

DIP14 - CERDIP 14 - SO14



BLOCK DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^{+}	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^{+} \geq 15V$	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS274C/AC/BC TS274I/AI/BI TS274M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

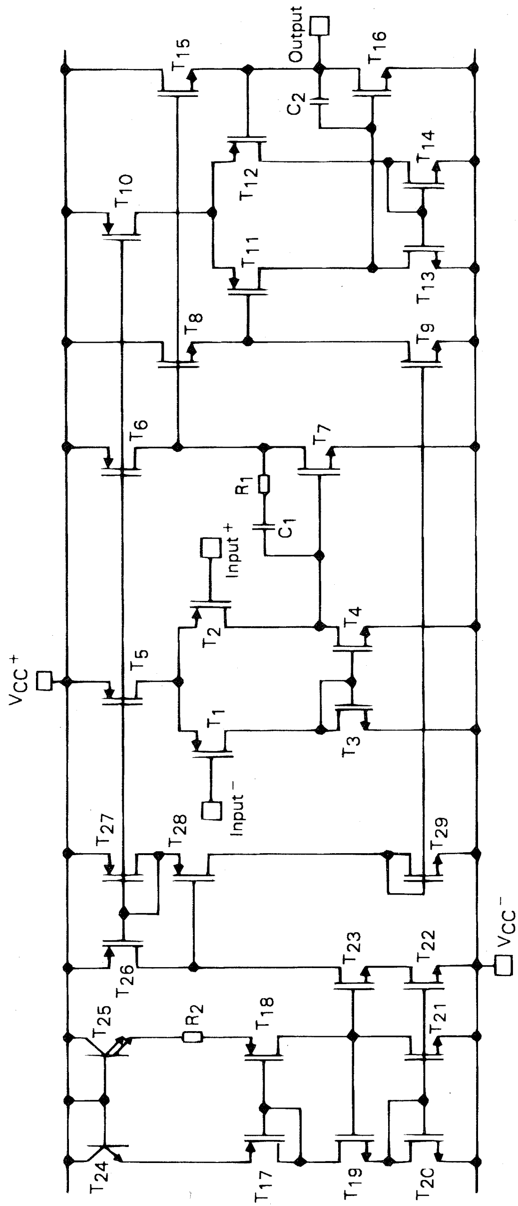
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.

OPTIMAL OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^{+}	Supply Voltage	3* to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^{+} - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/4 TS274)



S90TS274-03

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{AMB} = 25^oC$ (unless otherwise specified)

Symbol	Parameter	TS274C/AC/BC			TS274I/AI/BI TS274M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_i = 0V$ TS274C/I/M TS274AC/AI/AM TS274BC/BI/BM $T_{MIN} \leq T_{AMB} \leq T_{MAX}$ TS274C/I/M TS274AC/AI/AM TS274BC/BI/BM		1.1 0.9 0.25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		1	100		1	200	pA
I_{ib}	Input Bias Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		1	150		1	300	pA
V_{OH}	High Level Output Voltage $V_i = 10mV$, $R_L = 10k\Omega$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	8.2 8.1	8.4		8.2 8	8.4		V
V_{OL}	Low Level Output Voltage Vi = - 10mV			50			50	mV
A_{vd}	Large Signal Voltage Gain $V_o = 1V$ to $6V$, $R_L = 10k\Omega$, $V_i = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	10 7	15		10 6	15		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 10k\Omega$, $C_L = 100pF$ $f_{in} = 200$ kHz		3.5			3.5		MHz
CMR	Common Mode Rejection Ratio $V_o = 1.4V$, $V_i = 1V$ to $7.4V$	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to $10V$, $V_o = 1.4V$	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		1000	1500 1600		1000	1500 1700	µA
I_o	Output Short Circuit Current $V_i = 10mV$, $V_o = 0V$	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current Vi = - 10mV, $V_o = V_{CC}$	35	45	65	35	45	65	mA
S_{vo}	Slew-Rate at Unity Gain $R_L = 10k\Omega$, $C_L = 100pF$		5.5			5.5		V/µs
∅ m	Phase Margin at Unity Gain $A_v = 40$ dB, $R_L = 10k\Omega$, $C_L = 100pF$		40			40		degrees
K_{ov}	Overshoot Factor		30			30		%
V_n	Equivalent Input Noise Voltage f = 1kHz, $R_S = 10\Omega$		30			30		$nV/\sqrt{Hz}$
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

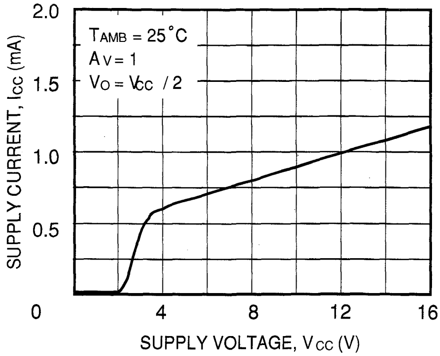


Figure 2 : Input Bias Current versus Free Air Temperature.

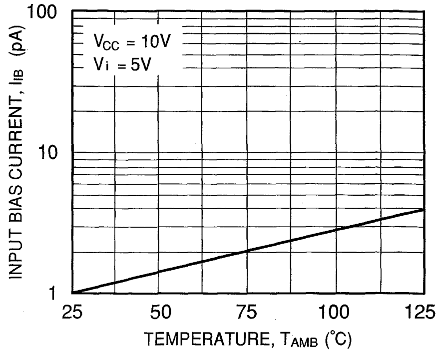


Figure 3a : High Level Output Voltage versus High Level Output Current.

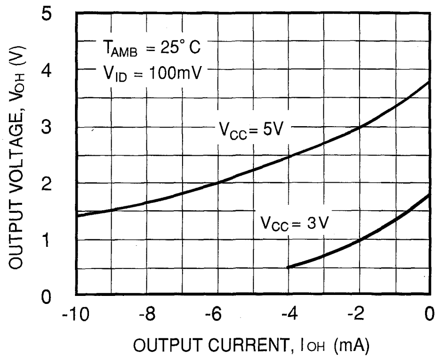


Figure 3b : High Level Output Voltage versus High Level Output Current.

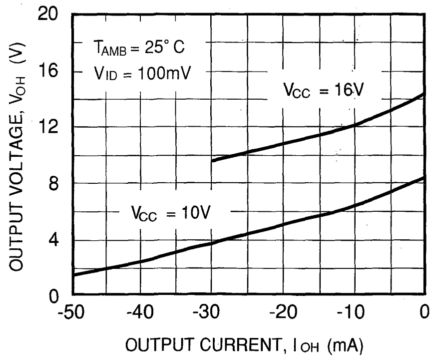


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

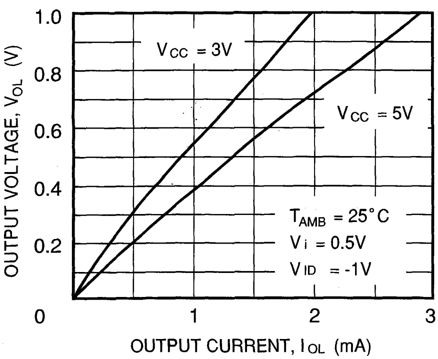
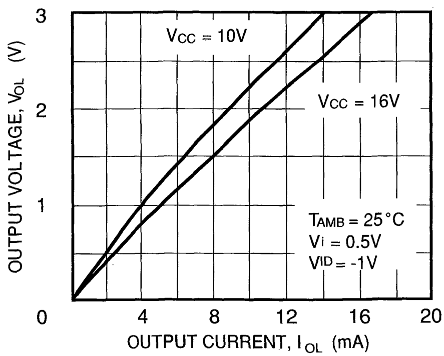


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift.

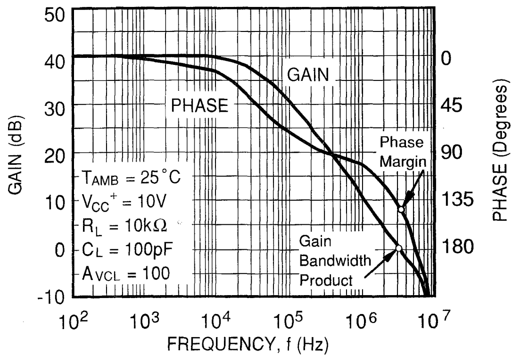


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

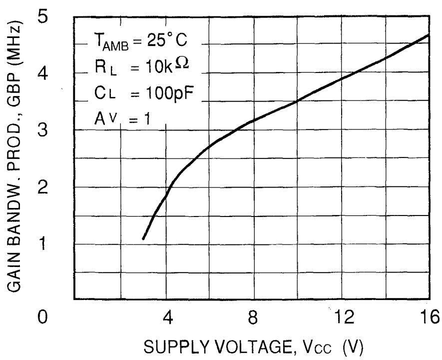


Figure 7 : Phase Margin versus Supply Voltage.

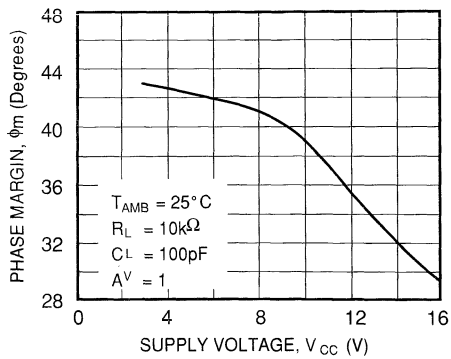


Figure 8 : Phase Margin versus Capacitive Load.

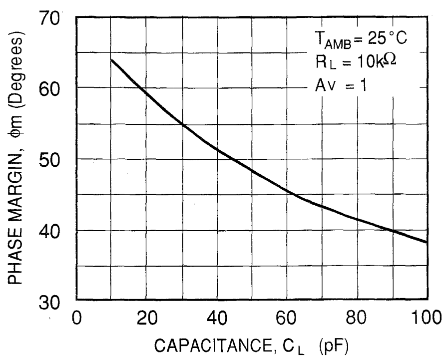
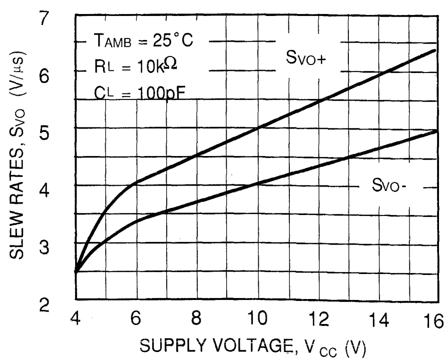
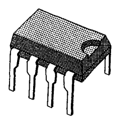


Figure 9 : Slew Rates versus Supply Voltage.



LOW POWER SINGLE CMOS TIMERS

- VERY LOW POWER CONSUMPTION : 100µA typ at V_{CC} = 5V
- HIGH MAXIMUM ASTABLE FREQUENCY 2.7MHz
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR NE555
- VOLTAGE RANGE : +2V to +18V
- HIGH OUTPUT CURRENT CAPABILITY
- SUPPLY CURRENT SPIKES REDUCED DURING OUTPUT TRANSITIONS
- HIGH INPUT IMPEDANCE : 10^{12} Ω
- OUTPUT COMPATIBLE WITH TTL,CMOS AND LOGIC MOS



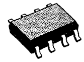
N

Minidip Plastic

J

CERDIP8

(Cerdip Package)



D

SO8

(Plastic Micropackage)

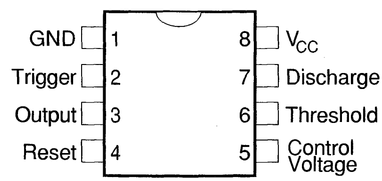
DESCRIPTION

The TS555 is a single CMOS timer which offers very low consumption ($Icc_{(TYP)}$ TS555 = 100µA $Icc_{(TYP)}$ NE555 = 3mA) and high frequency ($f_{(MAX)}$ TS555 = 2.7 MHz - $f_{(MAX)}$ NE555 = 0.1 MHz) Thus, either in Monostable or Astable mode, timing remains very accurate.
The TS555 provides reduced supply current spikes during output transitions, which enables the use of lower decoupling capacitors compared to those required by bipolar NE555.
Timing capacitors can also be minimized due to high input impedance (10^{12} Ω).

ORDER CODES

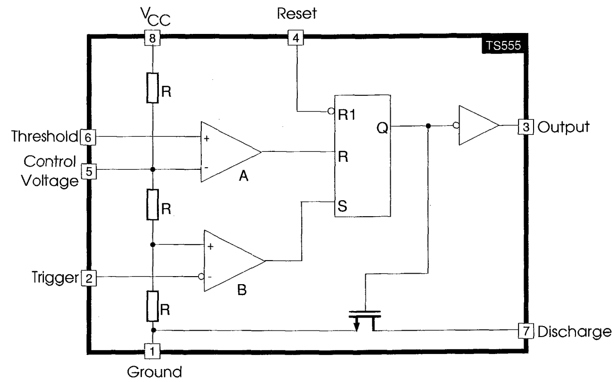
Part Number	Temperature Range	Package		
		N	D	J
TS555C	0 to +70°C	•	•	•
TS555I	-40 to +105°C	•	•	•
TS555M	-55 to +125°C	•	•	•
Examples : TS555CD , TS555IN				

PIN CONNECTION (top view)



S90TS555-01

BLOCK DIAGRAM



FUNCTION TABLE

RESET	TRIGGER	THRESHOLD	OUTPUT
Low	x	x	Low
High	Low	x	High
High	High	High	Low
High	High	Low	Previous State

LOW ↔ Level Voltage ≤ Min voltage specified

HIGH ↔ Level Voltage ≥ Max voltage specified

X ↔ Irrelevant

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+18	V
T_J	Junction Temperature	+150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
T_{OPER}	Operating Temperature Range		°C
	TS555C	0 to +70	
	TS555I	-40 to +105	
	TS555M	-55 to +125	
T_{STG}	Storage Temperature Range	-65 to +150	°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+2 to +16	V

STATIC ELECTRICAL CHARACTERISTICS

V_{CC} = +2V , T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS555C - TS555I - TS555M			Unit
		Min	Typ	Max	
I_{CC}	Supply Current (no load, High and Low States) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 65 -	 200 200	µA
V_{CL}	Control Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 1.2 1.1	 1.3 -	 1.4 1.5	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 1mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.05 -	 0.2 0.25	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 1mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.1 -	 0.3 0.35	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -0.3mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 1.5 1.5	 1.9 -	 - -	V
V_{TRIG}	Trigger Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 0.4 0.3	 0.67 -	 0.95 1.05	V
I_{TRIG}	Trigger Current	-	10	-	pA
I_{TH}	Threshold Current	-	10	-	pA
V_{RESET}	Reset Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 0.4 0.3	 1.1 -	 1.5 2.0	V
I_{RESET}	Reset Current	-	10	-	pA
I_{DIS}	Discharge Pin Leakage Current	-	1	100	nA

STATIC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +5V , T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS555C - TS555I - TS555M			Unit
		Min	Typ	Max	
I_{CC}	Supply Current (no load, High and Low States) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 - -	 110 -	 250 250	µA
V_{CL}	Control Voltage T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 2.9 2.8	 3.3 -	 3.8 3.9	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 10mA) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 - -	 0.2 -	 0.3 0.35	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 8mA) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 - -	 0.3 -	 0.6 0.8	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -2mA) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 4.4 4.4	 4.6 -	 - -	V
V_{TRIG}	Trigger Voltage T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 1.36 1.26	 1.67 -	 1.96 2.06	V
I_{TRIG}	Trigger Current	-	10	-	pA
I_{TH}	Threshold Current	-	10	-	pA
V_{RESET}	Reset Voltage T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 0.4 0.3	 1.1 -	 1.5 2.0	V
I_{RESET}	Reset Current	-	10	-	pA
I_{DIS}	Discharge Pin Leakage Current	-	1	100	nA

STATIC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +12V , T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS555C - TS555I - TS555M			Unit
		Min	Typ	Max	
I_{CC}	Supply Current (no load, High and Low States) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 - -	 170 -	 400 400	µA
V_{CL}	Control Voltage T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 7.4 7.3	 8 -	 8.6 8.7	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 80mA) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 - -	 0.9 -	 1.6 2.0	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 50mA) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 - -	 1.2 -	 2 2.8	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -10mA) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 10.5 10.5	 11 -	 - -	V
V_{TRIG}	Trigger Voltage T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 3.2 3.1	 4 -	 4.8 4.9	V
I_{TRIG}	Trigger Current	-	10	-	pA
I_{TH}	Threshold Current	-	10	-	pA
V_{RESET}	Reset Voltage T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 0.4 0.3	 1.1 -	 1.5 2.0	V
I_{RESET}	Reset Current	-	10	-	pA
I_{DIS}	Discharge Pin Leakage Current	-	1	100	nA

DYNAMIC ELECTRICAL CHARACTERISTICS

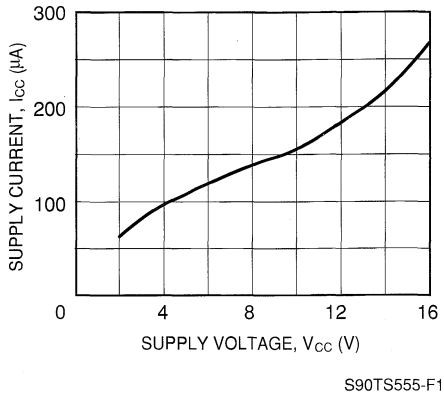
T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS555C - TS555I - TS555M			Unit
		Min	Typ	Max	
	Timing Accuracy (Monostable) - R = 10 kΩ , C = 0.1 µF - (Note 1) V_{CC} = +2V V_{CC} = +5V V_{CC} = +12V	 - - -	 1 2 4	 - - -	%
	Timing Shift with supply voltage variations (Monostable) R = 10 kΩ , C = 0.1 µF , V_{CC} = +5V ± 1V	-	0.38	-	%/V
	Timing Shift with temperature $T_{MIN} \leq T_{AMB} \leq T_{MAX}$, V_{CC} = +5V	-	75	-	ppm/ °C
f_{MAX}	Maximum astable frequency R_A = 470Ω , R_B = 200Ω , C = 200 pF , V_{CC} = +5V	-	2.7	-	MHz
	Astable frequency accuracy - (Note 2) R_A= R_B = 1kΩ to 100kΩ , C = 0.1µF V_{CC} = +5V V_{CC} = +12V	- -	3 3	- -	%
	Timing Shift with supply voltage variations (Astable mode) R_A = R_B = 1kΩ to 100kΩ , C = 0.1µF , V_{CC} = +5 to +12V	-	0.1	-	%/V
t_r	Output Rise Time (V_{CC} = +5V , C_{LOAD}= 10pF)	-	25	-	ns
t_f	Output Fall Time (V_{CC} = +5V , C_{LOAD} = 10pF)	-	20	-	ns
t_{PD}	Trigger Propagation Delay (V_{CC} = +5V)	-	100	-	ns
t_{RPW}	Minimum Reset Pulse Width (V_{TRIG} = +5V)	-	350	-	ns

Notes : 1. See Figure 1
2. See Figure 2

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each timer) versus Supply Voltage.

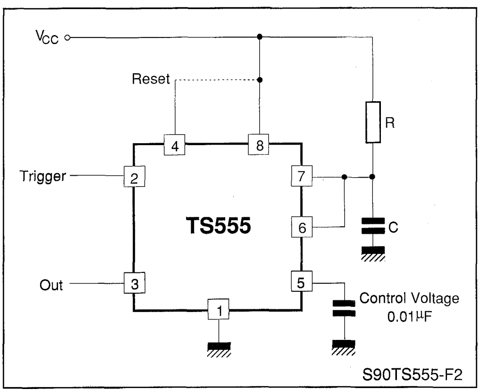


APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode,the timer functions as a one-shot. Referring to figure 2 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 2.



The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered,the circuit remains in this state until the set time has elapsed,even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R x C.

Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4) and the Trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

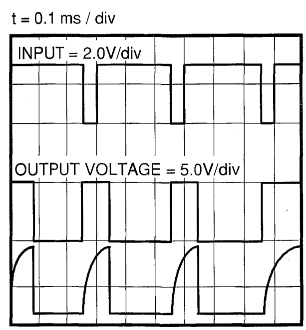
When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant τ = R x C.

When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state.

Figure 3 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possible or false triggering.

Figure 3.



CAPACITOR VOLTAGE = 2.0V/div

R = 9.1kΩ, C = 0.01μF , R_L = 1.0kΩ

S90TS555-F3

ASTABLE OPERATION

When the circuit is connected as shown in figure 4 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency, are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by :

$t1 = 0.693 (R_A + R_B) C$

and the discharge time (output LOW) by :

$t2 = 0.693 (R_B) C$

Thus the total period T is given by :

$T = t1 + t2 = 0.693 (R_A + 2R_B) C$

The frequency of oscillation is then :

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

The duty cycle is given by : $D = \frac{R_B}{R_A + 2R_B}$

Figure 4.

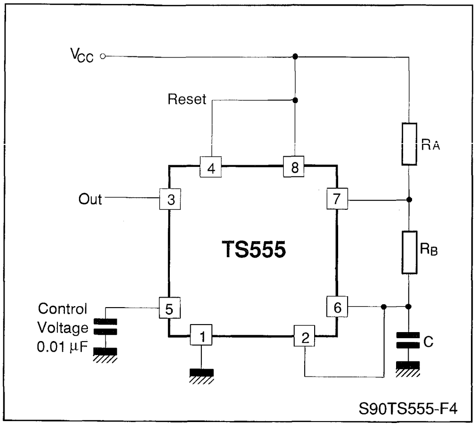
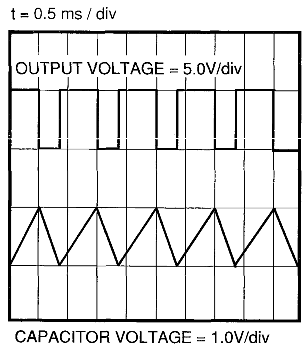


Figure 5.

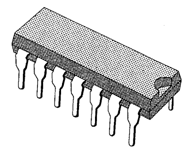


$R_A = R_B = 4.8\ k\Omega$, $C = 0.1\ \mu F$, $R_L = 1.0k\Omega$

S90TS555-F5

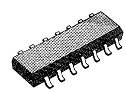
LOW POWER DUAL CMOS TIMERS

- VERY LOW POWER CONSUMPTION : 100µA typ / TIMER AT V_{CC} = 5V
- HIGH MAXIMUM ASTABLE FREQUENCY 2.7MHz
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR NE556
- VOLTAGE RANGE : +2V TO +18V
- HIGH OUTPUT CURRENT CAPABILITY
- SUPPLY CURRENT SPIKES REDUCED DURING OUTPUT TRANSITIONS
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$
- OUTPUT COMPATIBLE WITH TTL,CMOS AND LOGIC MOS



N
DIP14
(Plastic Package)

J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

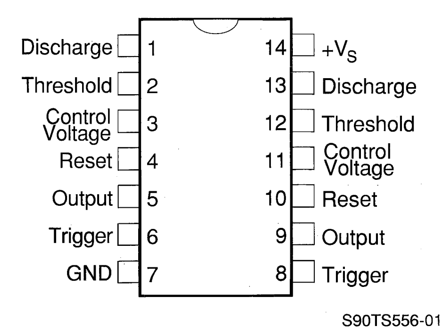
DESCRIPTION

The TS556 is a dual CMOS timer which offers very low consumption ($I_{CC(TYP)}$ TS556 = 200µA $I_{CC(TYP)}$ NE556 = 6mA) and high frequency ($f_{(MAX)}$ TS556 = 2.7MHz - $f_{(MAX)}$ NE556 = 0.1MHz) Thus, either in Monostable or Astable mode, timing remains very accurate.
The TS556 provides reduced supply current spikes during output transitions, which enables the use of lower decoupling capacitors compared to those required by bipolar NE556.
Timing capacitors can also be minimized due to high input impedance ($10^{12}\Omega$).

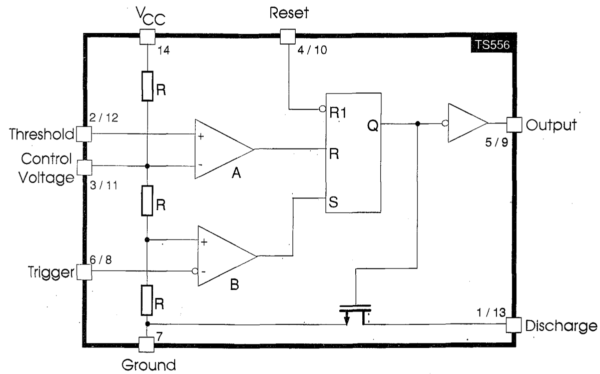
ORDER CODES

Part Number	Temperature Range	Package		
		N	D	J
TS556C	0 to +70°C	•	•	•
TS556I	-40 to +105°C	•	•	•
TS556M	-55 to +125°C	•	•	•
Examples : TS556CD , TS556IN				

PIN CONNECTION (top view)



BLOCK DIAGRAM (1/2 TS556)



S90TS556-02

FUNCTION TABLE

RESET	TRIGGER	THRESHOLD	OUTPUT
Low	x	x	Low
High	Low	x	High
High	High	High	Low
High	High	Low	Previous State

LOW ↔ Level Voltage ≤ Min voltage specified
HIGH ↔ Level Voltage ≥ Max voltage specified
X ↔ Irrelevant

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+18	V
T_J	Junction Temperature	+150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
T_{OPER}	Operating Temperature Range		°C
	TS556C	0 to +70	
	TS556I	-40 to +105	
	TS556M	-55 to +125	
T_{STG}	Storage Temperature Range	-65 to +150	°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+2 to +16	V

STATIC ELECTRICAL CHARACTERISTICS

V_{CC} = +2V , T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS556C - TS556I - TS556M			Unit
		Min	Typ	Max	
I_{CC}	Supply Current (no load, High and Low States) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 - -	 130 -	 400 400	µA
V_{CL}	Control Voltage T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 1.2 1.1	 1.3 -	 1.4 1.5	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 1mA) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 - -	 0.05 -	 0.2 0.25	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 1mA) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 - -	 0.1 -	 0.3 0.35	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -0.3mA) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 1.5 1.5	 1.9 -	 - -	V
V_{TRIG}	Trigger Voltage T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 0.4 0.3	 0.67 -	 0.95 1.05	V
I_{TRIG}	Trigger Current	-	10	-	pA
I_{TH}	Threshold Current	-	10	-	pA
V_{RESET}	Reset Voltage T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 0.4 0.3	 1.1 -	 1.5 2.0	V
I_{RESET}	Reset Current	-	10	-	pA
I_{DIS}	Discharge Pin Leakage Current	-	1	100	nA

STATIC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +5V , T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS556C - TS556I - TS556M			Unit
		Min	Typ	Max	
I_{CC}	Supply Current (no load, High and Low States) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 220 -	 500 500	µA
V_{CL}	Control Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 2.9 2.8	 3.3 -	 3.8 3.9	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 10mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.2 -	 0.3 0.35	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 8mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.3 -	 0.6 0.8	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -2mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 4.4 4.4	 4.6 -	 - -	V
V_{TRIG}	Trigger Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 1.36 1.26	 1.67 -	 1.96 2.06	V
I_{TRIG}	Trigger Current	-	10	-	pA
I_{TH}	Threshold Current	-	10	-	pA
V_{RESET}	Reset Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 0.4 0.3	 1.1 -	 1.5 2.0	V
I_{RESET}	Reset Current	-	10	-	pA
I_{DIS}	Discharge Pin Leakage Current	-	1	100	nA

STATIC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +12V , T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS556C - TS556I - TS556M			Unit
		Min	Typ	Max	
I_{CC}	Supply Current (no load, High and Low States) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 340 -	 800 800	µA
V_{CL}	Control Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 7.4 7.3	 8 -	 8.6 8.7	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 80mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.9 -	 1.6 2.0	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 50mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 1.2 -	 2 2.8	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -10mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 10.5 10.5	 11 -	 - -	V
V_{TRIG}	Trigger Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 3.2 3.1	 4 -	 4.8 4.9	V
I_{TRIG}	Trigger Current	-	10	-	pA
I_{TH}	Threshold Current	-	10	-	pA
V_{RESET}	Reset Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 0.4 0.3	 1.1 -	 1.5 2.0	V
I_{RESET}	Reset Current	-	10	-	pA
I_{DIS}	Discharge Pin Leakage Current	-	1	100	nA

DYNAMIC ELECTRICAL CHARACTERISTICS

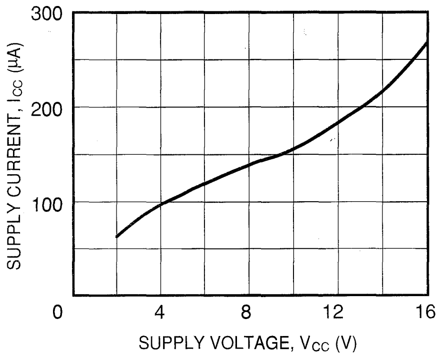
T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS556C - TS556I - TS556M			Unit
		Min	Typ	Max	
	Timing Accuracy (Monostable) - R = 10 kΩ , C = 0.1 μF - (Note 1) V_{CC} = +2V V_{CC} = +5V V_{CC} = +12V	 - - -	 1 2 4	 - - -	%
	Timing Shift with supply voltage variations (Monostable) R = 10 kΩ , C = 0.1 μF , V_{CC} = +5V ± 1V	-	0.38	-	%/V
	Timing Shift with temperature $T_{MIN} \leq T_{AMB} \leq T_{MAX}$, V_{CC} = +5V	-	75	-	ppm/ °C
f_{MAX}	Maximum astable frequency R_A = 470Ω , R_B = 200Ω , C = 200 pF , V_{CC} = +5V	-	2.7	-	MHz
	Astable frequency accuracy - (Note 2) R_A= R_B = 1kΩ to 100kΩ , C = 0.1μF V_{CC} = +5V V_{CC} = +12V	 - -	 3 3	 - -	%
	Timing Shift with supply voltage variations (Astable mode) R_A = R_B = 1kΩ to 100kΩ , C = 0.1μF , V_{CC} = +5 to +12V	-	0.1	-	%/V
t_r	Output Rise Time (V_{CC} = +5V , C_{LOAD}= 10pF)	-	25	-	ns
t_f	Output Fall Time (V_{CC} = +5V , C_{LOAD} = 10pF)	-	20	-	ns
t_{PD}	Trigger Propagation Delay (V_{CC} = +5V)	-	100	-	ns
t_{RPW}	Minimum Reset Pulse Width (V_{TRIG} = +5V)	-	350	-	ns

Notes : 1. See Figure 1
2. See Figure 2

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each timer) versus Supply Voltage.



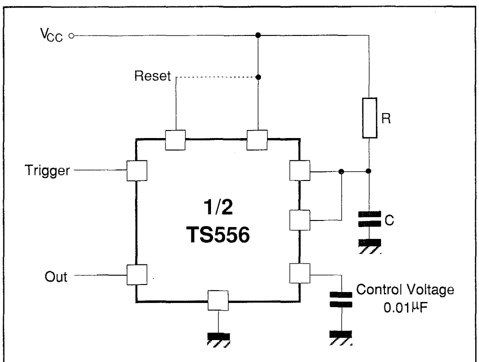
S90TS556-F1

APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode,the timer functions as a one-shot. Referring to figure 2 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 2.



S90TS556-F2

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered,the circuit remains in this state until the set time has elapsed,even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R x C.

Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4 or 10) and the Trigger terminal (pin 6 or 8) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to the trigger terminal, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant τ = R x C.

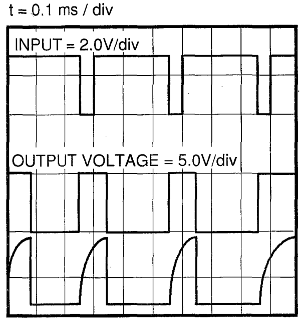
When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state.

Figure 3 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possible or false triggering.

Figure 3.

t = 0.1 ms / div



CAPACITOR VOLTAGE = 2.0V/div

R = 9.1kΩ, C = 0.01µF , R_L = 1.0kΩ

S90TS556-F3

ASTABLE OPERATION

When the circuit is connected as shown in figure 4, it triggers itself and free runs as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency, are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by :

$t1 = 0.693\ (R_A + R_B)\ C$

and the discharge time (output LOW) by :

$t2 = 0.693\ (R_B)\ C$

Thus the total period T is given by :

$T = t1 + t2 = 0.693\ (R_A + 2R_B)\ C$

The frequency of oscillation is then :

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

The duty cycle is given by : $D = \dfrac{R_B}{R_A + 2R_B}$

Figure 4.

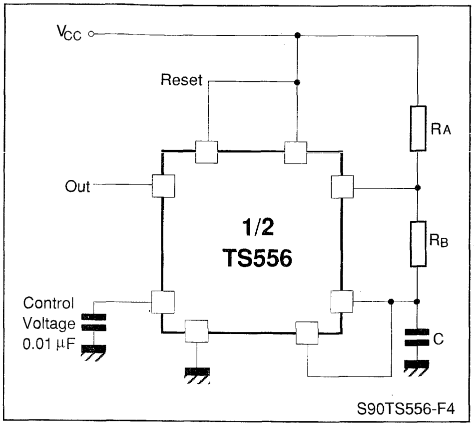
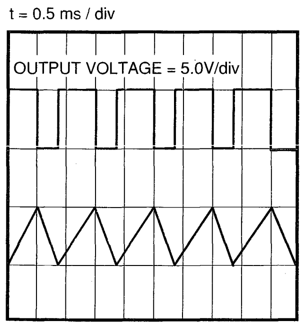


Figure 5.



CAPACITOR VOLTAGE = 1.0V/div

$R_A = R_B = 4.8\ k\Omega,\ C = 0.1\,\mu F\ ,\ R_L = 1.0k\Omega$

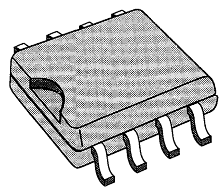
S90TS556-F5

PACKAGES

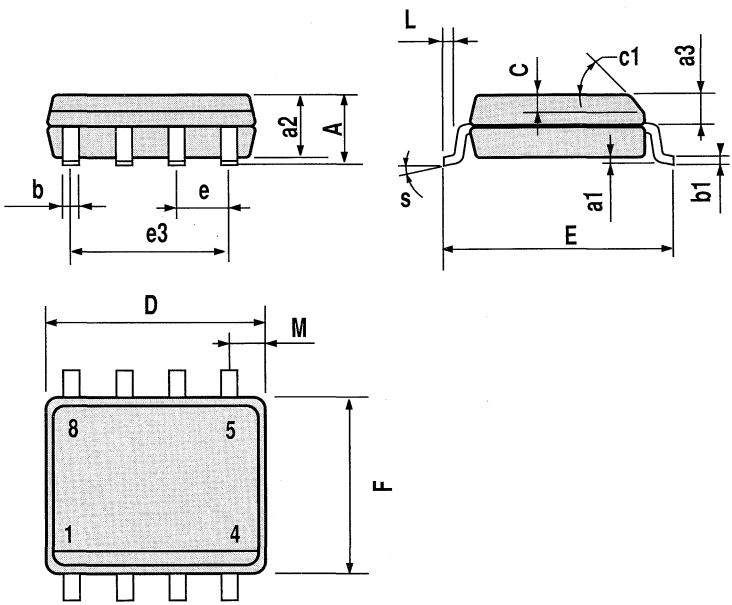
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO8

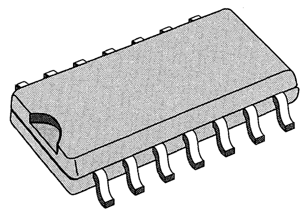


P013M

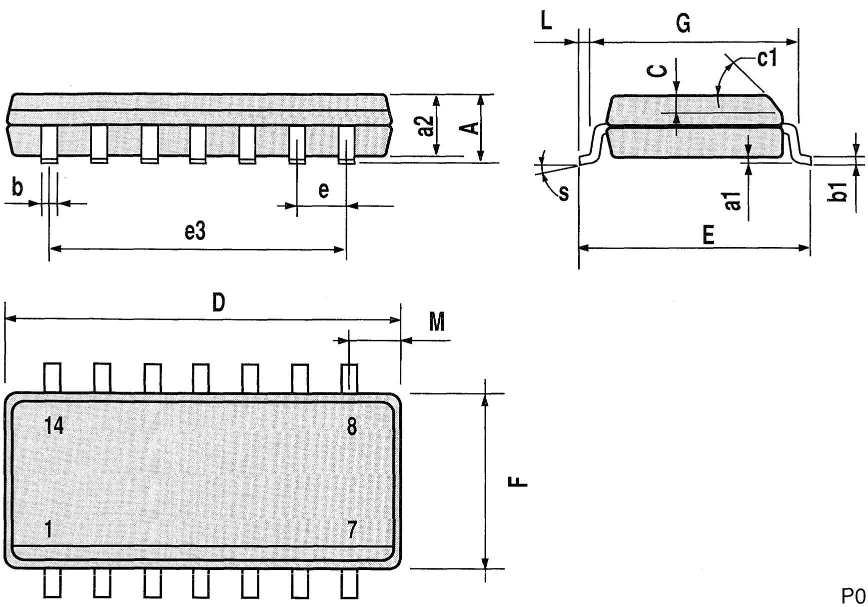
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.15		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



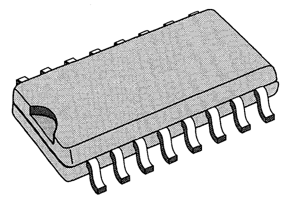
SO14



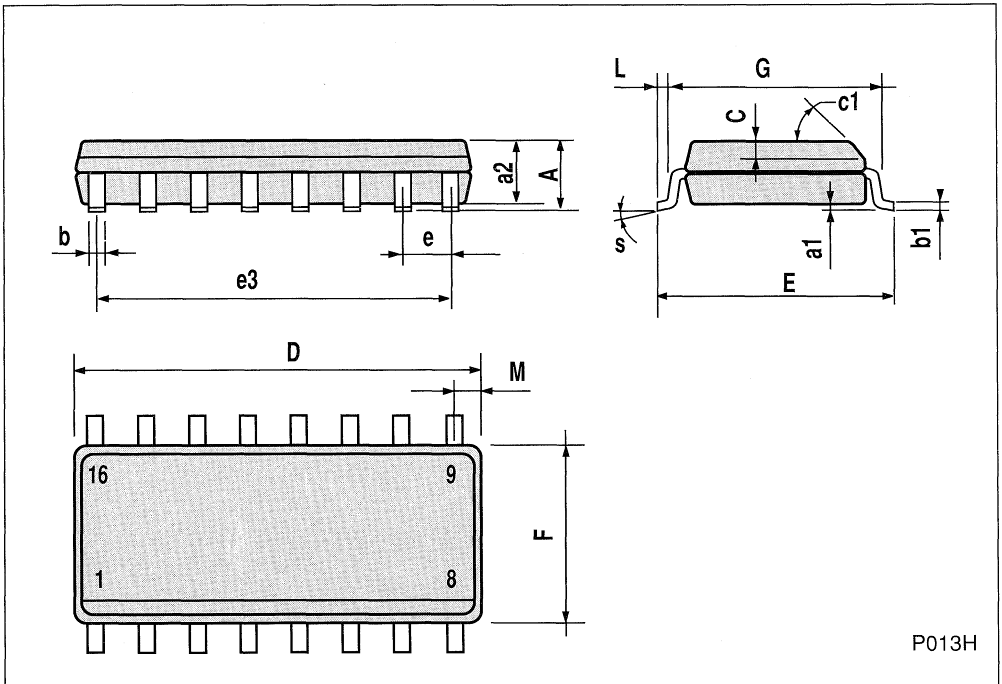
SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.5		1.27	0.020		0.050
M			0.62			0.024
S	8° (max.)					



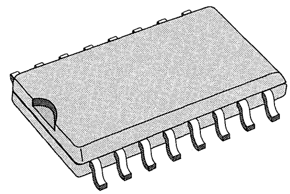
SO16



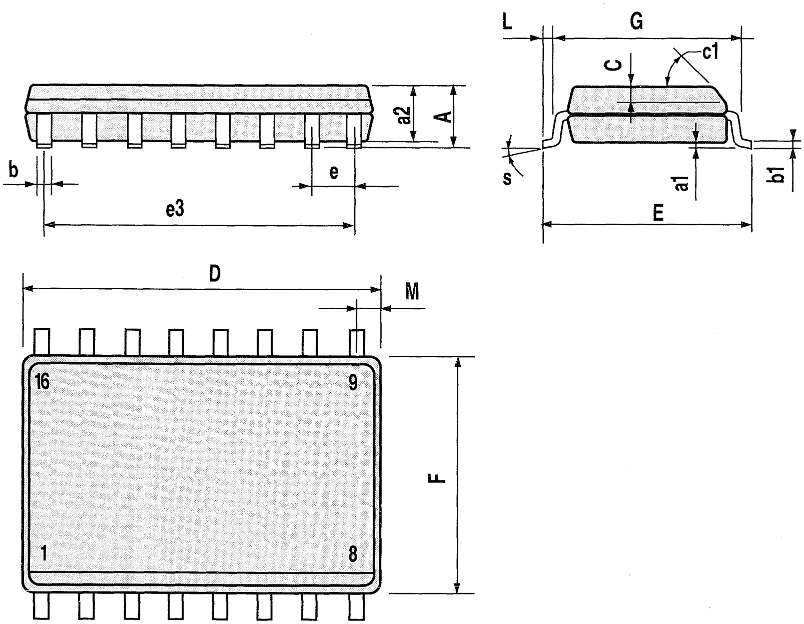
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.397		0.413
E	10.0		10.65	0.393		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.300
G	8.8		9.15	0.346		0.360
L	0.5		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO16L

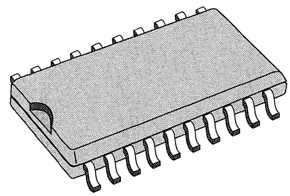


P013I

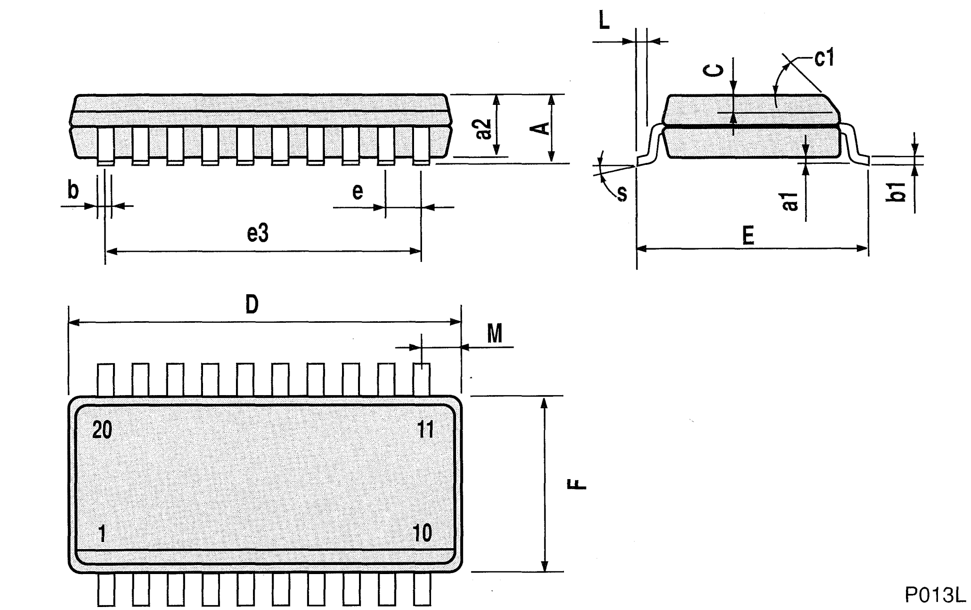
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



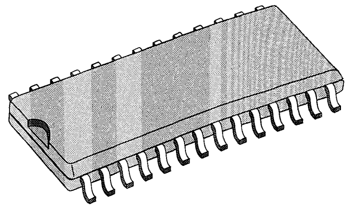
SO20



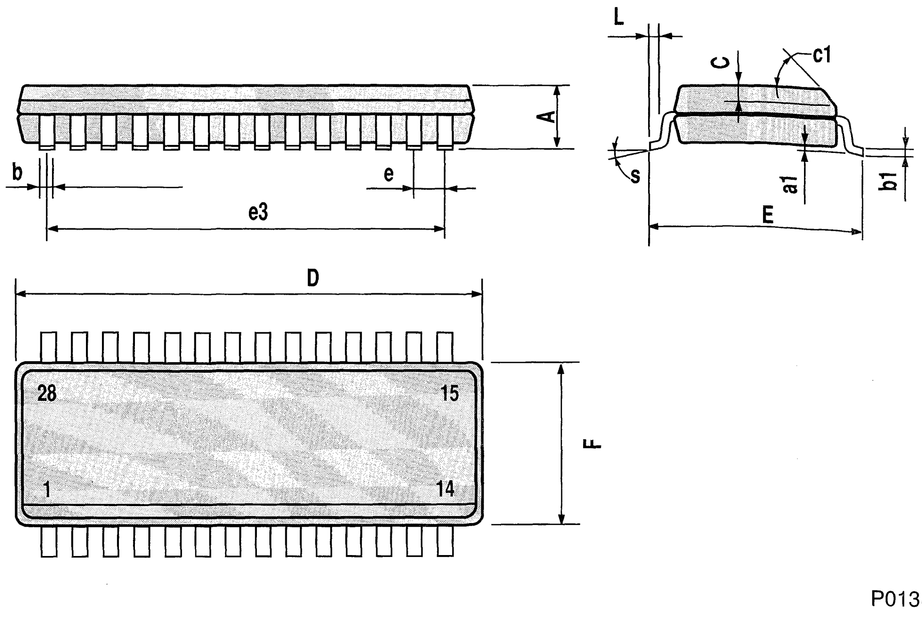
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



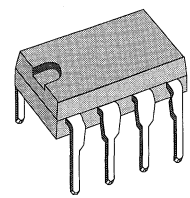
SO28



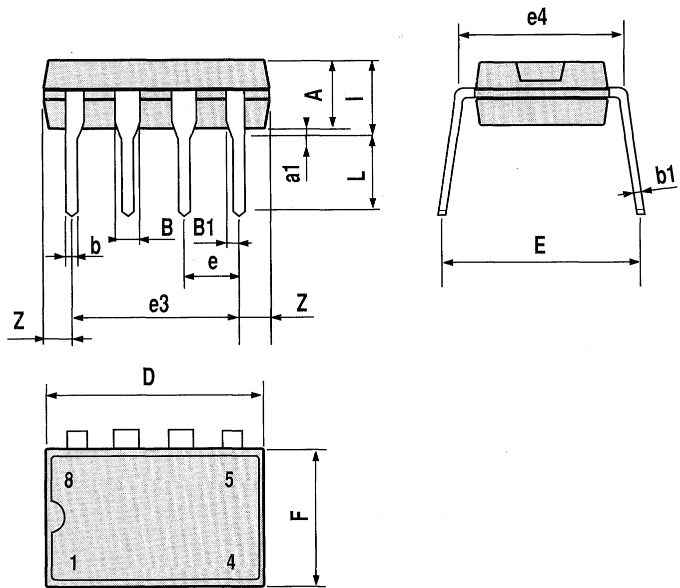
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Minidip (0.25)

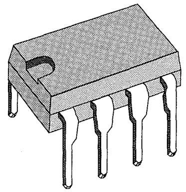


P001W

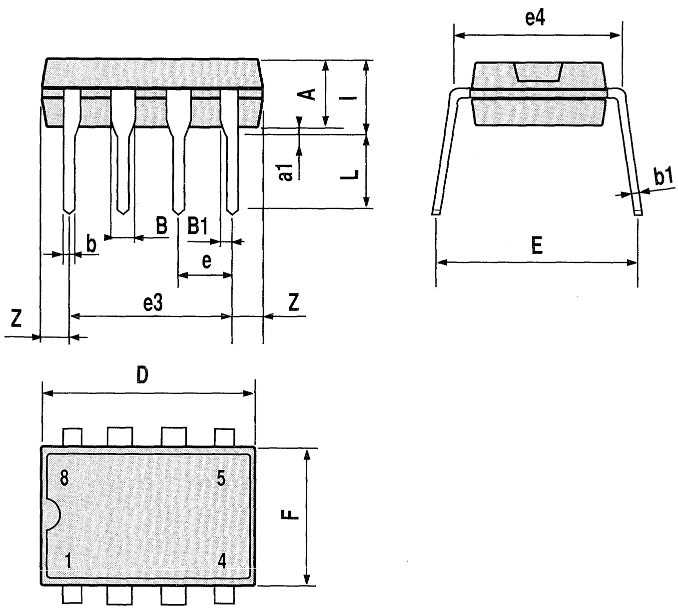
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Minidip (0.4)

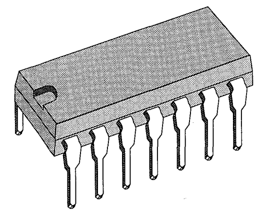


P001F

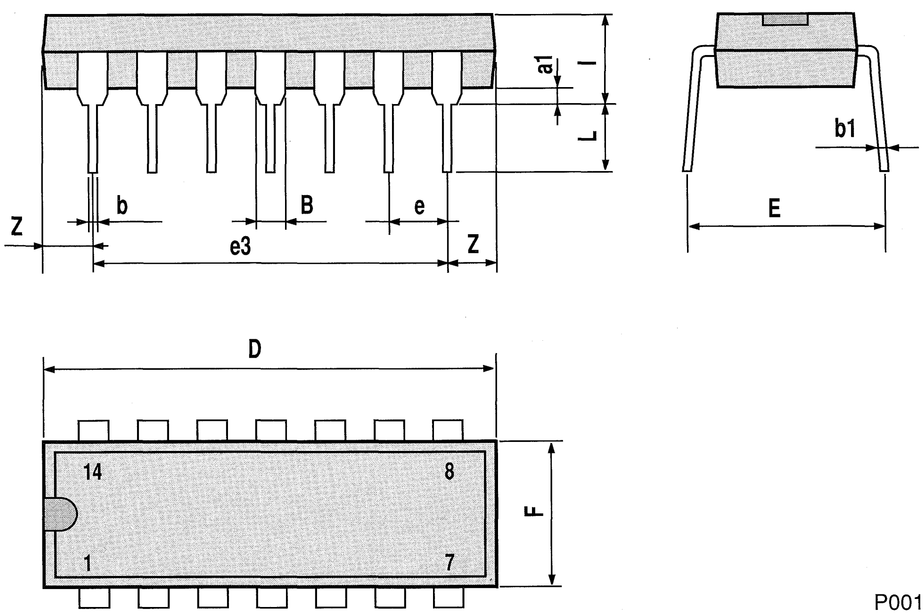
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP14

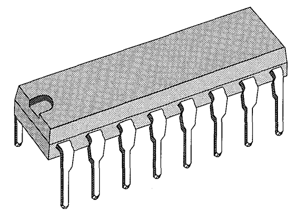


P001A

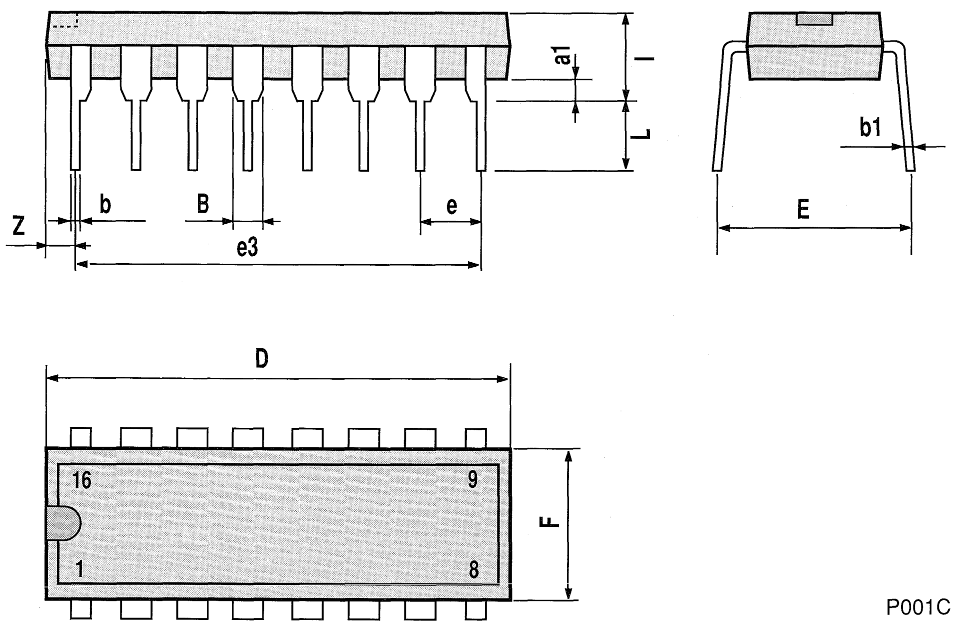
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



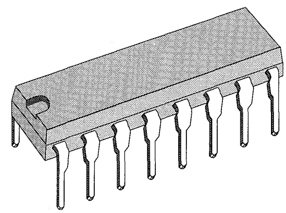
DIP16 (0.25)



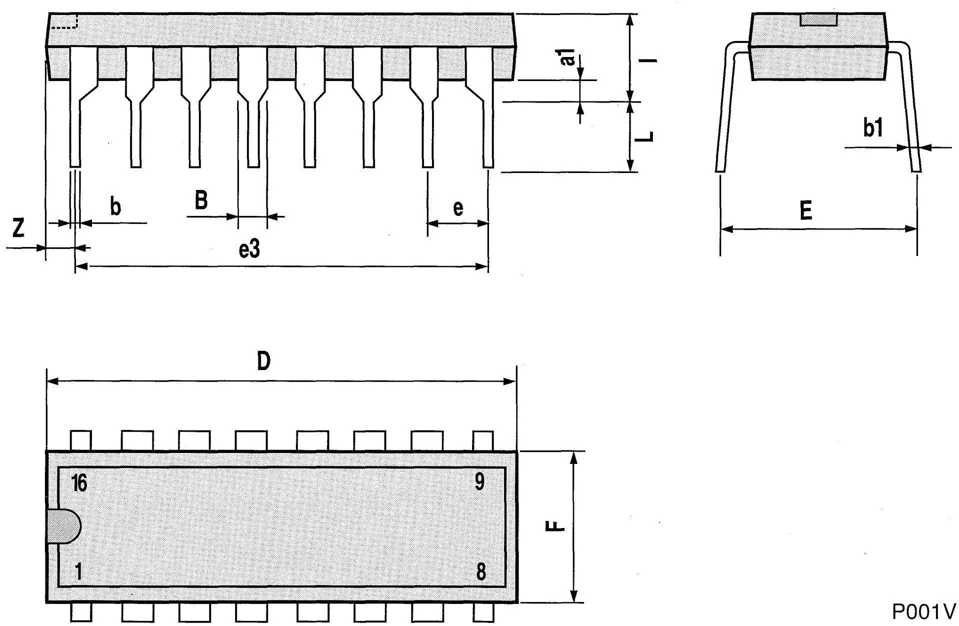
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			20			0.787
E		8.8			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



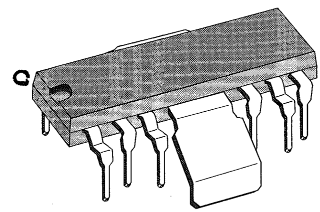
POWERDIP: (8+8), (12+2+2)



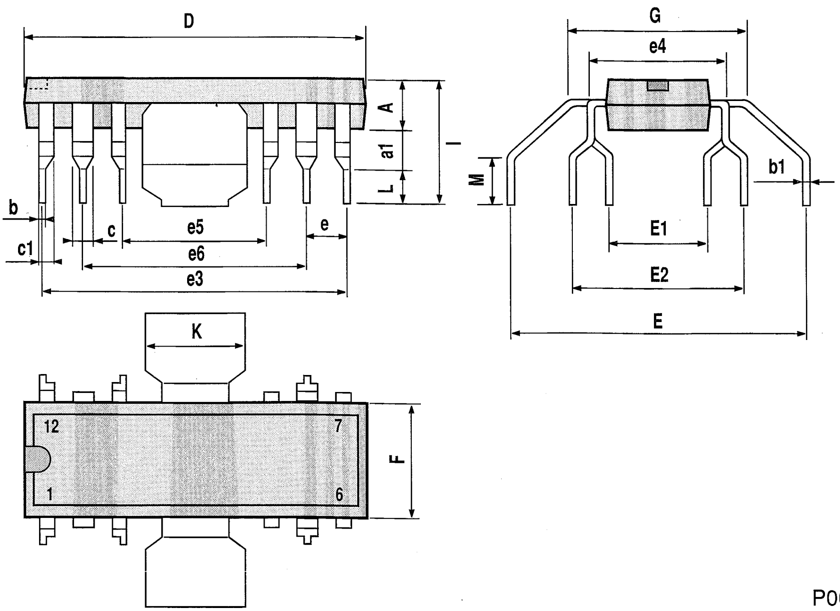
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.8		4.05	0.150		0.159
a1	1.5		1.75	0.059		0.069
b	0.55		0.6	0.022		0.024
b1	0.3		0.35	0.012		0.014
c		1.32			0.052	
c1		0.94			0.037	
D	19.2		19.9	0.756		0.783
E	16.8	17.2	17.6	0.661	0.677	0.693
E1	4.86		5.56	0.191		0.219
E2	10.11		10.81	0.398		0.426
e	2.29	2.54	2.79	0.090	0.100	0.110
e3	17.43	17.78	18.13	0.686	0.700	0.714
e4		7.62			0.300	
e5	7.27	7.62	7.97	0.286	0.300	0.314
e6	12.35	12.7	13.05	0.486	0.500	0.514
F	6.3		7.1	0.248		0.280
G		9.8			0.386	
I	7.8		8.6	0.307		0.339
K	6.1		6.5	0.240		0.256
L	2.5		2.9	0.098		0.114
M	2.5		3.1	0.098		0.122

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Findip

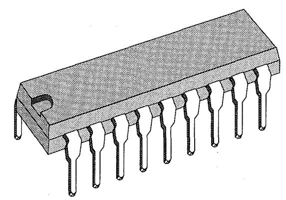


P001H

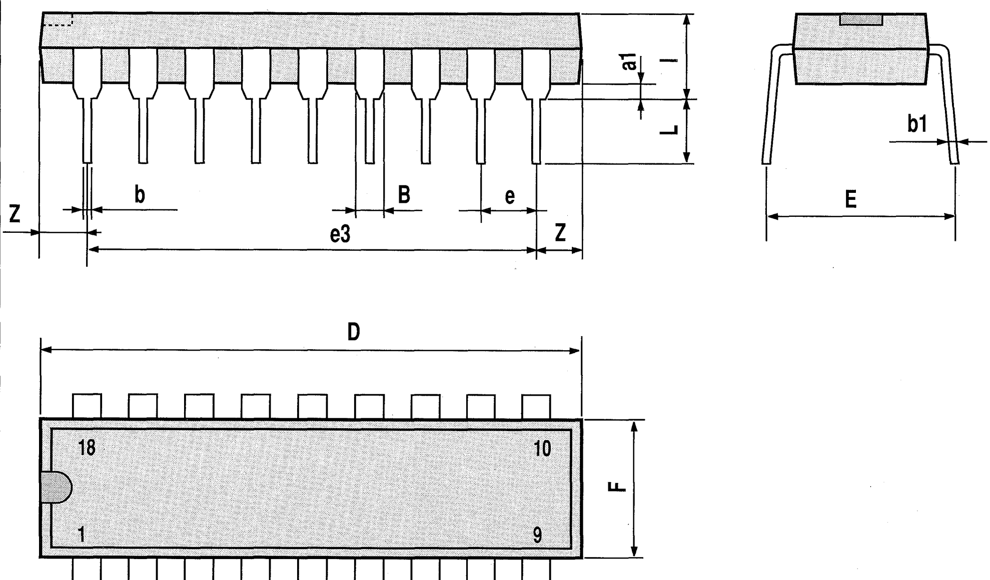
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.064
b		0.46			0.018	
b1		0.25			0.010	
D			23.24			0.914
E		8.5			0.335	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z		1.27	1.59		0.050	0.062

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP18 (0.25)

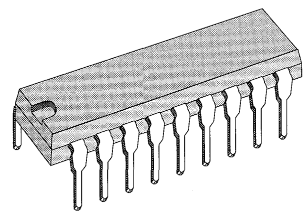


P001T

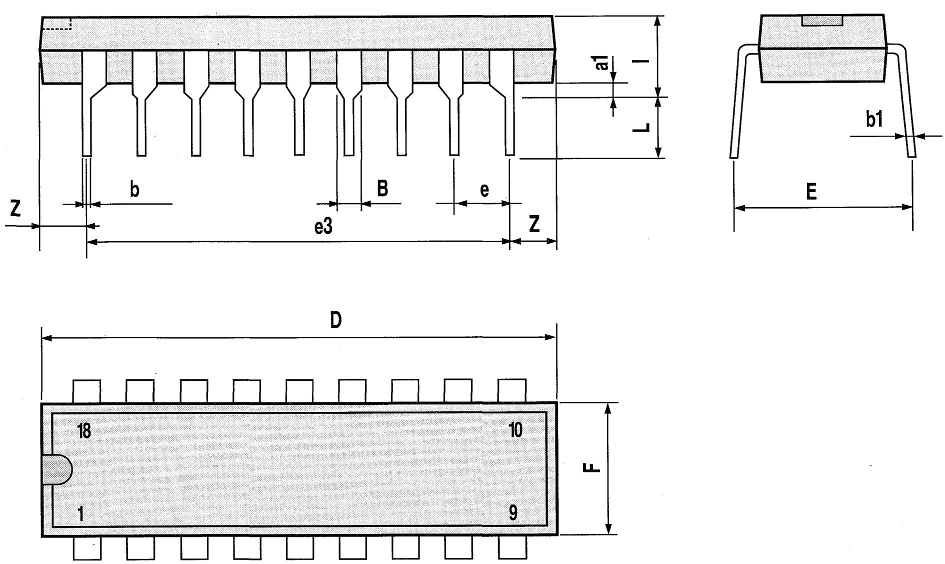
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			2.54			0.100

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP: (9+9), (12+3+3)

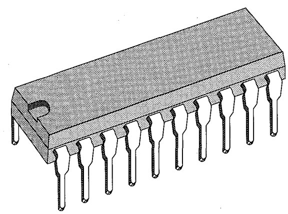


P001U

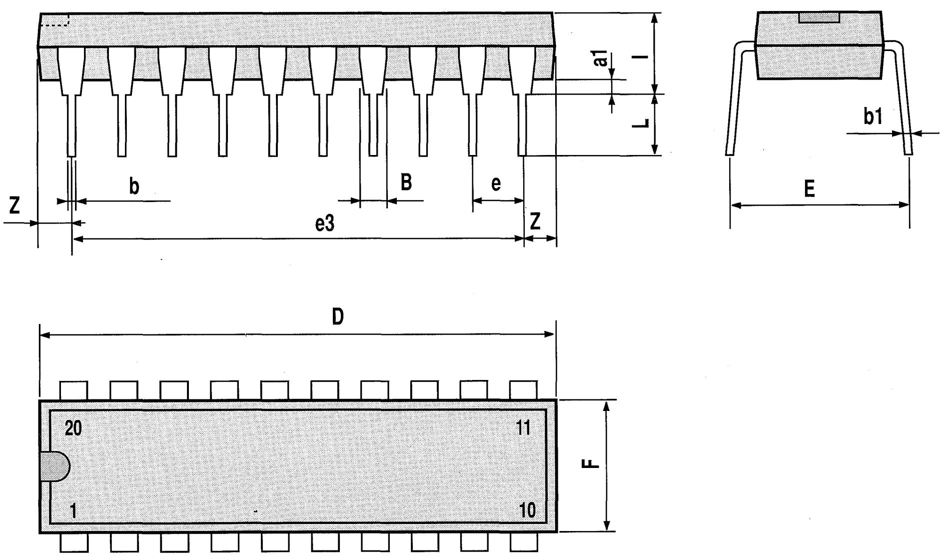
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP20 (0.25)

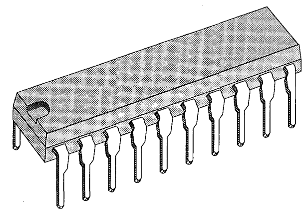


P001J

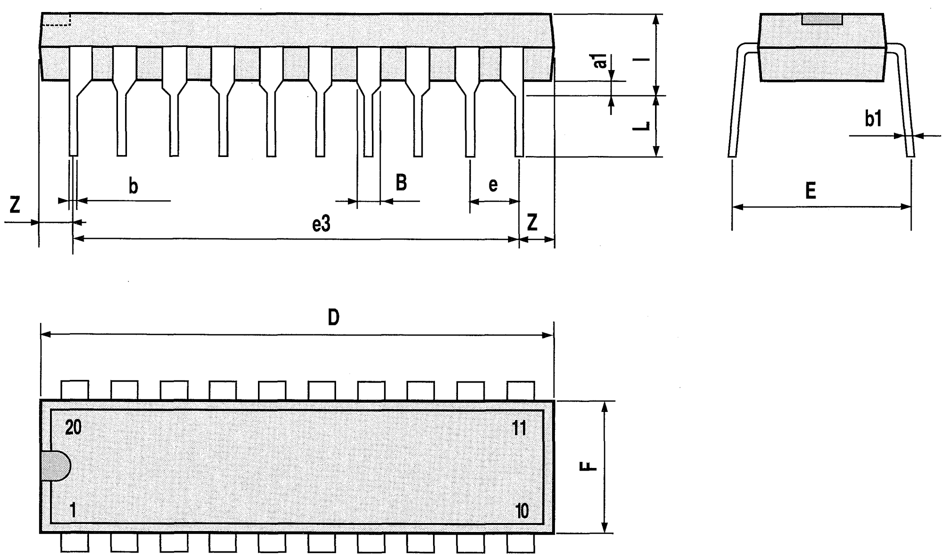
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP (16+2+2)

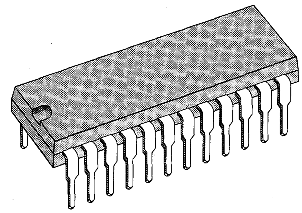


P001X

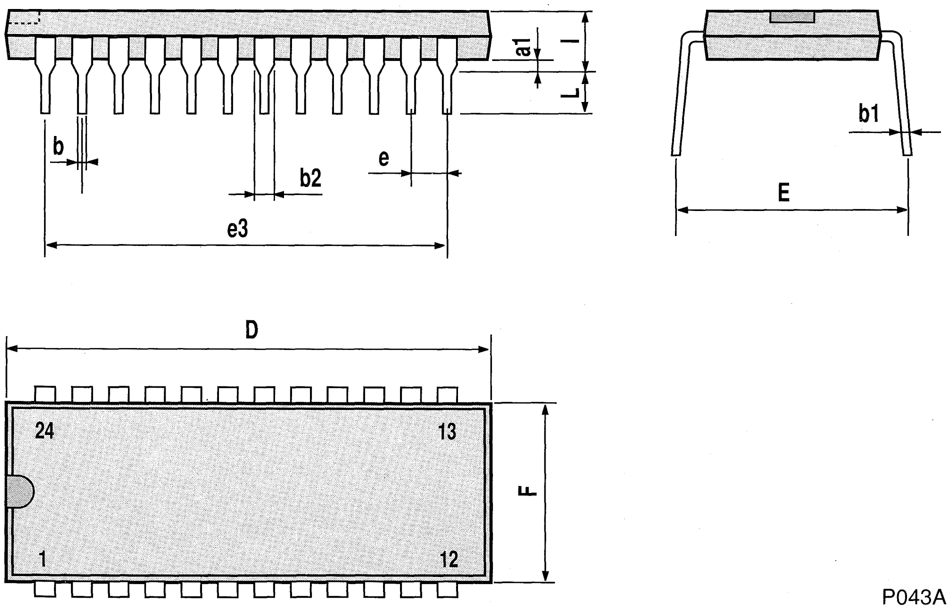
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP24 (0.25)

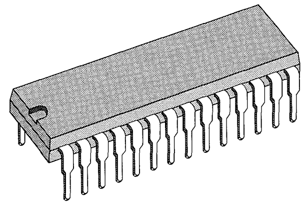


P043A

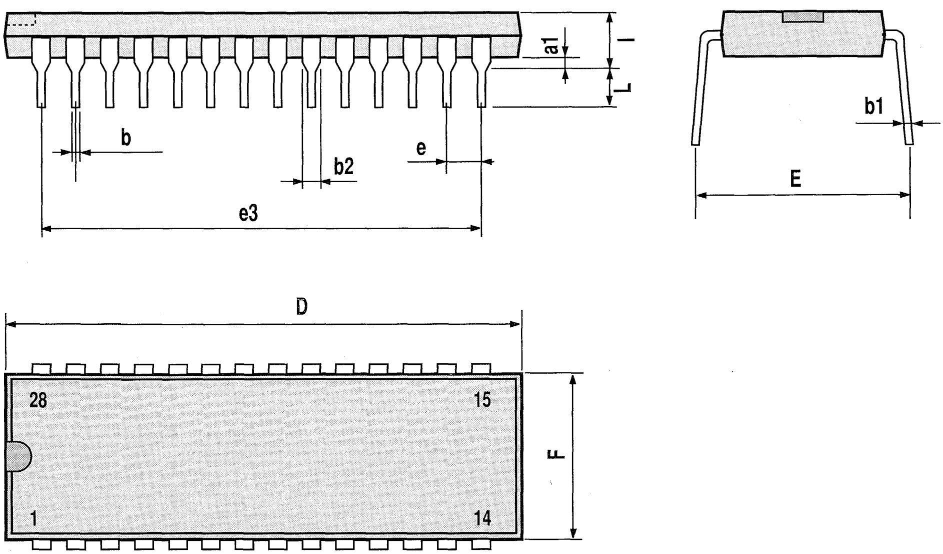
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



DIP28

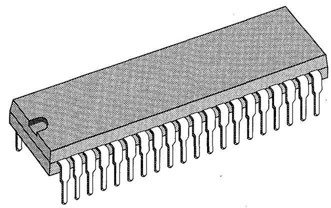


P043D

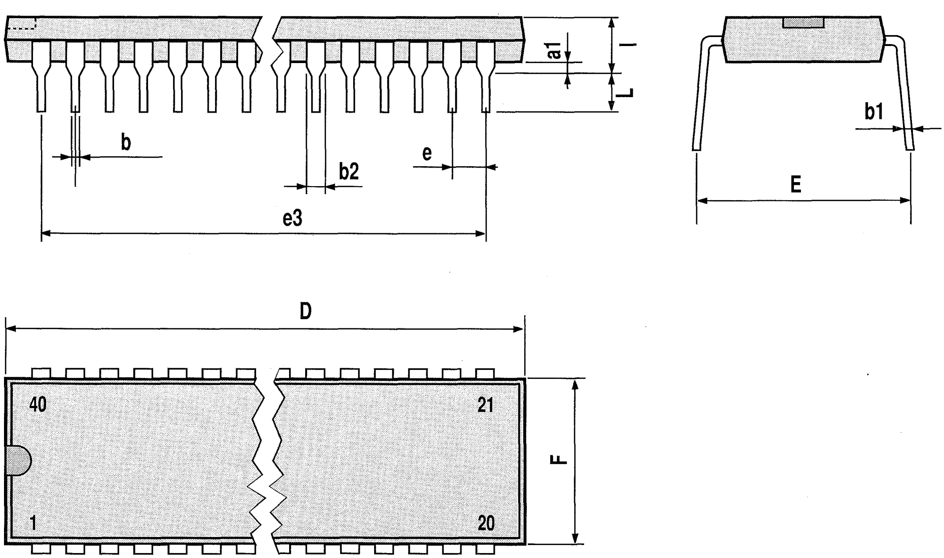
DIM.	mm			inch		
	MIN	TYP	MAX	MIN	TYP	MAX
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP40

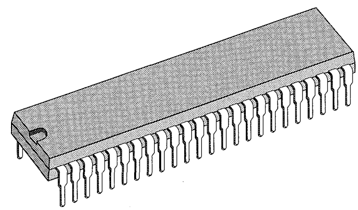


P043E

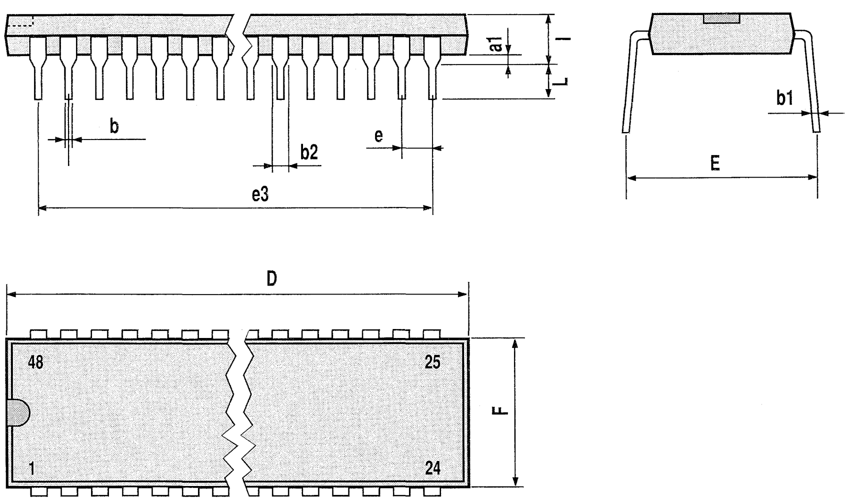
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			62.74			2.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		58.42			2.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP48

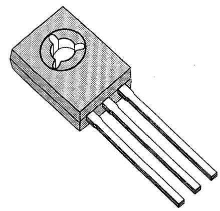


P043F

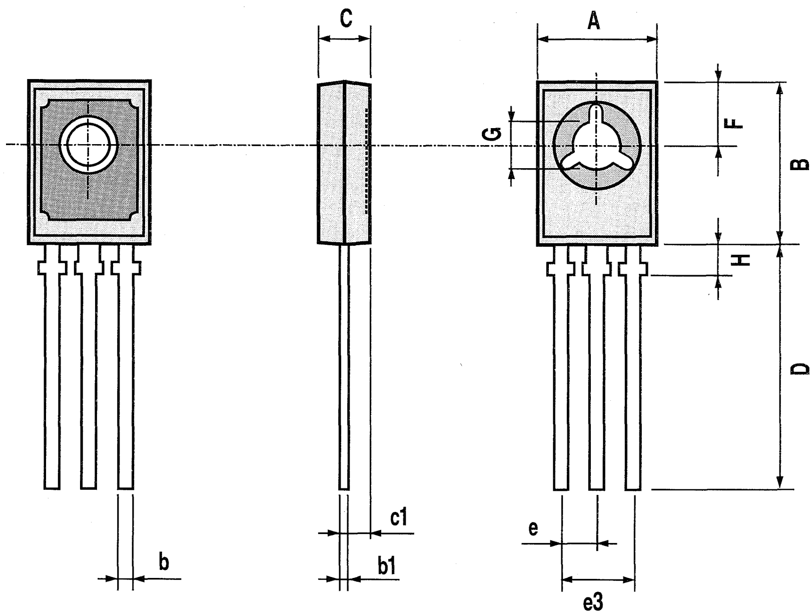
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		10.8	0.413		0.425
b	0.7		0.9	0.028		0.035
b1	0.49		0.75	0.019		0.030
C	2.4		2.7	0.094		0.106
c1		1.2			0.047	
D	15.7			0.618		
e		2.2			0.087	
e3		4.4			0.173	
F		3.8			0.150	
G	3		3.2	0.118		0.126
H			2.54			0.100

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SOT32

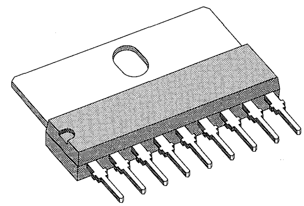


P032

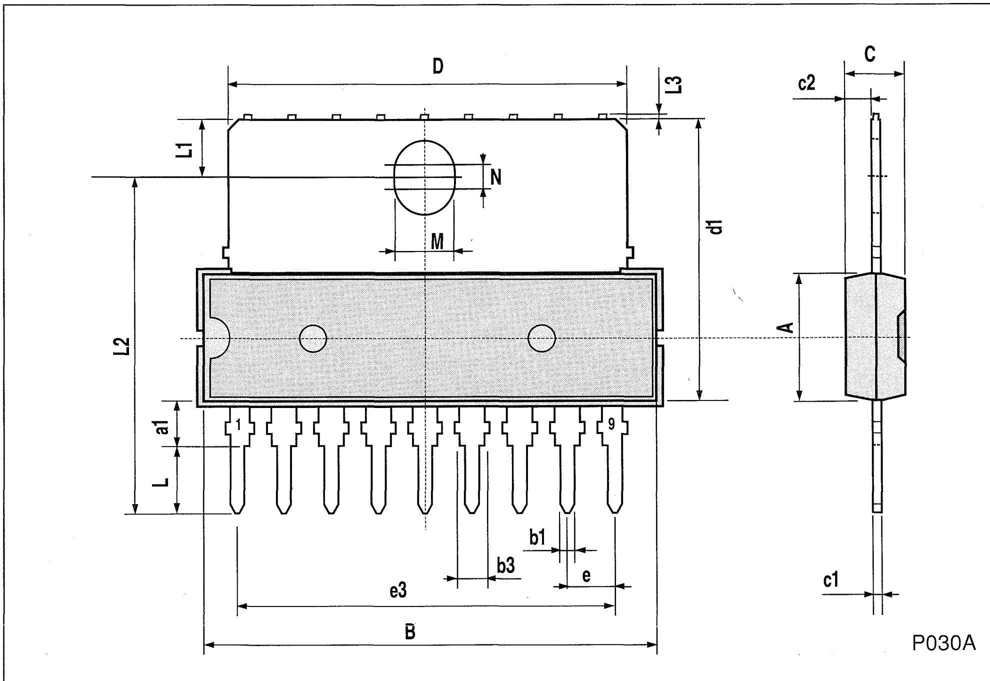
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



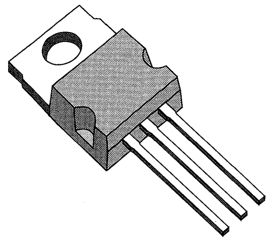
SIP9



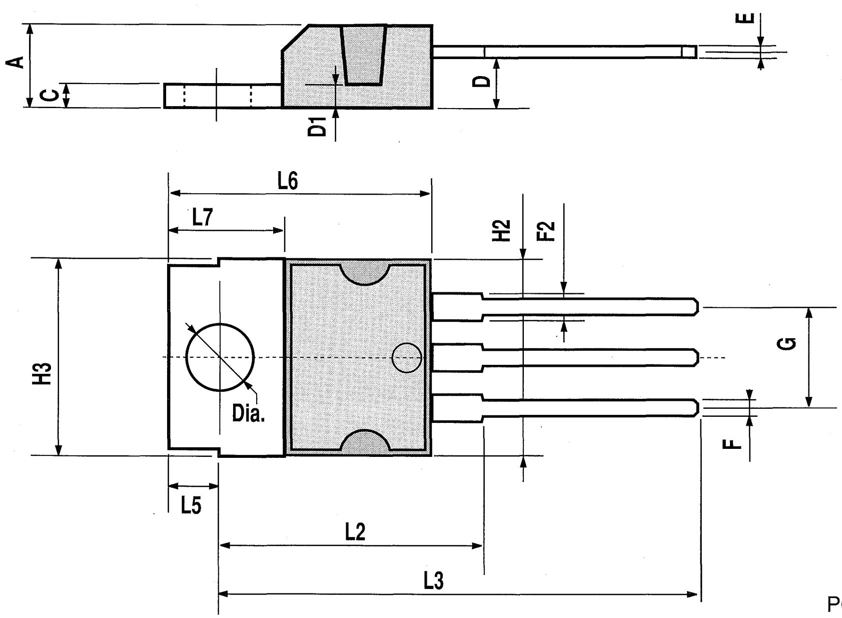
SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F2	1.15		1.4	0.045		0.055
G	4.95	5.08	5.21	0.195	0.200	0.205
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L2		16.2			0.638	
L3	26.3	26.7	27.1	1.035	1.051	1.067
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia	3.65		3.85	0.144		0.152



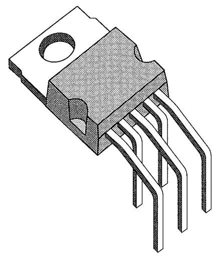
TO220



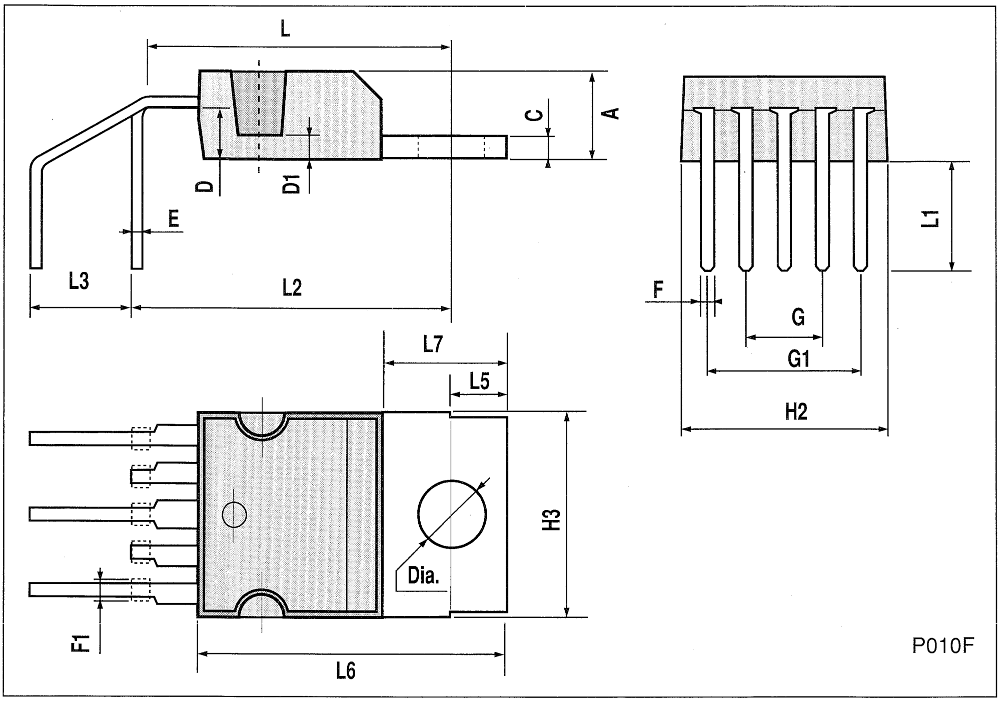
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G	3.2	3.4	3.6	0.126	0.134	0.142
G1	6.6	6.8	7	0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		14.2			0.559	
L1		6			0.236	
L2		14.8			0.583	
L3	3.6		4.2	0.142		0.165
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



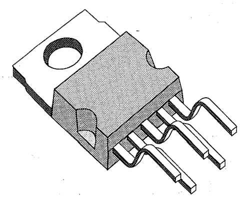
Pentawatt H



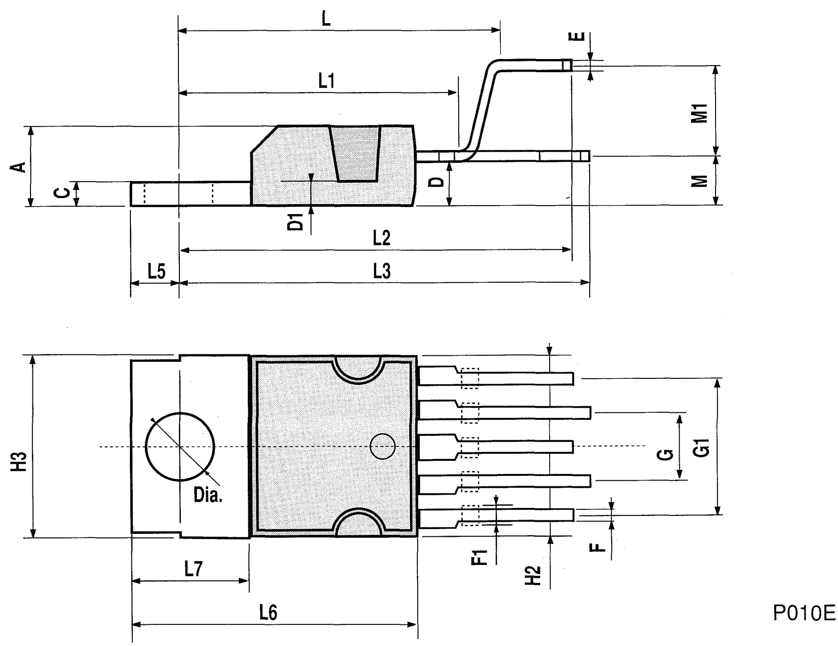
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G	3.2	3.4	3.6	0.126	0.134	0.142
G1	6.6	6.8	7	0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



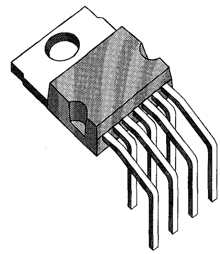
Pentawatt V



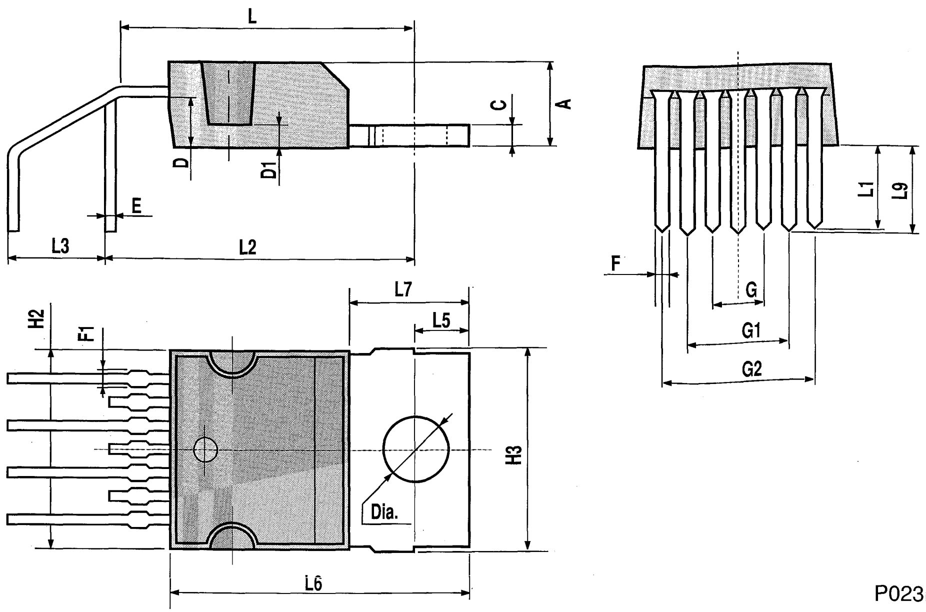
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		14.2			0.559	
L1		4.4			0.173	
L2		15.8			0.622	
L3		5.1			0.201	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
L9		4.44			0.175	
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Heptawatt H

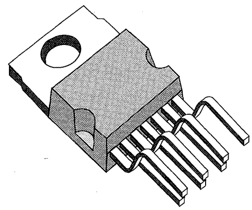


P023B

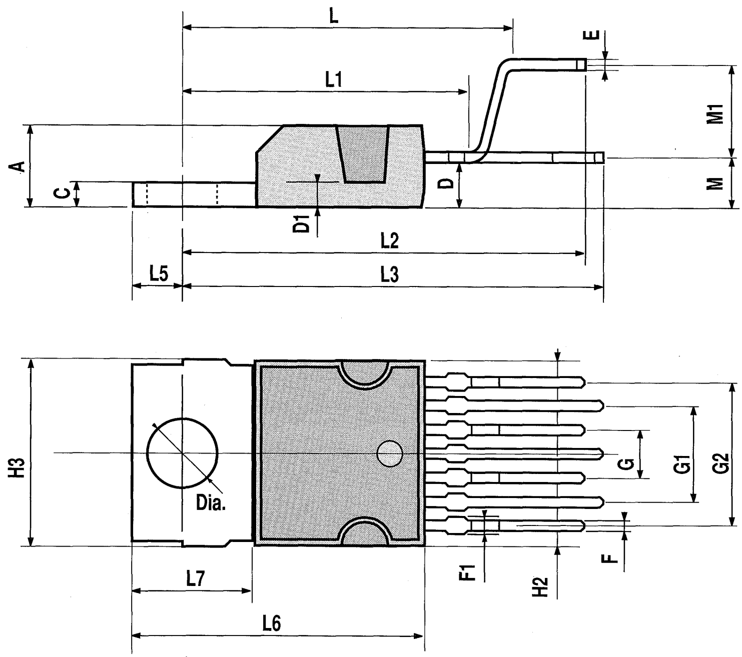
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Heptawatt V

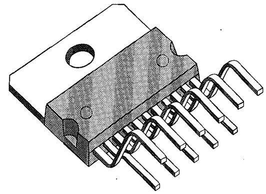


P023A

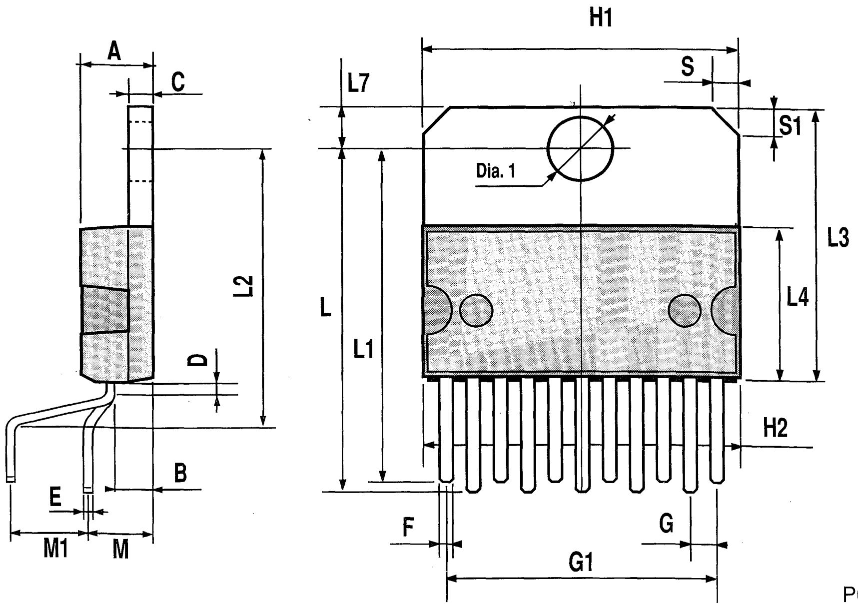
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.88		0.95	0.035		0.037
G	1.57	1.7	1.83	0.062	0.067	0.072
G1	16.87	17	17.13	0.664	0.669	0.674
H1	19.6			0.772		
H2			20.2			0.795
L	21.5		22.3	0.846		0.878
L1	21.4		22.2	0.843		0.874
L2	17.4		18.1	0.685		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.1	4.3	4.5	0.161	0.169	0.177
M1	4.88	5.08	5.3	0.192	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Multiwatt11 V

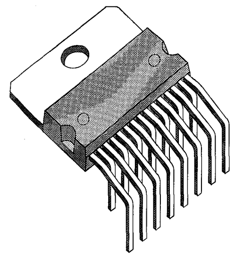


P017A

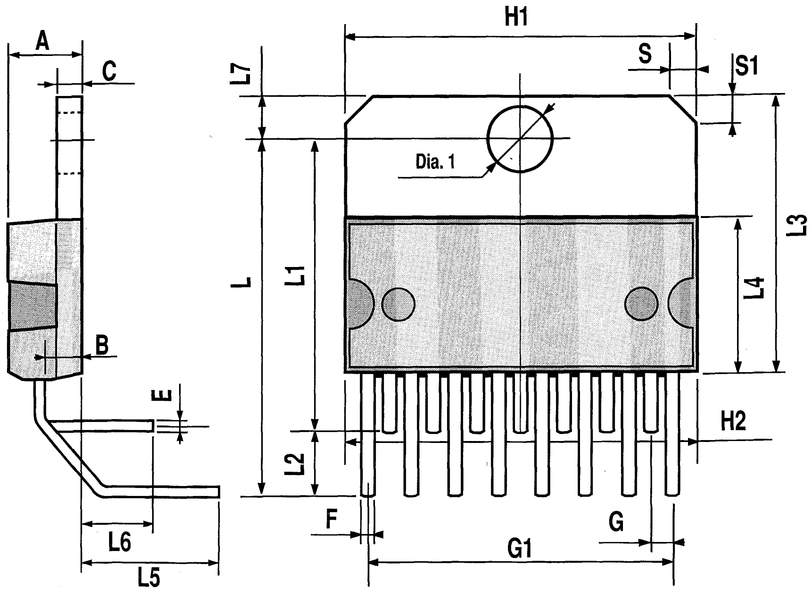
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L		20.57			0.810	
L1		18.03			0.710	
L2		2.54			0.100	
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L5		5.28			0.208	
L6		2.38			0.094	
L7	2.65		2.9	0.104		0.114
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON
MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Multiwatt15 H



P017H

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

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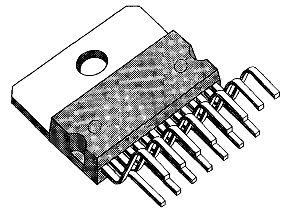
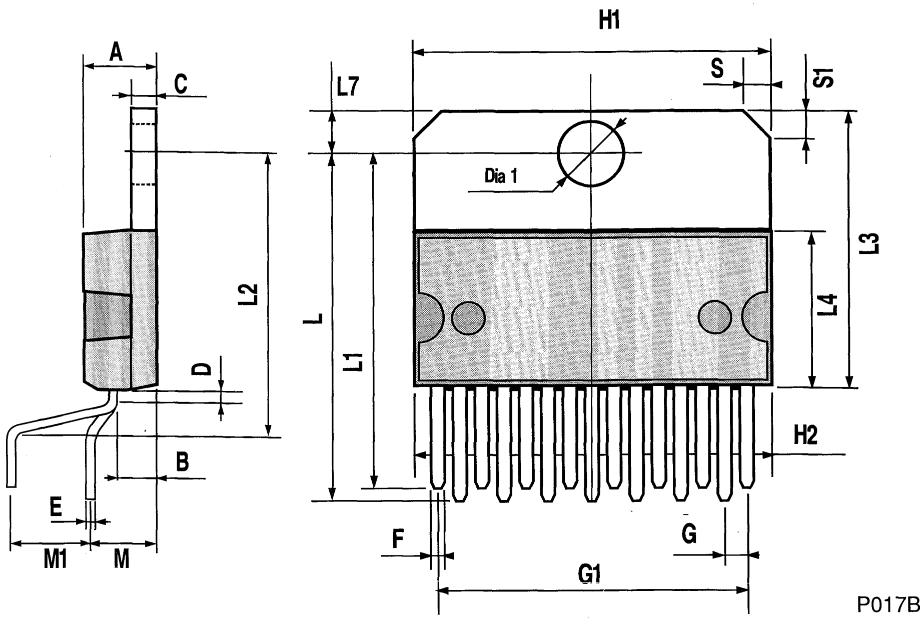
OUTLINE AND MECHANICAL DATA



Multiwatt15 V



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Cover design by Keith & Koppel, Segrate, Italy
Typesetting and layout on Desk Top Publishing
Printed by Grafiche Moretti, Segrate, Italy

ORDER CODE: DBAUDIOPROST/1